

**Description**

The AP7335A is a 300mA, 5.0V fixed output voltage, low dropout linear regulator with  $\pm 1\%$  output voltage accuracy. The device included pass element, error amplifier, band-gap, current limit and thermal shutdown circuitry. The device is turned on when EN pin is set to logic high level.

The characteristics of low dropout voltage and low quiescent current make it suitable for low power applications, for example, battery powered devices. The typical quiescent current is 35 $\mu$ A. Built-in current-limit and thermal-shutdown functions prevent IC from damage in fault conditions.

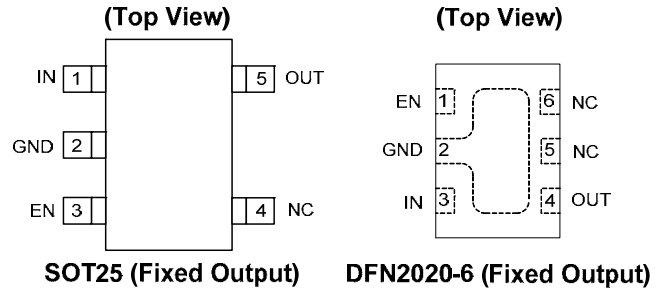
This device is only available as 5.0V fixed version. Please contact your local sales office for any other voltage options.

The AP7335A is packaged in SOT25 and DFN2020-6.

**Applications**

- Smart Phones
- MP3/MP4
- Battery-powered devices
- Bluetooth headset
- Battery Charger
- LCD TV
- Multifunction Monitors

**Pin Assignments**

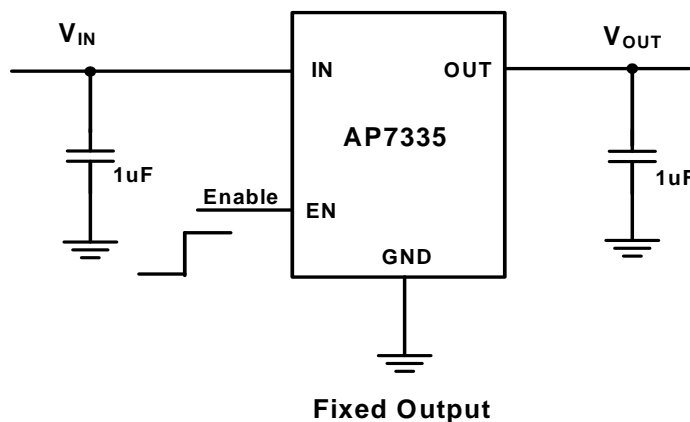


**Features**

- 300mA Low Dropout Regulator with EN
- Very low  $I_Q$  35 $\mu$ A
- Fixed output at 5.0V
  - $V_{IN\ MIN}$  5.5V
- High PSRR: 65dB at 1kHz
- Fast start-up time 220 $\mu$ s
- Stable with low ESR, 1 $\mu$ F ceramic output capacitor
- Excellent Load/Line Transient Response
- Low dropout 150mV at 300mA
- Current limit and short circuit protection
- Thermal shutdown protection
- Ambient temperature range -40°C to 85°C
- SOT25, and DFN2020-6 Available in "Green" Molding Compound (No Br, Sb)
- Lead Free Finish/ RoHS Compliant (Note 1)

Note: 1. EU Directive 2002/95/EC (RoHS). All applicable RoHS exemptions applied. Please visit our website at [http://www.diodes.com/products/lead\\_free.html](http://www.diodes.com/products/lead_free.html).

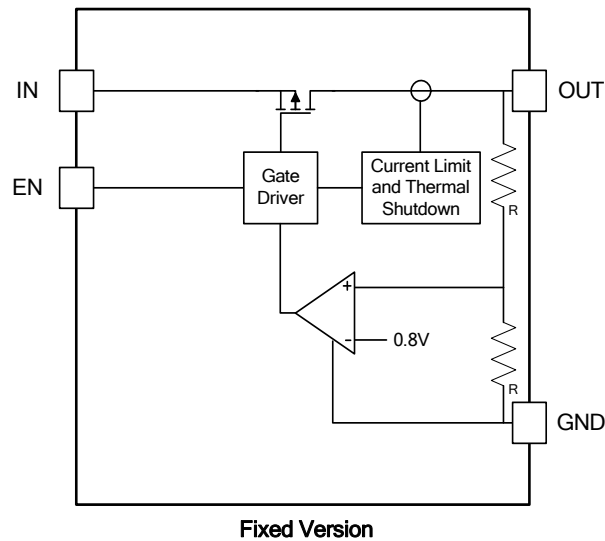
**Typical Application Circuit**



**Pin Descriptions**

Pin Name	Pin Number		Description
	SOT25 (fixed)	DFN2020-6 (fixed)	
IN	1	3	Voltage input pin. Bypass to ground through at least 1µF MLCC capacitor
GND	2	2	Ground
EN	3	1	Enable input, active high
ADJ	-	-	Output feedback pin
NC	4	5, 6	No connection
OUT	5	4	Voltage output pin. Bypass to ground through 1µF MLCC capacitor

**Functional Block Diagram**



### Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
ESD HBM	Human Body Model ESD Protection	2000	V
ESD MM	Machine Model ESD Protection	200	V
$V_{IN}$	Input Voltage	6.5	V
	OUT, EN Voltage	$V_{IN} + 0.3$	V
	Continuous Load Current per Channel	Internal Limited	
$T_{ST}$	Storage Temperature Range	-65 to 150	°C
$T_J$	Maximum Junction Temperature	150	°C

Stresses greater than the 'Absolute Maximum Ratings' specified above, may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.

### Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
$V_{IN}$	Input voltage (Note 3)	2 (Note 3)	6	V
$I_{OUT}$	Output Current (Note 2)	0	300	mA
$T_A$	Operating Ambient Temperature	-40	85	°C

Notes: 2. The device maintains a stable, regulated output voltage without a load current.  
3.  $V_{IN(MIN)} = 5.5V$  for 5.0V,  $V_{OUT}$  at 300mA  $I_{OUT}$

### Electrical Characteristics

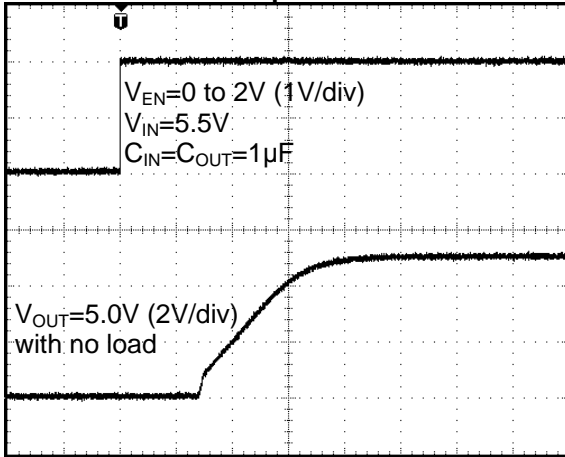
( $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 5.5$  to  $6\text{V}$ ,  $C_{IN} = 1\mu\text{F}$ ,  $C_{OUT} = 1\mu\text{F}$ ,  $V_{EN} = 2\text{V}$ , unless otherwise stated)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{OUT}$	Output Voltage Accuracy	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ , $I_{OUT} = 10\%$ of $I_{OUT-Max}$	-1		1	%
$\frac{\Delta V_{OUT}}{\Delta V_{IN}/V}$	Line Regulation	$V_{IN} = 5.5\text{V}$ to $6\text{V}$ , $V_{EN} = V_{IN}$ , $I_{OUT} = 1\text{mA}$		0.02	0.20	%/V
$\frac{\Delta V_{OUT}}{I_{OUT}}$	Load Regulation	$V_{IN} = 5.5\text{V}$ to $6\text{V}$ , $I_{OUT} = 1\text{mA}$ to $300\text{mA}$	-0.6		0.6	%
$V_{DROPOUT}$	Dropout Voltage (Note 4)	$I_{OUT} = 300\text{mA}$		150	200	mV
$I_Q$	Input Quiescent Current	$V_{EN} = V_{IN}$ , $I_{OUT} = 0\text{mA}$		35	80	$\mu\text{A}$
$I_{SHDN}$	Input Shutdown Current	$V_{EN} = 0\text{V}$ , $I_{OUT} = 0\text{mA}$		0.1	1	$\mu\text{A}$
$I_{LEAK}$	Input Leakage Current	$V_{EN} = 0\text{V}$ , OUT grounded		0.1	1	$\mu\text{A}$
$t_{ST}$	Start-up Time	$V_{EN} = 0\text{V}$ to $2.0\text{V}$ in $1\mu\text{s}$ , $I_{OUT} = 300\text{mA}$		220		$\mu\text{s}$
PSRR	PSRR	$V_{IN} = 5.5\text{V}_{DC} + 0.5\text{V}_{ppAC}$ , $f = 1\text{kHz}$ , $I_{OUT} = 50\text{mA}$		65		dB
$I_{SHORT}$	Short-circuit Current	$V_{IN} = V_{IN-Min}$ to $V_{IN-Max}$ , $V_{OUT} < 0.2\text{V}$ (fixed) or		160		mA
$I_{LIMIT}$	Current limit	$V_{IN} = V_{IN-Min}$ to $V_{IN-Max}$ , $V_{OUT}/R_{OUT} = 1.2\text{A}$	400	650		mA
$V_{IL}$	EN Input Logic Low Voltage	$V_{IN} = V_{IN-Min}$ to $V_{IN-Max}$			0.4	V
$V_{IH}$	EN Input Logic High Voltage	$V_{IN} = V_{IN-Min}$ to $V_{IN-Max}$	1.4			V
$I_{EN}$	EN Input Current	$V_{IN} = 0\text{V}$ or $V_{IN-Max}$	-1		1	$\mu\text{A}$
$T_{SHDN}$	Thermal shutdown threshold			145		$^\circ\text{C}$
$T_{HYS}$	Thermal shutdown hysteresis			15		$^\circ\text{C}$
$\theta_{JA}$	Thermal Resistance Junction-to-Ambient	SOT25 (Note 5)		187		$^\circ\text{C}/\text{W}$
		DFN2020-6 (Note 5)		251		

Notes: 4. Dropout voltage is the voltage difference between the input and the output at which the output voltage drops 1% below its nominal value.  
5. Test condition for all packages: Device mounted on FR-4 substrate PC board, 1oz copper, with minimum recommended pad layout.

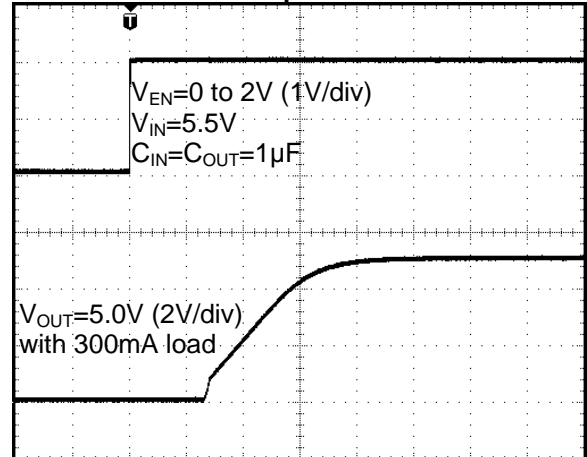
**Typical Performance Characteristics**

**Start-Up Time**



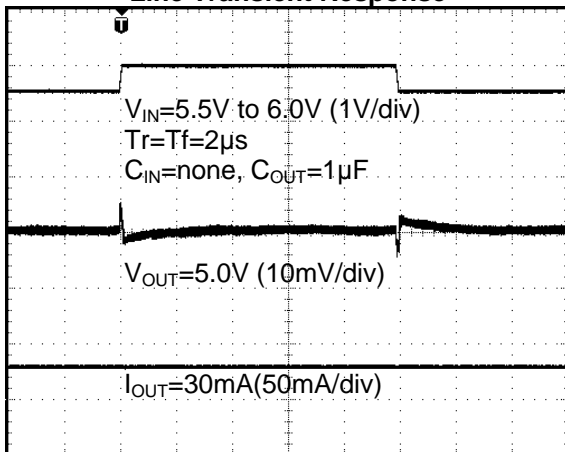
Time (40µs/div)

**Start-Up Time**



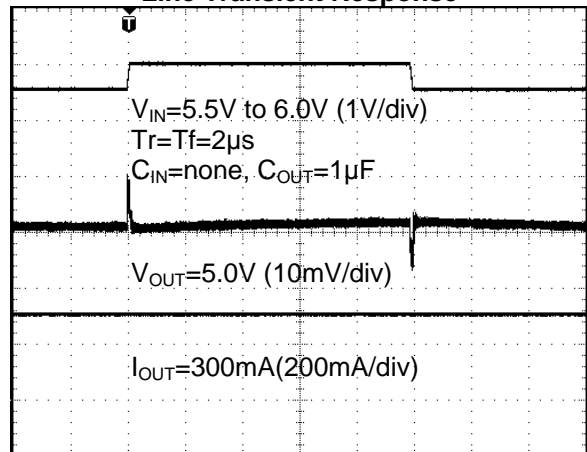
Time (40µs/div)

**Line Transient Response**



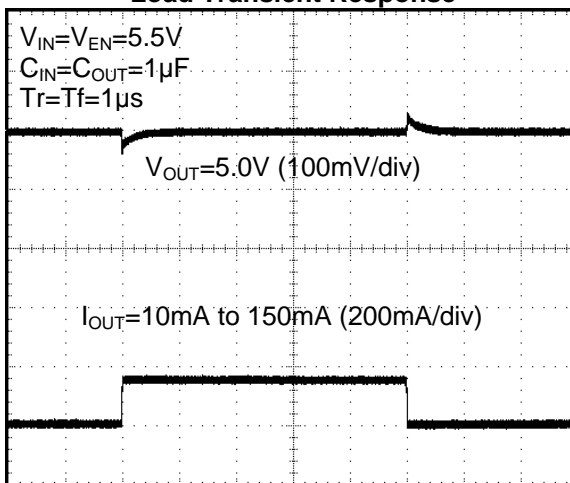
Time (40µs/div)

**Line Transient Response**



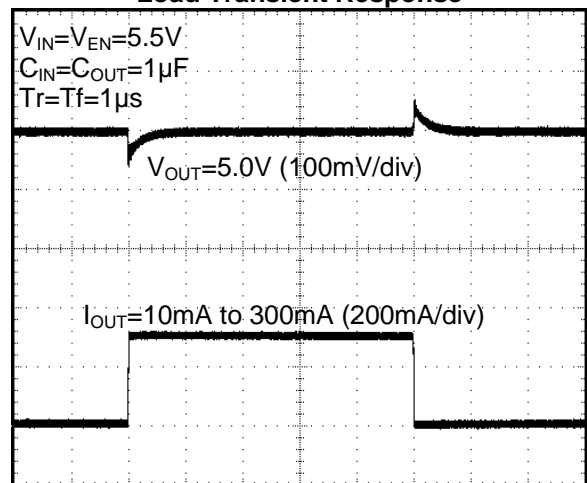
Time (40µs/div)

**Load Transient Response**



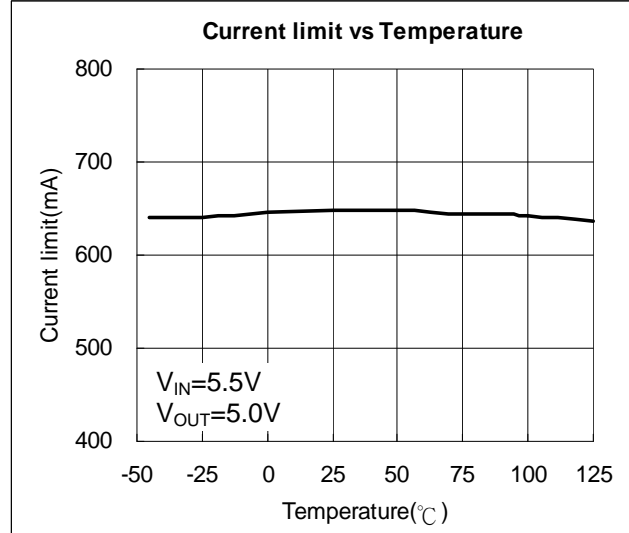
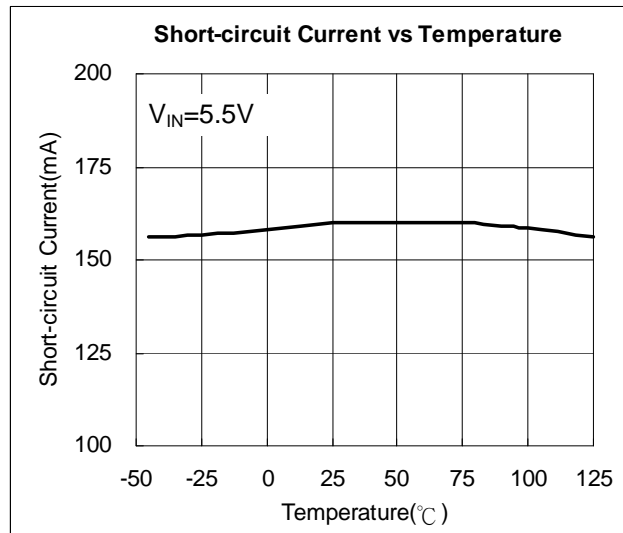
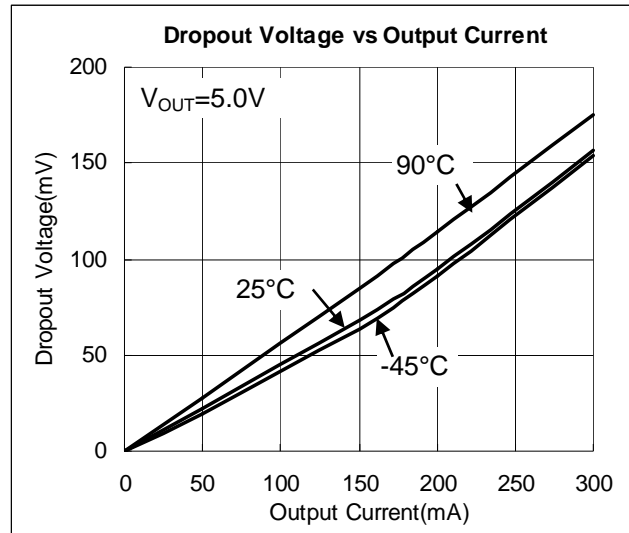
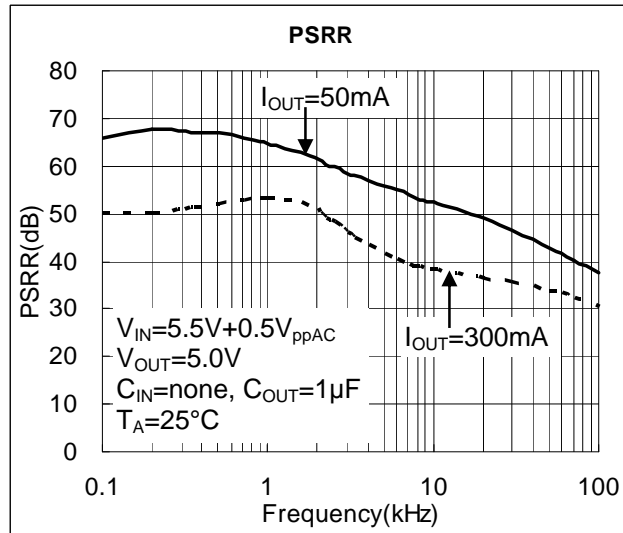
Time (100µs/div)

**Load Transient Response**



Time (100µs/div)

**Typical Performance Characteristics (cont.)**



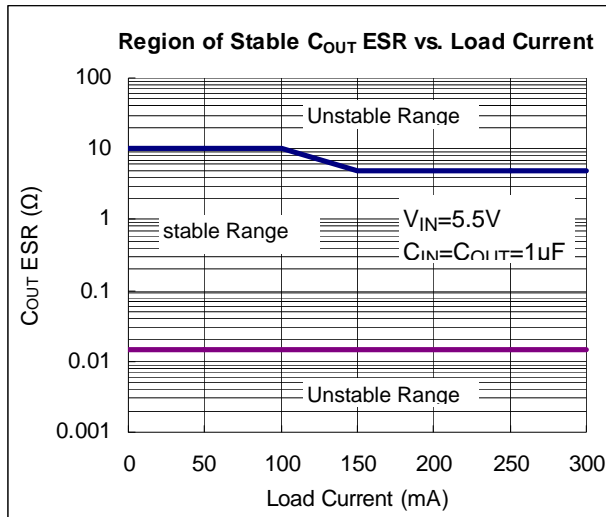
**Application Note**

**Input Capacitor**

A 1 $\mu$ F ceramic capacitor is recommended between IN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and reduce noise. For PCB layout, a wide copper trace is required for both IN and GND pins. A lower ESR capacitor type allows the use of less capacitance, while higher ESR type requires more capacitance.

**Output Capacitor**

The output capacitor is required to stabilize and improve the transient response of the LDO. The AP7335A is stable with very small ceramic output capacitors. Using a ceramic capacitor value that is at least 1 $\mu$ F with ESR > 15m $\Omega$  on the output ensures stability. Higher capacitance values help to improve line and load transient response. The output capacitance may be increased to keep low undershoot and overshoot. Output capacitor must be placed as close as possible to OUT and GND pins.



**No Load Stability**

No minimum load is required to keep the device stable. The device will remain stable and regulated in no load condition.

**ON/OFF Input Operation**

The AP7335A is turned on by setting the EN pin high, and is turned off by pulling it low. If this feature is not used, the EN pin should be tied to IN pin to keep the regulator output on at all time. To ensure proper operation, the signal source used to drive the EN pin must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under  $V_{IL}$  and  $V_{IH}$ .

**Current Limit Protection**

When output current at OUT pin is higher than current limit threshold, the current limit protection will be triggered and clamp the output current to approximately 650mA to prevent over-current and to protect the regulator from damage due to overheating.

**Short Circuit Protection**

When OUT pin is short-circuit to GND, short circuit protection will be triggered and clamp the output current to approximately 160mA. This feature protects the regulator from over-current and damage due to overheating.

**Thermal Shutdown Protection**

Thermal protection disables the output when the junction temperature rises to approximately +145°C, allowing the device to cool down. When the junction temperature reduces to approximately +130°C the output circuitry is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the heat dissipation of the regulator, protecting it from damage due to overheating.

**Ultra Fast Start-up**

After enabled, the AP7335A is able to provide full power in as little as tens of microseconds, typically 220 $\mu$ s, without sacrificing low ground current. This feature will help load circuitry move in and out of standby mode in real time, eventually extend battery life for mobile phones and other portable devices.

**Fast Transient Response**

Fast transient response LDO can extend battery life. TDMA-based cell phone protocols such as Global System for Mobile Communications (GSM) have a transmit/receive duty factor of only 12.5 percent, enabling power savings by putting much of the baseband circuitry into standby mode in between transmit cycles. In baseband circuits, the load often transitions virtually instantaneously from 100 $\mu$ A to 100mA. To meet this load requirement, the LDO must react very quickly without a large voltage drop or overshoot — a requirement that cannot be met with conventional, general-purpose LDO.

The AP7335A's fast transient response from 0 to 300mA provides stable voltage supply for fast DSP and GSM chipset with fast changing load.

**Low Quiescent Current**

The AP7335A, consuming only around 35 $\mu$ A for all input range, provides great power saving in portable and low power applications.

**Application Note (cont.)**

**Power Dissipation**

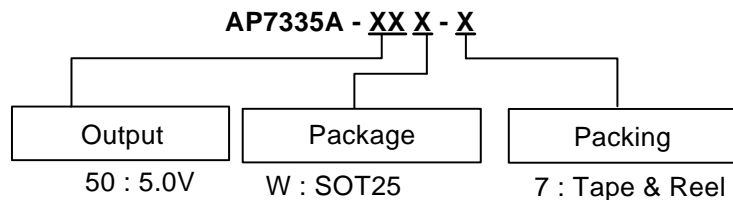
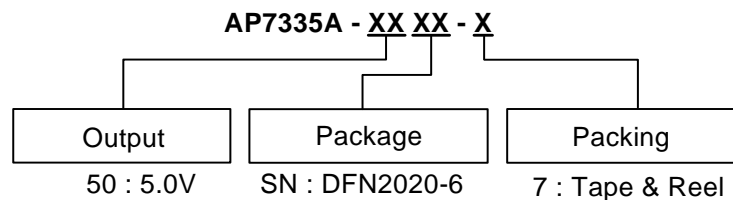
The device power dissipation and proper sizing of the thermal plane that is connected to the thermal pad is critical to avoid thermal shutdown and ensure reliable operation. Power dissipation of the device depends on input voltage and load conditions and can be calculated by:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

The maximum power dissipation, handled by the device, depends on the maximum junction to ambient thermal resistance, maximum ambient temperature, and maximum device junction temperature, which can be calculated by the following equation:

$$P_D (\text{max}@T_A) = \frac{(+145^\circ\text{C} - T_A)}{R_{\theta JA}}$$

**Ordering Information**



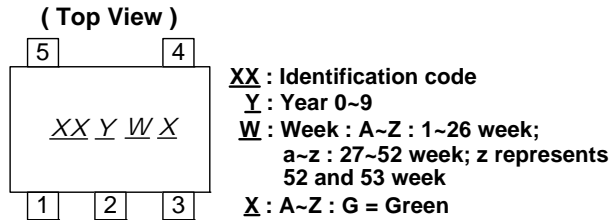
Device	Package Code	Packaging (Note 6)	7"/13" Tape and Reel	
			Quantity	Part Number Suffix
AP7335A-XXW-7	W	SOT25	3000/Tape & Reel	-7
AP7335A-XXSN-7	SN	DFN2020-6	3000/Tape & Reel	-7

Note: 6. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at <http://www.diodes.com/datasheets/ap02001.pdf>.



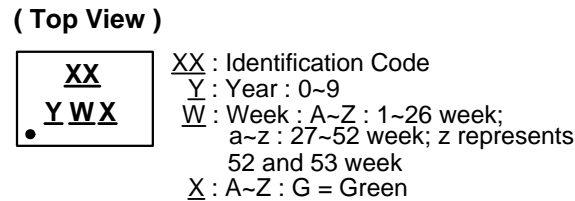
**Marking Information**

**(1) SOT25**



Device	Package	Identification Code
AP7335A-50	SOT25	TP

**(2) DFN2020-6**

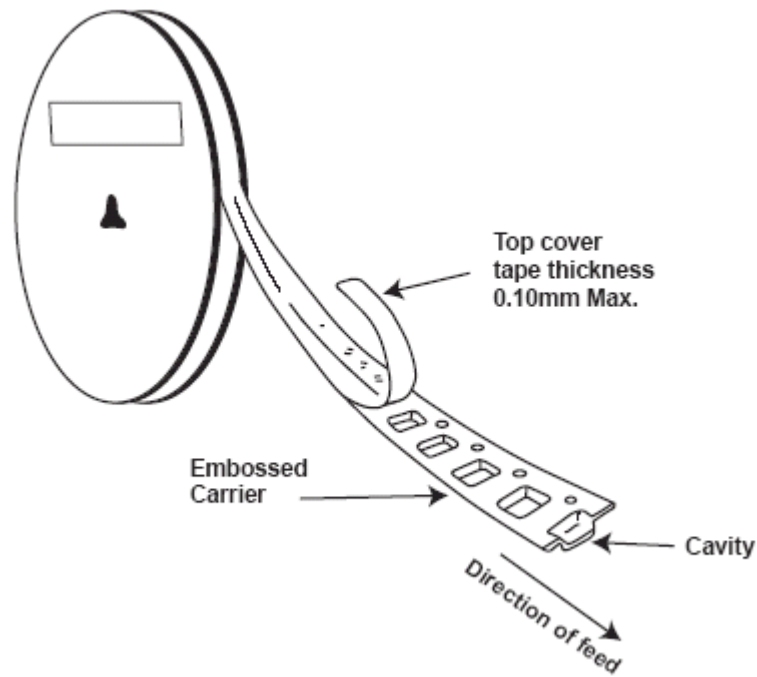
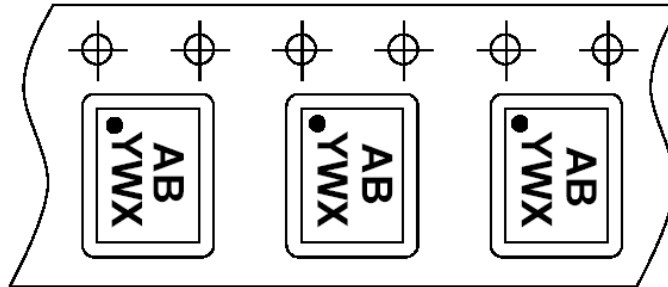


Device	Package	Identification Code
AP7335A-50	DFN2020-6	TP



**Taping Orientation (Note 7)**

For DFN2020-6



Note: 7. The taping orientation of the other package type can be found on our website at <http://www.diodes.com/datasheets/ap02007.pdf>.

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