

## Dual Channel 500mA/500mA Regulator + Reset IC

### Features

- Low Quiescent Current : 110µA (No load)
- Low Dropout Voltage :  
 $V_{DRO P1}=500mV@500mA$   
 $V_{DRO P2}=500mV@500mA$
- Fixed Output Voltage :  
 $V_{OUT1}=3.3V/500mA$   
 $V_{OUT2}=3.3V/500mA$
- Stable with 4.7µF Output Capacitor
- Stable with Aluminum, Tantalum or Ceramic Capacitors
- Built in Thermal Protection
- Fast Transient Response
- Short Setting Time
- SOP-8, SOP-8-P with Thermal Pad Packages
- Adjustment-free Reset Detection Voltage :  
 3.9V or 4.2V typ
- Easy to Set Delay Time from Voltage Detection to Reset Release

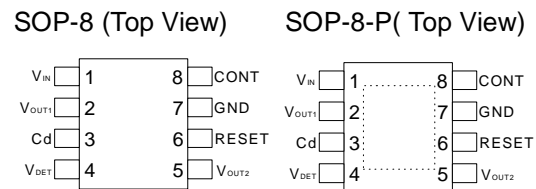
### Applications

- Optical Storage System

### General Description

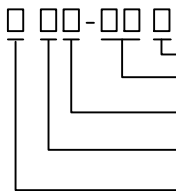
The APL5546 is a dual-channel regulator with reset function (specific voltage monitoring), and internal delay circuit, set to detect 3.9V or 4.2V. Maximum input voltage is 6V, and both output1 and output2 can deliver up to 500mA. The typical dropout voltage of both channel is 500mV at 500mA loading. Design with an internal P-channel MOSFET pass transistor, the APL5546 maintains a low supply current. Other features include, thermal-shutdown protection, current limit protection to ensure specified output current. The APL5546 come in miniature SOP-8 and SOP-8-P packages.

### Pin Configuration



= Thermal Pad  
 (connected to GND plane for better heat dissipation)

### Ordering and Marking Information

|   |  |
|---|--|
| <p>APL5546 - </p>  | <p>Package Code<br/>                 K : SOP-8    KA : SOP-8-P<br/>                 Temp. Range<br/>                 C : 0 to 70°C    I : -40 to 85°C<br/>                 Handling Code<br/>                 TR : Tape &amp; Reel<br/>                 Detection Voltage :<br/>                 A : 3.9V    B : 4.2V<br/>                 Lead Free Code<br/>                 L : Lead Free Device<br/>                 Blank : Original Device</p> |
| <p>APL5546 K / KA: <span style="border: 1px solid black; padding: 2px;">APL5546X<br/>XXXXX</span></p> | <p>X        - Detection Voltage<br/>                 XXXXX - Date Code</p>   |

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## Pin Description

| PIN |                   | I/O | Description  |
|-----|-------------------|-----|--|
| No. | Name              |     |  |
| 1   | V <sub>IN</sub>   | O   | Voltage supply input pin.  |
| 2   | V <sub>OUT1</sub> | O   | Regulator output pin.  |
| 3   | Cd                |     | Delay time capacitor pin, RESET pin output delay time can be set by the capacitor connected to the Cd pin. $t_{PLH} = 130000 * C$ , $t_{PLH}$ : transmission delay time (s), C:capacitor value (F) |
| 4   | V <sub>DET</sub>  | I   | Input pin of voltage detection.  |
| 5   | V <sub>OUT2</sub> | O   | Regulator output pin.  |
| 6   | RESET             | O   | Input voltage detection output pin , high = $V_{DET} < V_S$ , low = $V_{DET} > V_S$  |
| 7   | GND               |     | GND pin  |
| 8   | CONT              | I   | V <sub>OUT1</sub> on/off-control pin, V <sub>OUT1</sub> will be turn off when CONT pull to low.  |

## Absolute Maximum Ratings

| Symbol                             | Parameter                                | Rating             | Unit |
|------------------------------------|--|--------------------|------|
| V <sub>IN</sub> , V <sub>OUT</sub> | Input Voltage or Out Voltage             | 6.5                | V    |
| CONT                               | V <sub>OUT1</sub> Shutdown Control Pin   | 6.5                | V    |
| V <sub>DET</sub>                   | RESET Pin Supply Voltage                 | 6.5                | V    |
| R <sub>TH,JA</sub>                 | Thermal Resistance – Junction to Ambient |                    |      |
|                                    | SOP-8                                    | 150                | °C/W |
|                                    | SOP-8-P                                  | 80                 |      |
| R <sub>TH,JC</sub>                 | Thermal Resistance – Junction to Case    |                    |      |
|                                    | SOP-8                                    | 30                 | °C/W |
|                                    | SOP-8-P                                  | 5                  |      |
| P <sub>D</sub>                     | Power Dissipation                        | Internally Limited | W    |
| T <sub>J</sub>                     | Operating Junction Temperature           |                    |      |
|                                    | Control Section                          | 0 to 125           | °C   |
|                                    | Power Transistor                         | 0 to 170           |      |
| T <sub>STG</sub>                   | Storage Temperature Range                | -65 to +150        | °C   |
| T <sub>L</sub>                     | Lead Temperature (Soldering, 10 second)  | 260                | °C   |

## Electrical Characteristics

Unless otherwise noted these specifications apply over full temperature ,  $V_{IN}=5V$ ,  $C_{IN}=1\mu F$ ,  $C_{OUT1}=4.7\mu F$ ,  $C_{OUT2}=4.7\mu F$ ,  $CONT=V_{IN}$ ,  $T_J=0$  to  $125^\circ C$  . Typical values refer to  $T_J=25^\circ C$  .

| Symbol            | Parameter   | Test Conditions                                 | APL5546 |      |              | Unit            |
|-------------------|---|---|---------|------|--------------|-----------------|
|                   |   |   | Min.    | Typ. | Max.         |                 |
| $V_{IN}$          | Input Voltage   |   |         |      | 6            | V               |
| $I_Q$             | Quiescent Current   | $I_{OUT1}=0mA$ , $I_{OUT2}=0mA$                 |         | 100  |              | $\mu A$         |
|                   | Shutdown Supply Current   | $CONT = low$ ,<br>$I_{OUT2}=0mA$                |         | 70   |              | $\mu A$         |
| $I_{CONT}$        | Shutdown Input Bias current   | $V_{CONT}=V_{IN}$                               |         |      | 0.1          | $\mu A$         |
| $V_{CONT}$        | High Threshold Voltage  |   | 1.6     |      | $V_{IN}+0.3$ | V               |
|                   | Low Threshold Voltage   |   | -0.3    |      | 0.4          |                 |
| $I_{CCQ}$         | $V_{DET}$ Input Current   | $V_{DET}=5V$                                    |         | 20   | 40           | $\mu A$         |
| <b>Regulator1</b> |   |   |         |      |              |                 |
| $V_{OUT1}$        | Output Voltage  | $V_{IN}=5V$                                     | 3.234   | 3.3  | 3.366        | V               |
| $I_{LIMIT}$       | Circuit Current Limit   | $V_{IN}=5V$                                     |         | 800  |              | mA              |
| $I_{OUT}$         | Load Current  |   | 500     |      |              | mA              |
| $REG_{LINE}$      | Line Regulation   | $V_{OUT}+0.5V < V_{IN} < 6.0V$ , $I_{OUT}=10mA$ |         | 4    | 6            | mV              |
| $REG_{LOAD}$      | Load Regulation   | $V_{IN}=5V$ , $0mA < I_{OUT} < I_{MAX}$         |         | 25   | 60           | mV              |
| $V_{DROP}$        | Dropout Voltage <sup>(Note)</sup><br>( $V_{OUT}(\text{Nominal})=3.3V$<br>Version) | $I_{OUT}=500mA$                                 |         | 500  | 650          | mV              |
| PSRR              | Ripple Rejection  | $F \leq 1kHz$ , $1V_{pp}$ at $I_{OUT}=50mA$     | 45      | 55   |              | dB              |
| OTS               | Over Temperature Shutdown   |   |         | 170  |              | $^\circ C$      |
|                   | Over Temperature Shutdown Hysteresis  | Hysteresis                                      |         | 15   |              | $^\circ C$      |
| TC                | Output Voltage Temperature Coefficient  | $T_A = -20 \sim 80^\circ C$                     |         | 100  |              | ppm/ $^\circ C$ |
| $C_{OUT}$         | Output Capacitor  |   |         | 4.7  |              | $\mu F$         |
|                   | ESR   |   | 0.01    |      | 1            | Ohm             |
| <b>Regulator2</b> |   |   |         |      |              |                 |
| $V_{OUT2}$        | Output Voltage  | $V_{IN}=5V$                                     | 3.234   | 3.3  | 3.366        | V               |
| $I_{LIMIT}$       | Circuit Current Limit   | $V_{IN}=5V$                                     |         | 800  |              | mA              |
| $I_{OUT}$         | Load Current  |   | 500     |      |              | mA              |
| $REG_{LINE}$      | Line Regulation   | $V_{OUT}+0.5V < V_{IN} < 6.0V$ , $I_{OUT}=10mA$ |         | 4    | 6            | mV              |
| $REG_{LOAD}$      | Load Regulation   | $V_{IN}=5V$ , $0mA < I_{OUT} < I_{MAX}$         |         | 25   | 60           | mV              |
| $V_{DROP}$        | Dropout Voltage <sup>(Note)</sup><br>( $V_{OUT}(\text{Nominal})=3.3V$<br>Version) | $I_{OUT}=500mA$                                 |         | 500  | 650          | mV              |

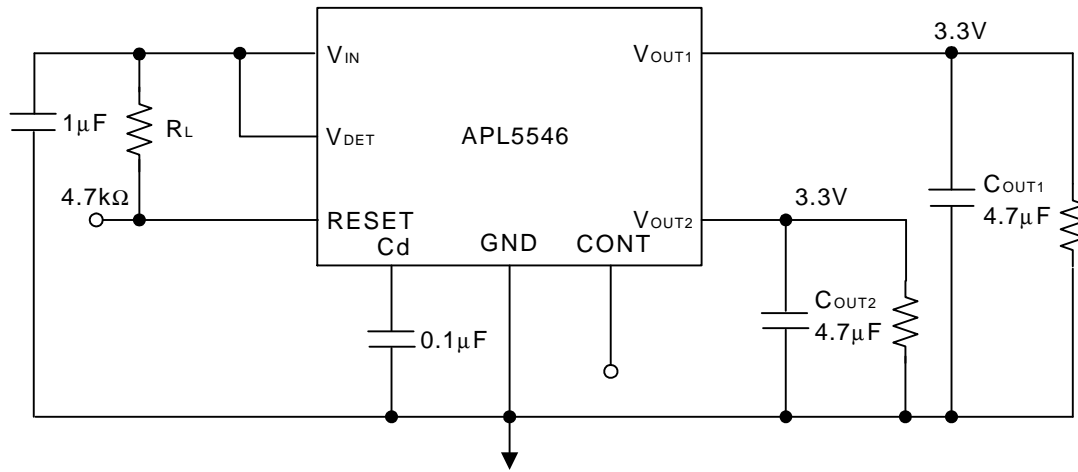
Note : Dropout voltage definition :  $V_{IN} - V_{OUT}$  when  $V_{OUT}$  is 2% below the value of  $V_{OUT}$  for  $V_{IN}=5V$

## Electrical Characteristics (Cont.)

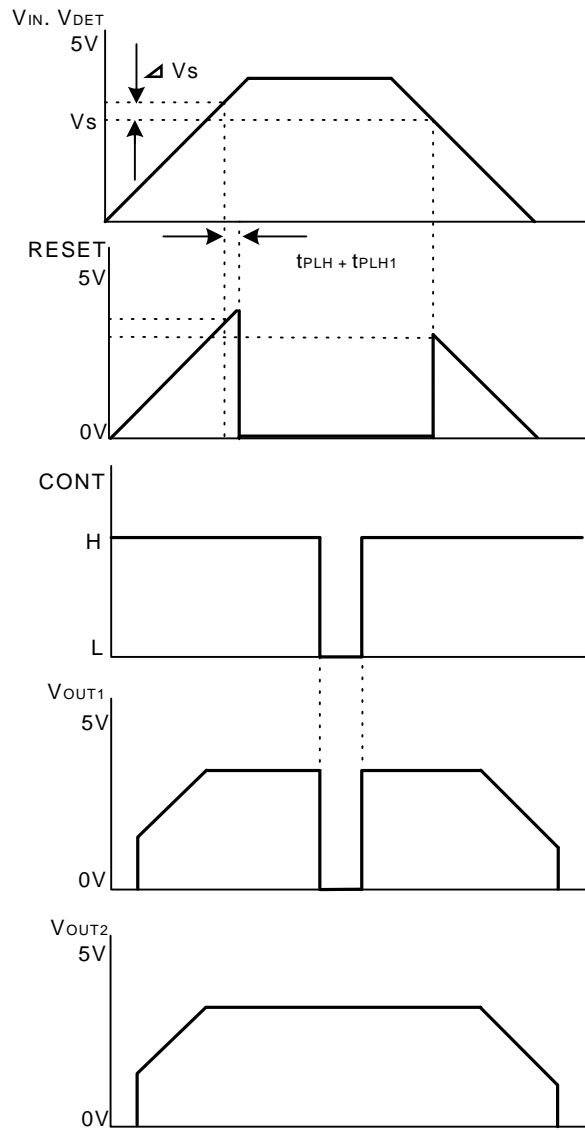
Unless otherwise noted these specifications apply over full temperature ,  $V_{IN}=5V$ ,  $C_{IN}=1\mu F$ ,  $C_{OUT1}=4.7\mu F$ ,  $C_{OUT2}=4.7\mu F$ ,  $CONT=V_{IN}$ ,  $T_J=0$  to  $125^\circ C$  . Typical values refer to  $T_J=25^\circ C$  .

| Symbol        | Parameter                              | Test Conditions   | APL5546 |      |      | Unit            |
|---------------|--|---|---------|------|------|-----------------|
|               |  |   | Min.    | Typ. | Max. |                 |
| Regulator2    |  |   |         |      |      |                 |
| PSRR          | Ripple Rejection                       | $F \leq 1kHz$ , $1V_{pp}$ at $I_{OUT}=50mA$                           | 45      | 55   |      | dB              |
| OTS           | Over Temperature Shutdown              |   |         | 170  |      | $^\circ C$      |
|               | Over Temperature Shutdown Hysteresis   | Hysteresis  |         | 15   |      | $^\circ C$      |
| TC            | Output Voltage Temperature Coefficient | $T_a = -20 \sim 80^\circ C$   |         | 100  |      | ppm/ $^\circ C$ |
| $C_{OUT}$     | Output Capacitor                       |   |         | 4.7  |      | $\mu F$         |
|               | ESR                                    |   | 0.01    |      | 1    | Ohm             |
| RESET / RESET |  |   |         |      |      |                 |
| VS            | Detection Voltage                      | $V_{DET}=H \rightarrow L$ (APL5546A)                                  |         | 3.9  |      | V               |
|               |  | $V_{DET}=H \rightarrow L$ (APL5546B)                                  |         | 4.2  |      | V               |
| VS/ T         | Vs Temperature Coefficient             | $T_A = A -20 \sim +80^\circ C$  |         | 100  |      | ppm/ $^\circ C$ |
| VS            | Hysteresis Voltage                     | $V_{DET} = H \rightarrow L$   | 130     | 180  | 230  | mV              |
| $V_{OL}$      | Low-level Output Voltage               | $V_{DET} = 3.9V$ , $R_L = 4.7k\Omega$                                 |         | 22   | 60   | mV              |
| $I_{OH}$      | Output Leakage Current                 | $V_{DET} = 5V$  |         | 0.5  | 1    | $\mu A$         |
| $I_{OL1}$     | Output Current1                        | $V_{DET} = 3.9V$ , $V_{RESET} = 0.4V$                                 | 10      | 14   |      | mA              |
| $I_{OL2}$     | Output Current2                        | $V_{DET} = 3.9V$ , $V_{RESET} = 0.4V$<br>$T_A = -20 \sim +80^\circ C$ | 8       | 14   |      | mA              |
| tPLH          | “H” Transmission Delay Time            | $C_d = 0\mu F$  |         | 42   | 90   | $\mu s$         |
| tPLH1         | Reset Delay Time                       | $V_{DET} = 3.7V \rightarrow 5V$ , $C_d = 0.1\mu F$                    | 8       | 13   | 18   | ms              |
| tPHL          | “L” Transmission Delay Time            | $C_d = 0\mu F$  |         | 4    | 90   | $\mu s$         |
| $V_{OPL}$     | Threshold Operating Voltage            | $V_{RESET} = 0.4V$  |         | 0.95 | 1.25 | V               |

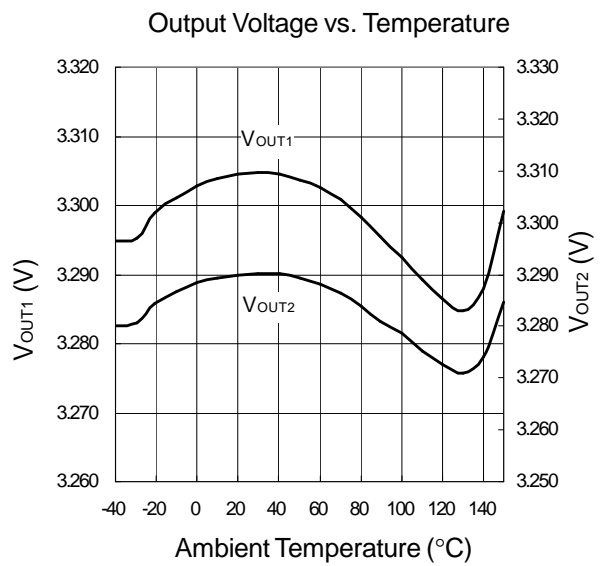
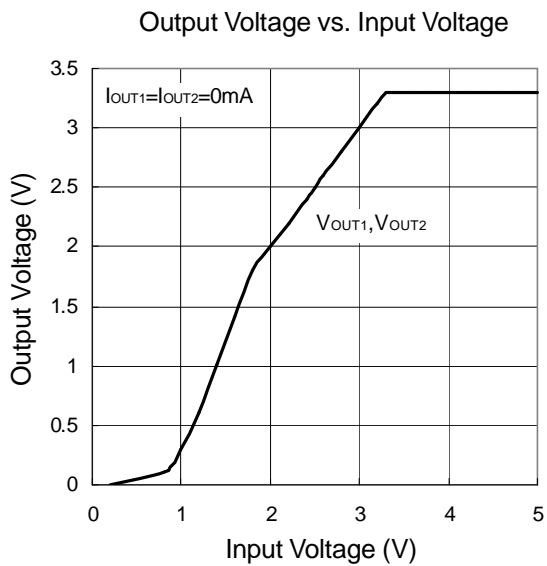
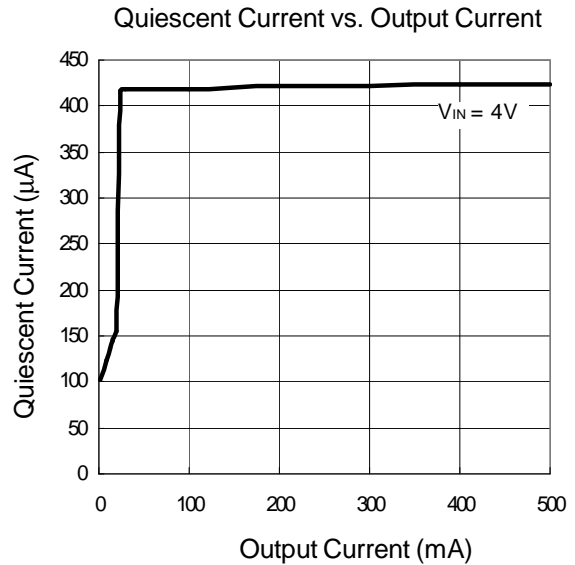
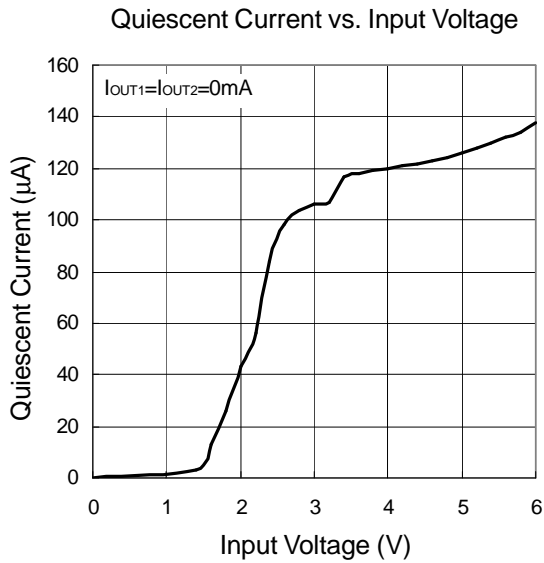
Application Circuit



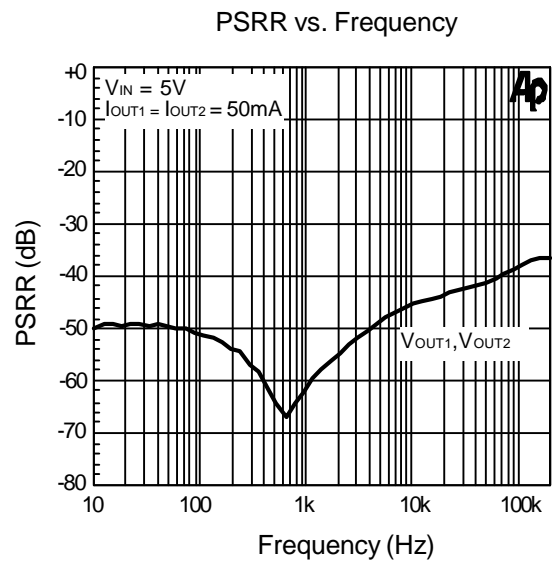
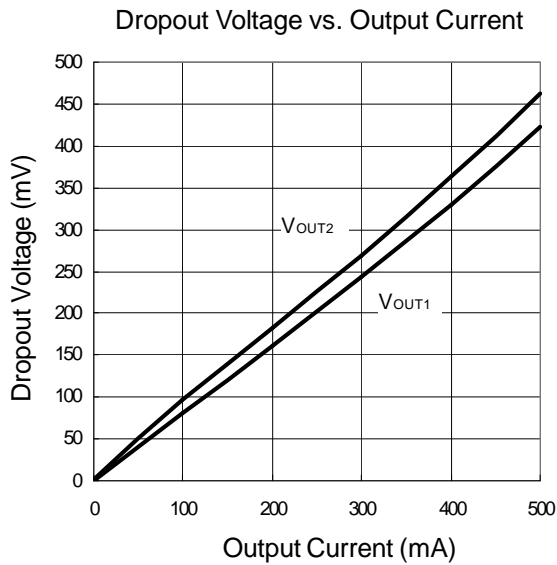
Timing Chart



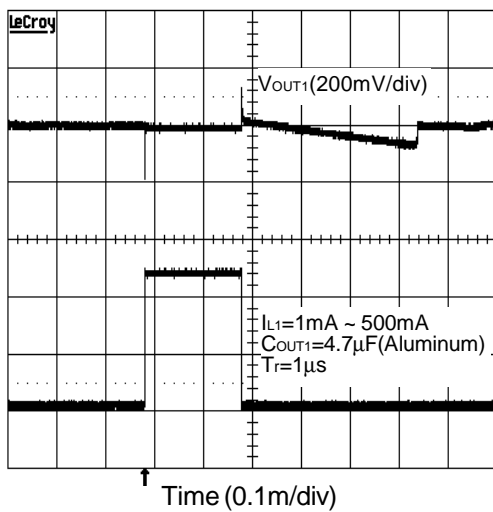
## Typical Characteristics



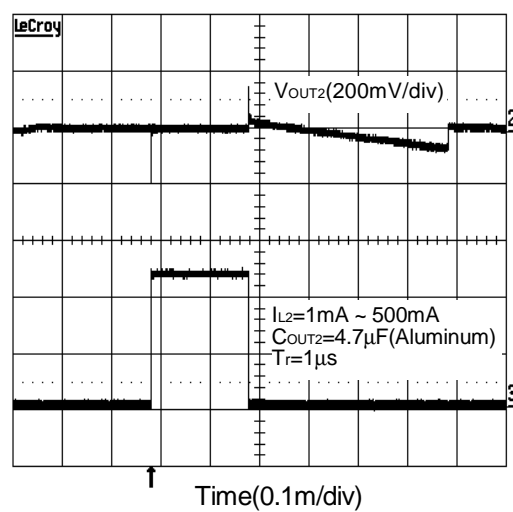
## Typical Characteristics



Load-Transient Response



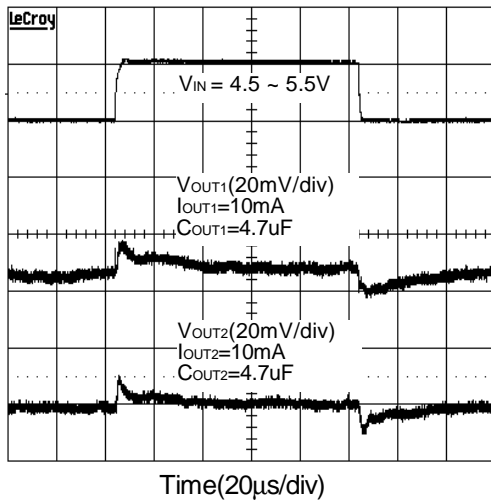
Load-Transient Response



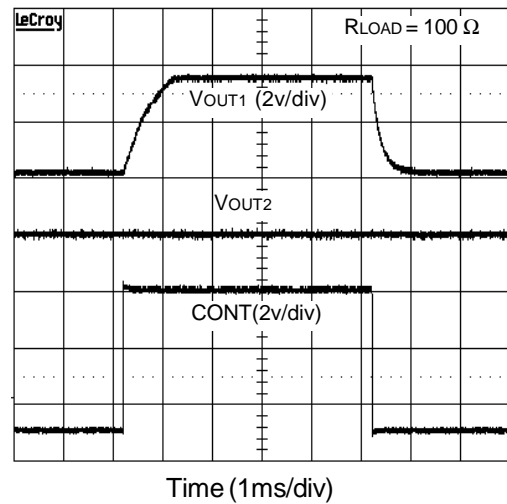


## Typical Characteristics

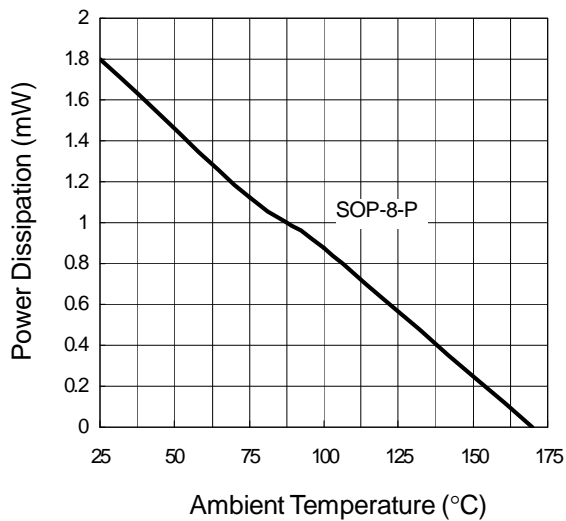
Line-Transient Response



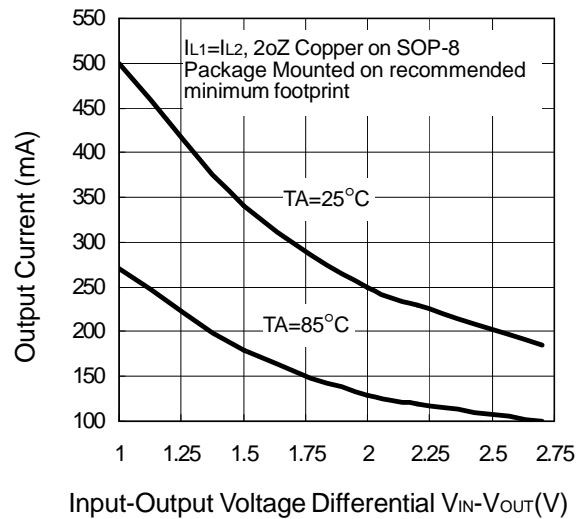
Shutdown Response



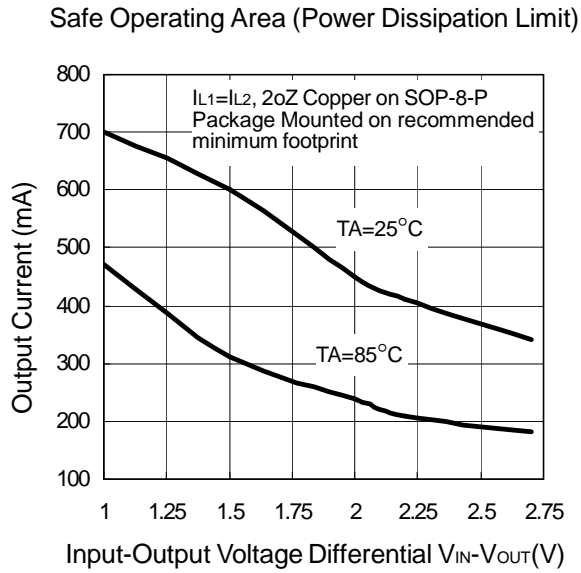
Power Dissipation vs. Ambient Temperature



Safe Operating Area (Power Dissipation Limit)



## Typical Characteristics



## Application Information

### Capacitor Selection and Regulator Stability

The APL5546 uses at least a 1 $\mu$ F capacitor on the input. This capacitor can use Aluminum, Tantalum or Ceramic capacitors. Input capacitor with large value and low ESR provides better PSRR and line-transient response. The output capacitor also can use Aluminum, Tantalum or Ceramic capacitors, and its minimum values is recommended 4.7 $\mu$ F, ESR must be above 0.01 $\Omega$ . Large output capacitor values can reduce noise and improve load-transient response, stability, and PSRR. Note that some ceramic dielectrics exhibit large capacitance and ESR variation with Temperature. If use this capacitor, it may be necessary to use 4.7 $\mu$ F or more to ensure stability at temperature below -10°C.

### Load-Transient Considerations

The APL5546 load-transient response graphs in Typical Characteristics show the transient response. A step change in the load current from 1mA to 500mA at 1 $\mu$  second will cause less than 200mV transient spike. Large output capacitor's value and low ESR can reduce transient spike.

### Shutdown/Enable

The APL5546 has an active high enable function. Force CONT high (>1.6V) enables the  $V_{OUT1}$ , CONT low (<0.4V) disables the  $V_{OUT1}$  and  $V_{OUT2}$  can not be affected by CONT. Enter the shutdown mode, it also causes the output voltage to discharge through a 500  $\Omega$  resistance to ground. In shutdown mode, the quiescent current can reduce to 70 $\mu$ A. The CONT pin cannot be floating, a floating CONT pin may cause an indeterminate state on the output. If it is no use, connect to  $V_{IN}$  for normal operation.

### RESET

The RESET pin is asserted whenever  $V_{DET}$  falls below the reset threshold voltage or if CONT is forced low at some special IC (refer timing chart and pin description). The reset function ensures the microprocessor is properly reset and powers up into a known condition after a power failure. RESET will remain valid with  $V_{IN}$  as low as 0.95V. The RESET output is a simple open-drain N channel MOSFET structure. A pull-up resistor must be used to pull this output up to some voltage. For most application, this voltage will be the same power supply that supplies  $V_{IN}$  to the APL5546. The APL5546 is relatively immune to negative-going glitches below the reset threshold. Typically reset delay time is 13ms while using 0.1 $\mu$ F at Cd pin. If more transient immunity is needed, a Cd capacitor can be placed as larger as possible.

### Input-Output (Dropout) Voltage

The minimum input-output voltage differential (dropout) determines the lowest usable supply voltage. The dropout voltage is a function of drain-to-source on resistance multiplied by the load current.

### Current Limit

APL5546 includes two separate current-limit circuitry for each linear regulator. The current limit protection, which sense the current flows the P-channel MOSFET, and controls the output voltage. The point where limiting occurs is  $I_{OUT}=800$ mA. The output can be shorted to ground for an indefinite amount of time without damaging to the part.

## Application Information

### Thermal Protection

Thermal protection limits total power dissipation in the APL5546. When the junction temperature exceeds  $T_J=+170^{\circ}\text{C}$ , the thermal sensor generate a logic signal to turn off the pass transistor and let IC to cool. When the IC's junction temperature cools by  $15^{\circ}\text{C}$ , the thermal sensor will turn the pass transistor on again, resulting in a pulsed output during continuous thermal protection. Thermal protection is designed to protect the IC in the event of fault conditions. For continual operation, do not exceed the absolute maximum junction temperature rating of  $T_J=+180^{\circ}\text{C}$ .

### Operating Region and Power Dissipation

The thermal resistance of the case and circuit board, ambient and junction air temperature, and the rate of air flow all control the APL5546 maximum power dissipation. The power dissipation across the device is  $P = I_{OUT}(V_{IN}-V_{OUT})$ . The maximum power dissipation is:

$$P_{MAX} = (T_J - T_A) / (\theta_{JB} + \theta_{BA})$$

where  $T_J - T_A$  is the temperature difference between the junction and ambient air.

$\theta_{JB}$  is the thermal resistance of the package,  $\theta_{BA}$  is the thermal resistance through the printed circuit board, copper traces, and other materials to the surrounding air. The GND pin provides an electrical connection to ground and channeling heat away. Connect the GND pin to ground using a large pad or ground plane as a heat sink, it can improve maximize thermal dissipation.

See figure 1. The SOP-8-P utilizes a bottom thermal pad to minimize the thermal resistance of the package, making the package suitable for high current applications. The thermal pad is soldered to the top ground pad and is connected to the internal or bottom ground plane by several vias. The printed circuit board (PCB) forms a heat sink and dissipates most of the

heat into ambient air. The vias are recommended to have proper size to retain solder, helping heat conduction.

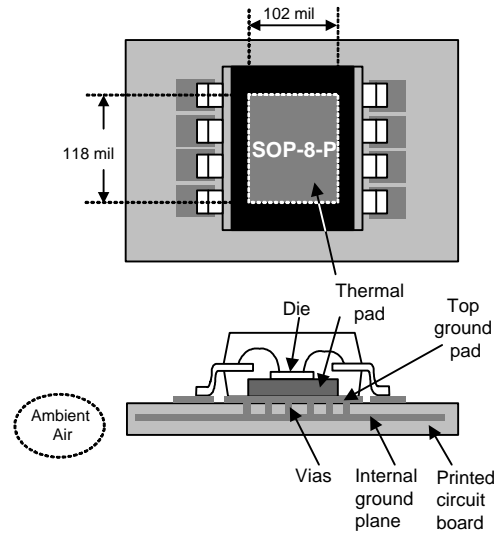
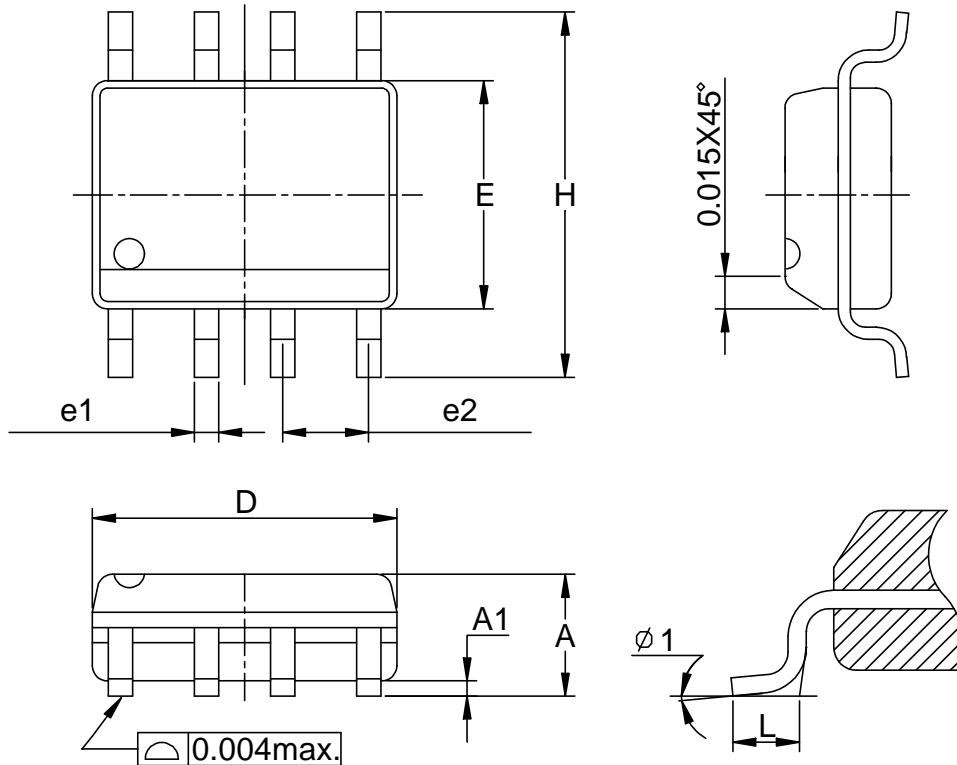


Figure 1

## Packaging Information

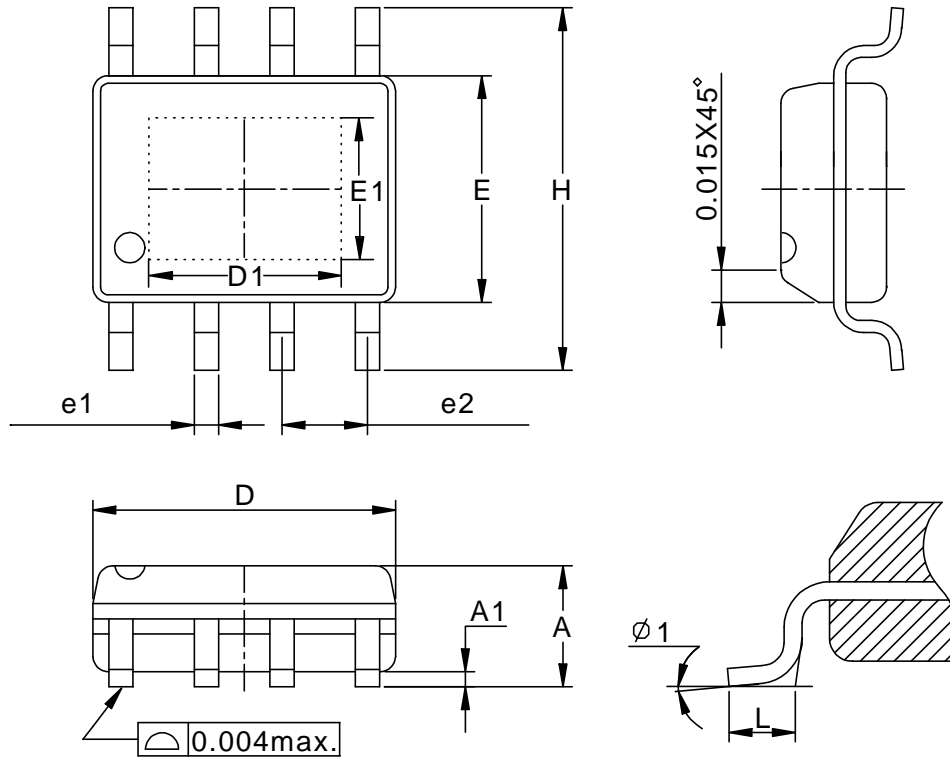
SOP-8 pin ( Reference JEDEC Registration MS-012)



| Dim | Millimeters |      | Inches  |       |
|-----|-------------|------|---------|-------|
|     | Min.        | Max. | Min.    | Max.  |
| A   | 1.35        | 1.75 | 0.053   | 0.069 |
| A1  | 0.10        | 0.25 | 0.004   | 0.010 |
| D   | 4.80        | 5.00 | 0.189   | 0.197 |
| E   | 3.80        | 4.00 | 0.150   | 0.157 |
| H   | 5.80        | 6.20 | 0.228   | 0.244 |
| L   | 0.40        | 1.27 | 0.016   | 0.050 |
| e1  | 0.33        | 0.51 | 0.013   | 0.020 |
| e2  | 1.27BSC     |      | 0.50BSC |       |
| φ 1 | 8°          |      | 8°      |       |

## Packaging Information

SOP-8-P pin ( Reference JEDEC Registration MS-012)

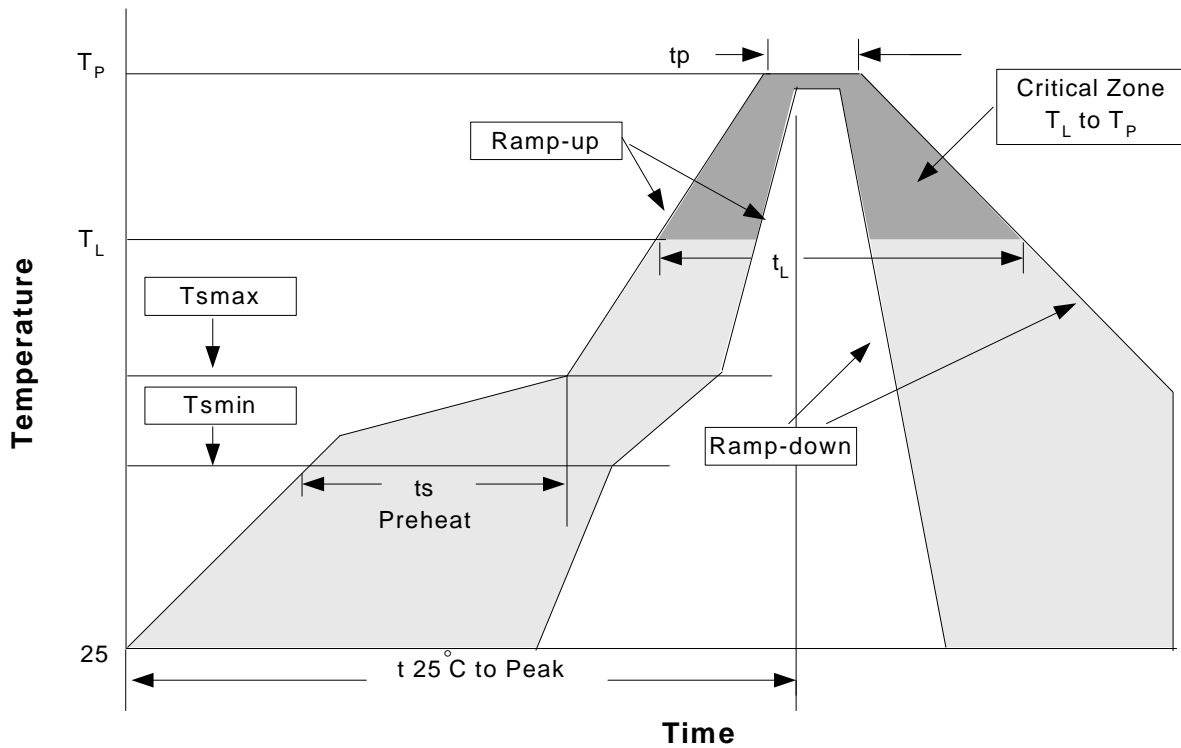


| Dim | Millimeters |      | Inches   |       |
|-----|-------------|------|----------|-------|
|     | Min.        | Max. | Min.     | Max.  |
| A   | 1.35        | 1.75 | 0.053    | 0.069 |
| A1  | 0           | 0.15 | 0        | 0.006 |
| D   | 4.80        | 5.00 | 0.189    | 0.197 |
| D1  | 3.00REF     |      | 0.118REF |       |
| E   | 3.80        | 4.00 | 0.150    | 0.157 |
| E1  | 2.60REF     |      | 0.102REF |       |
| H   | 5.80        | 6.20 | 0.228    | 0.244 |
| L   | 0.40        | 1.27 | 0.016    | 0.050 |
| e1  | 0.33        | 0.51 | 0.013    | 0.020 |
| e2  | 1.27BSC     |      | 0.50BSC  |       |
| φ 1 | 8°          |      | 8°       |       |

## Physical Specifications

|                    |  |
|--------------------|--|
| Terminal Material  | Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb), 100%Sn |
| Lead Solderability | Meets EIA Specification RS186-91, ANSI/J-STD-002 Category 3.         |

### Reflow Condition (IR/Convection or VPR Reflow)



### Classification Reflow Profiles

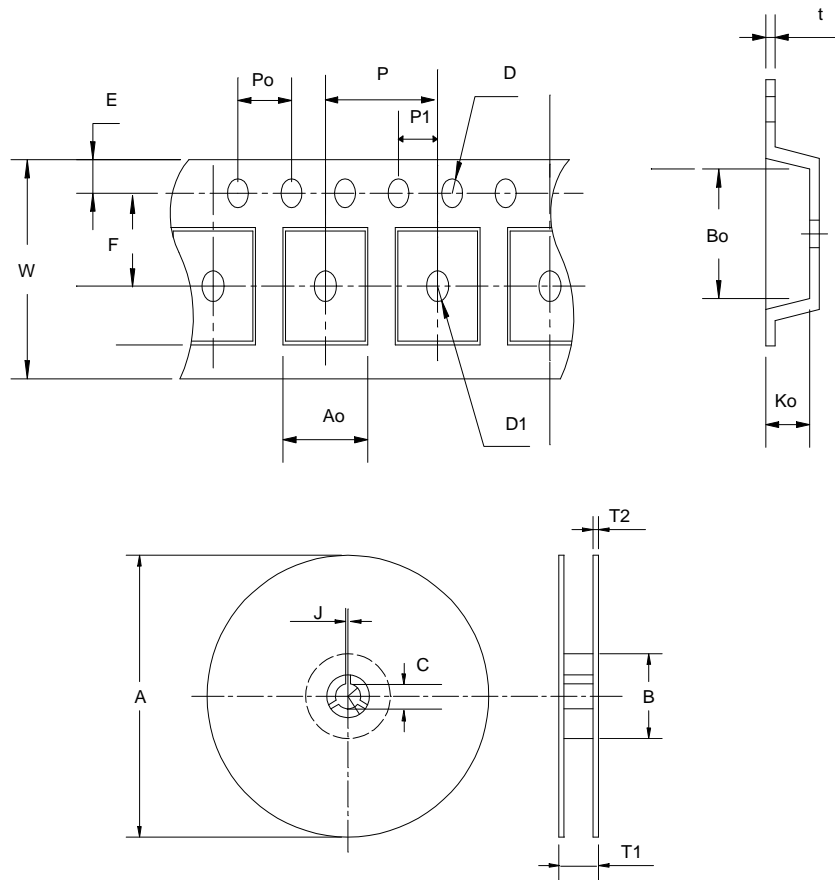
| Profile Feature                                     | Sn-Pb Eutectic Assembly |               | Pb-Free Assembly |               |
|---|-------------------------|---------------|------------------|---------------|
|   | Large Body              | Small Body    | Large Body       | Small Body    |
| Average ramp-up rate ( $T_L$ to $T_P$ )             | 3°C/second max.         |               | 3°C/second max.  |               |
| Preheat   |                         |               |                  |               |
| - Temperature Min ( $T_{smin}$ )                    | 100°C                   |               | 150°C            |               |
| - Temperature Mix ( $T_{smax}$ )                    | 150°C                   |               | 200°C            |               |
| - Time (min to max)( $t_s$ )                        | 60-120 seconds          |               | 60-180 seconds   |               |
| $T_{smax}$ to $T_L$                                 |                         |               |                  |               |
| - Ramp-up Rate                                      |                         |               | 3°C/second max   |               |
| $T_{smax}$ to $T_L$                                 |                         |               |                  |               |
| - Temperature( $T_L$ )                              | 183°C                   |               | 217°C            |               |
| - Time ( $t_L$ )                                    | 60-150 seconds          |               | 60-150 seconds   |               |
| Peak Temperature( $T_p$ )                           | 225 +0/-5°C             | 240 +0/-5°C   | 245 +0/-5°C      | 250 +0/-5°C   |
| Time within 5°C of actual Peak Temperature( $t_p$ ) | 10-30 seconds           | 10-30 seconds | 10-30 seconds    | 20-40 seconds |
| Ramp-down Rate                                      | 6°C/second max.         |               | 6°C/second max.  |               |
| Time 25°C to Peak Temperature                       | 6 minutes max.          |               | 8 minutes max.   |               |

Note: All temperatures refer to top side of the package. Measured on the body surface.

## Reliability test program

| Test item     | Method              | Description                    |
|---------------|---------------------|--------------------------------|
| SOLDERABILITY | MIL-STD-883D-2003   | 245°C , 5 SEC                  |
| HOLT          | MIL-STD-883D-1005.7 | 1000 Hrs Bias @ 125 °C         |
| PCT           | JESD-22-B, A102     | 168 Hrs, 100 % RH , 121°C      |
| TST           | MIL-STD-883D-1011.9 | -65°C ~ 150°C, 200 Cycles      |
| ESD           | MIL-STD-883D-3015.7 | VHBM > 2KV, VMM > 200V         |
| Latch-Up      | JESD 78             | 10ms , I <sub>tr</sub> > 100mA |

## Carrier Tape



| Application | A       | B         | C              | J         | T1         | T2        | W        | P        | E         |
|-------------|---------|-----------|----------------|-----------|------------|-----------|----------|----------|-----------|
| SOP- 8/-P   | 330 ± 1 | 62 +1.5   | 12.75+<br>0.15 | 2 ± 0.5   | 12.4 ± 0.2 | 2 ± 0.2   | 12± 0.3  | 8± 0.1   | 1.75±0.1  |
|             | F       | D         | D1             | Po        | P1         | Ao        | Bo       | Ko       | t         |
|             | 5.5± 1  | 1.55 +0.1 | 1.55+ 0.25     | 4.0 ± 0.1 | 2.0 ± 0.1  | 6.4 ± 0.1 | 5.2± 0.1 | 2.1± 0.1 | 0.3±0.013 |

(mm)



## Cover Tape Dimensions

| Application | Carrier Width | Cover Tape Width | Devices Per Reel |
|-------------|---------------|------------------|------------------|
| SOP- 8/-P   | 12            | 9.3              | 2500             |

## Customer Service

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