4-Bit Micro-Controller With LCD Driver, 1K Word

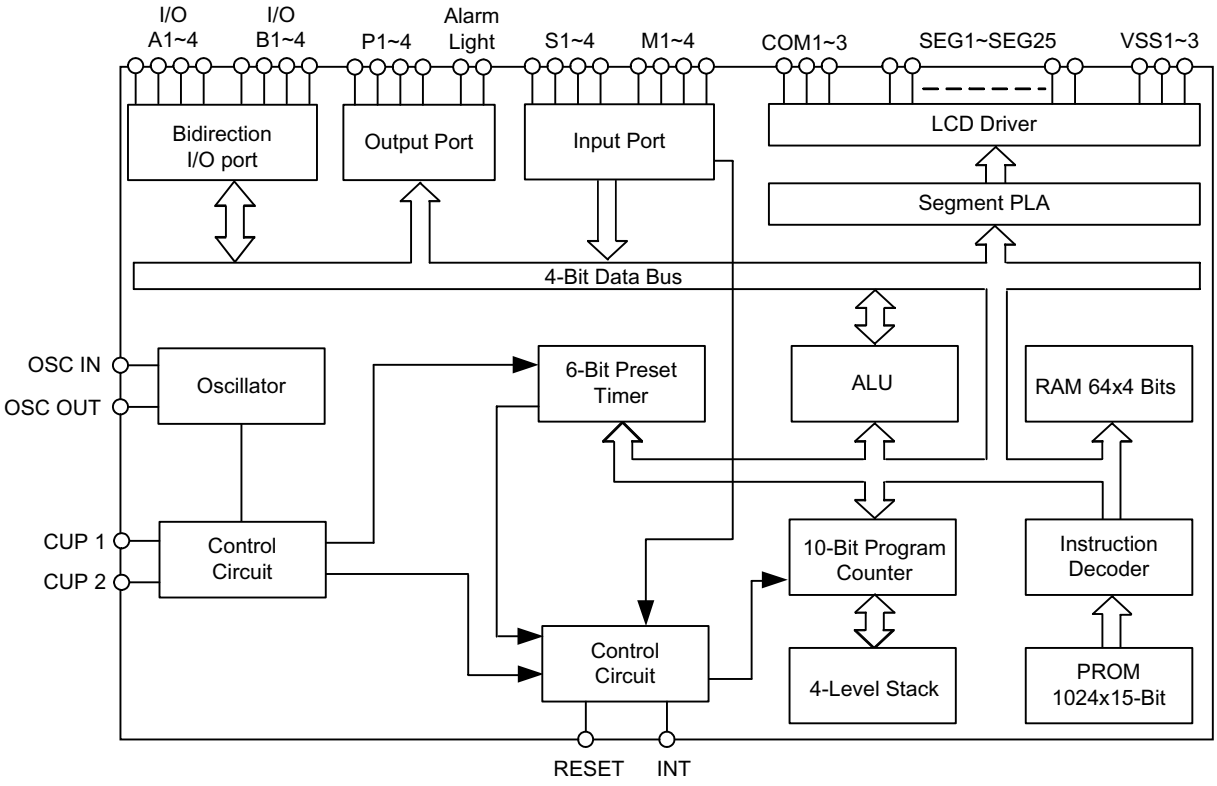
Features

- Very low current dissipation
- Wide operating voltage range
- Supports both Ag and Li batteries
- Powerful instruction set
- 4-level subroutine nesting (including interrupt)
- 4 event driven interrupts, 2 external and 2 internal
- ROM size: 1024x15 bits
- RAM size: 64x4 bits
- Input ports: 2 ports/8 pins (S and M)
- Output port: 1 port/4 pins (P)
- Pseudo serial output port (P)
- Input/output ports: 2 ports/8 pins (I/OA and I/OB)
- Control outputs: ALARM, LIGHT
- LCD driver outputs (can drive up to 75 LCD segments)
- Mask option to select 4 LCD drive modes: static, duplex (1/2 duty 1/2 bias, 1/3 duty 1/2 bias or 1/3 duty 1/3 bias)
- Mask option permits LCD driver output pins to be used for DC output ports; up to 25 pins are available
- Segment PLA circuit permits any layout on LCD panel
- Built-in clock generator (crystal or RC)
- Built-in voltage doubler, halver, tripler

General Description

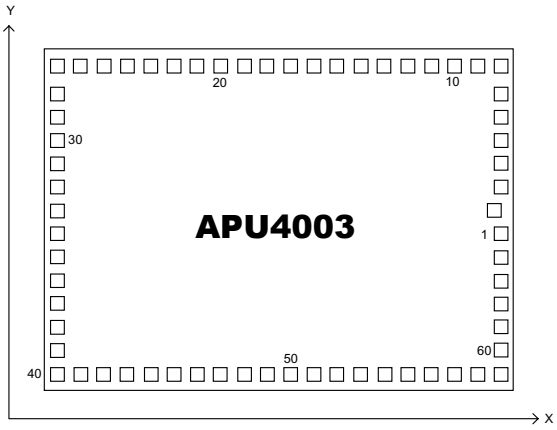
The APU4003 is a single chip 4-bit micro-controller with LCD drivers. It can drive up to 3 common times or 25 segments, i.e. a 75-segment LCD driver. This 4-bit micro-controller contains a 4-bit parallel processing ALU, 1024x15-bit program ROM, 64x4-bit data RAM, input/output ports, alarm driver, timer, clock generator, crystal and RC oscillator circuit, LCD driver and 79 powerful instructions in a single chip. The HALT instruction can be used to stop all internal operations other than timer, clock generator, crystal/RC oscillator and LCD driver. Very low current dissipation can be easily achieved by combining 4 kinds of interrupt functions and HALT instruction to minimize the operation cycle.

Block Diagram



Pad Assignment

Pad open: 90μm X 90μm
Pad pitch: 160μm (Min.)



Pad Coordinates

Pad No.	Pad Name	X (μm)	Y (μm)	Pad No.	Pad Name	X (μm)	Y (μm)
1	VDD	3118	1010	33	OSCIN	50	1170
2	GND	3087	1170	34	CAP	50	1010
3	VSS1	3113	1330	35	OSCOUT	50	850
4	VSSO	3118	1490	36	COM1	50	690
5	VSS2	3118	1650	37	SEG1	50	530
6	ALARM	3118	1810	38	SEG2	50	370
7	LIGHT	3118	1970	39	SEG3	50	210
8	S4	3118	2196	40	SEG4	50	50
9	S3	2935	2196	41	SEG5	210	50
10	IOA1	2775	2196	42	SEG6	370	50
11	IOA2	2615	2196	43	SEG7	530	50
12	IOA3	2455	2196	44	SEG8	690	50
13	IOA4	2295	2196	45	SEG9	850	50
14	IOB1	2135	2196	46	SEG10	1010	50
15	IOB2	1975	2196	47	SEG11	1170	50
16	IOB3	1815	2196	48	SEG12	1330	50
17	IOB4	1655	2196	49	SEG13	1490	50
18	RESET	1495	2196	50	SEG14	1650	50
19	INT	1335	2196	51	SEG15	1810	50
20	P1	1175	2196	52	SEG16	1970	50
21	P2	1015	2196	53	SEG17	2130	50
22	P3	855	2196	54	SEG18	2290	50
23	P4	695	2196	55	SEG19	2450	50
24	M1	535	2196	56	SEG20	2610	50
25	M2	375	2196	57	SEG21	2770	50
26	M3	215	2196	58	SEG22	2930	50
27	M3	50	2196	59	SEG23	3118	50
28	TESTA	50	1970	60	SEG24	3118	210
29	CUP1	50	1810	61	SEG25	3118	370
30	CUP2	50	1650	62	COM3	3118	530
31	S2	50	1490	63	COM2	3118	690
32	S1	50	1330	64	VSS3	3118	850

* Note: The substrate must connect to VDD.

Pin Description

Pin Name	Type	Description
OSCIN OSCOUT	I O	Typical 32.768kHz crystal is connected across OSCIN/OSCOUT for Oscillation; R/C oscillation mode also available.
CAP	I	Connected to OSCOUT for compensation capacitor.
S1~4	I	Port for input only with chattering eliminator for CK10 (32ms), CK8 (8ms) & CK6 (2ms). (PLA mask option).
M1~4	I	Input ports.
P1~4	O	Output ports.
IOA1~4	I/O	Input/Output ports. After power-on reset, sets as input mode.
IOB1~4	I/O	Input/Output ports. After power-on reset, sets as input mode.
INT	I	External interrupt request control input pin.
RESET	I	System reset pin.
LIGHT	O	Output only for outputting signal to drive transistor for light.
ALARM	O	Output only for outputting 4kHz/2kHz/1kHz modulation signal. Also can be used to output a non-modulation signal.
VDD	—	(+)Power supply pin.
GND	—	Power supply pin for logic unit inside LSI. When using Li version, a capacitor must be connected across GND and VDD to prevent the logic unit from malfunctioning.
VSS0 VSS1 VSS2 VSS3	—	(--) Power supply pin. * For Ag version, apply (--) side to both VSS0 & VSS1. For other than Ag version, apply (--) side to both VSS0 & VSS2. LCD power supply pin.
CUP1~2	O	Pins for connecting the voltage step-up (step-down) capacitor.
COM1~3	O	Output pins for LCD panel common plate. The following pin is used in each case. * Frequency can be doubled, quadrupled with PLA.

	Statuc	1/2 duty	1/3 duty
COM1	0	0	0
COM2	—	0	0
COM3	—	—	0
Alternating Frequency	32Hz*	32Hz*	43Hz*

SEG1~25	O	Output pins for LCD panel segments. * Also used as output ports with mask option.	
TESTA	*	Test pin (for internal testing only).	

Absolute Maximum Rating

Ta = 0 to 70℃, VDD=0V

Name	Symbol	Rating	Unit
Maximum Supply Voltage	V_{SS1}	-5.5 ~ +0.3	V
	V_{SS2}	-5.5 ~ +0.3	V
	V_{SS3}	-8.5 ~ +0.3	V
Maximum Input Voltage	V_{IN1}	V_{SS1}-0.3 to +0.3	V
	V_{IN2}	V_{SS2}-0.3 to +0.3	V
Maximum Output Voltage	V_{OUT1}	V_{SS1}-0.3 to +0.3	V
	V_{OUT2}	V_{SS2}-0.3 to +0.3	V
	V_{OUT3}	V_{SS3}-0.3 to +0.3	V
Maximum Operating Temperature	t_{OPG}	0 to +70	℃
Maximum Storage Temperature	t_{STG}	-25 to +125	℃

Allowable Operating Conditions

Ta = 0 to 70℃, V_{DD}=0V

Name	Symbol	Condition	Min.	Max.	Unit
Supply Voltage	V_{SS1}	External RC Mode	-5.25	-1.7	V
	V_{SS2}		-5.25	-3.5	V
	V_{SS3}		-8.0	-3.5	V
Supply Voltage	V_{SS1}	Crystal Mode	-5.25	-1.2	V
	V_{SS2}		-5.25	-2.4	V
	V_{SS3}		-8.0	-2.4	V
Oscillator Start-up Supply Voltage	V_{SS1}	Crystal Mode		-1.35	V
	V_{SS2}			-2.4	V
Input ″H″ Voltage	V_{IH1}	Ag Battery Mode	$0.3V_{SS1}$	0	V
Input ″L″ Voltage	V_{IL1}		V_{SS1}	$0.7V_{SS1}$	V
Input ″H″ Voltage	V_{IH2}	Li Battery Mode	$0.3V_{SS2}$	0	V
Input ″L″ Voltage	V_{IL2}		V_{SS2}	$0.7V_{SS2}$	V
Input ″H″ Voltage	V_{IH3}	OSCIN at Ext. RC & Ag Battery Mode	$0.3V_{SS1}$	0	V
Input ″L″ Voltage	V_{IL3}		V_{SS1}	$0.8V_{SS1}$	V
Input ″H″ Voltage	V_{IH4}	OSCIN at Ext. RC & Li Battery Mode	$0.2V_{SS2}$	0	V
Input ″L″ Voltage	V_{IL4}		V_{SS2}	$0.8V_{SS2}$	V
Operating Freq.	f_{OPG1}	Ag Battery Mode	32	32	kHz
	f_{OPG2}	Li Battery Mode	32	100	kHz
	f_{OPG3}	External RC Mode	32	1000	kHz

Electrical Characteristics

Ta=0 to 70℃, VDD=0V

Input resistance

Name	Symbol	Condition	Min.	Typ.	Max.	Unit
″L″-Level Hold t_R	R_{IIH1}	V_I=0.8V_{SS1}, #1	10	40	100	kΩ
	R_{IIH2}	V_I=0.8V_{SS2}, #2	10	40	100	kΩ
	R_{IIH3}	V_I=0.8V_{SS2}, #3	5	20	50	kΩ
M/S Pull-Down t_R	R_{MSD1}	V_I=V_{DD}, #1	200	500	1000	kΩ
	R_{MSD2}	V_I=V_{DD}, #2	200	500	1000	kΩ
	R_{MSD3}	V_I=V_{DD}, #3	100	250	500	kΩ
INT Pull-Up t_R	R_{INTU1}	V_I=V_{SS1}, #1	200	500	1000	kΩ
	R_{INTU2}	V_I=V_{SS2}, #2	200	500	1000	kΩ
	R_{INTU3}	V_I=V_{SS2}, #3	100	250	500	kΩ
INT Pull-Down t_R	R_{INTD1}	V_I=V_{DD}, #1	200	500	1000	kΩ
	R_{INTD2}	V_I=V_{DD}, #2	200	500	1000	kΩ
	R_{INTD3}	V_I=V_{DD}, #3	100	250	500	kΩ
RES Pull-Down t_R	R_{MSD1}	V_I=V_{DD} or V_{SS1}, #1	5	20	50	kΩ
	R_{MSD2}	V_I=V_{DD} or V_{SS2}, #2	5	20	50	kΩ
	R_{MSD3}	V_I=V_{DD} or V_{SS2}, #3	5	20	50	kΩ

Note: #1: V_{SS1}= -1.2V (Ag), #2: V_{SS2}= -2.4V (Li), #3: V_{SS2}= -4V (ExtV).

DC output characteristics

Name	Symbol	Condition	For	Min.	Typ.	Max.	Unit
Output ″H″ Voltage	V_{OH1a}	I_{OH}=-200μA, #1	Alarm Light	-0.5	-0.3	-0.1	V
	$V_{OH2\ a}$	I_{OH}=-1mA, #2		-1	-0.6	-0.3	V
	$V_{OH3\ a}$	I_{OH}=-3mA, #3		-1.5	-1.0	-0.5	V
Output ″L″ Voltage	$V_{OL1\ a}$	I_{OL}=400μA, #1	P port IOA-n IOB-n	-1.1	-0.9	-0.7	V
	$V_{OL2\ a}$	I_{OL}=2mA, #2		-2.1	-1.8	-1.4	V
	$V_{OL3\ a}$	I_{OL}=6mA, #3		-3.5	-3.0	-2.5	V
Output ″H″ Voltage	V_{OH1b}	I_{OH}=-100μA, #1		-0.5	-0.3	-0.1	V
	V_{OH2b}	I_{OH}=-500μA, #2		-1	-0.6	-0.3	V
	V_{OH3b}	I_{OH}=-1.5mA, #3		-1.5	-1.0	-0.5	V
Output ″L″ Voltage	V_{OL1b}	I_{OL}=200μA, #1		-1.1	-0.9	-0.7	V
	V_{OL2b}	I_{OL}=1mA, #2		-2.1	-1.8	-1.4	V
	V_{OL3b}	I_{OL}=3mA, #3		-3.5	-3.0	-2.5	V

Note: #1: V_{SS1}= -1.2V (Ag), #2: V_{SS2}= -2.4V (Li), #3: V_{SS2}= -4V (ExtV).

Segment driver output characteristics

Name	Symbol	Condition	For	Min.	Typ.	Max.	Unit
CMOS output mode							
Output ″H″ Voltage	V_{OH1c}	I_{OH}=-10μA, #1	SEG-n	-0.5	-0.3	-0.1	V
	V_{OH2c}	I_{OH}=-50μA, #2		-1	-0.6	-0.3	V
	V_{OH3c}	I_{OH}=-200μA, #3		-1.5	-1.0	-0.5	V
Output ″L″ Voltage	V_{OL1c}	I_{OL}=20μA, #1		-1.1	-0.9	-0.7	V
	V_{OL2c}	I_{OL}=100μA, #2		-2.1	-1.8	-1.4	V
	V_{OL3c}	I_{OL}=400μA, #3		-3.5	-3.0	-2.5	V
Static display mode							
Output ″H″ Voltage	V_{OH1d}	I_{OH}=-1μA, #1	SEG-n	-0.2			V
	V_{OH2d}	I_{OH}=-1μA, #2		-0.2			V
	V_{OH3d}	I_{OH}=-1μA, #3		-0.2			V
Output ″L″ Voltage	V_{OL1d}	I_{OL}=1μA, #1				-1.0	V
	V_{OL2d}	I_{OL}=1μA, #2				-2.2	V
	V_{OL3d}	I_{OL}=1μA, #3				-3.8	V
Output ″H″ Voltage	V_{OH1e}	I_{OH}=-10μA, #1	COM-n	-0.2			V
	V_{OH2e}	I_{OH}=-10μA, #2		-0.2			V
	V_{OH3e}	I_{OH}=-10μA, #3		-0.2			V
Output ″L″ Voltage	V_{OL1e}	I_{OL}=10μA, #1				-1.0	V
	V_{OL2e}	I_{OL}=10μA, #2				-2.2	V
	V_{OL3e}	I_{OL}=10μA, #3				-3.8	V
Duplex (1/2 bias, 1/2 duty) display mode							
Output ″H″ Voltage	V_{OH12f}	I_{OH}=-1μA, #1, #2	SEG-n	-0.2			V
	V_{OH3f}	I_{OH}=-1μA, #3		-0.2			V
Output ″L″ Voltage	V_{OL12f}	I_{OL}=1μA, #1, #2				-2.2	V
	V_{OL3f}	I_{OL}=1μA, #3				-3.8	V

Name	Symbol	Condition	For	Min.	Typ.	Max.	Unit
Output ″H″ Voltage	V_{OH12g}	I_{OH}=-10μA, #1, #2	COM-n	-0.2			V
	V_{OH3g}	I_{OH}=-10μA, #3		-0.2			V
Output ″M″ Voltage	V_{OM12g}	$I_{OI/H}$=±10μA, #1, #2		-1.4		-1.0	V
	V_{OM3g}	$I_{OI/H}$=±10μA, #3		-2.2		-1.8	V
Output ″L″ Voltage	V_{OL12g}	I_{OL}=10μA, #1, #2				-2.2	V
	V_{OL3g}	I_{OL}=10μA, #3				-3.8	V
1/2 bias, 1/3 duty display mode							
Output ″H″ Voltage	V_{OH12h}	I_{OH}=-1μA, #1, #2	SEG-n	-0.2			V
	V_{OH3h}	I_{OH}=-1μA, #3		-0.2			V
Output ″L″ Voltage	V_{OL12h}	I_{OL}=1μA, #1, #2				-2.2	V
	V_{OL3h}	I_{OL}=1μA, #3				-3.8	V
Output ″H″ Voltage	V_{OH12i}	I_{OH}=-10μA, #1, #2	COM-n	-0.2			V
	V_{OH3i}	I_{OH}=-10μA, #3		-0.2			V
Output ″M″ Voltage	V_{OM12i}	$I_{OI/H}$=±10μA, #1, #2		-1.4		-1.0	V
	V_{OM3i}	$I_{OI/H}$=±10μA, #3		-2.2		-1.8	V
Output ″L″ Voltage	V_{OL12i}	I_{OL}=10μA, #1, #2				-2.2	V
	V_{OL3i}	I_{OL}=10μA, #3				-3.8	V
1/3bias, 1/3duty display mode							
Output ″H″ Voltage	V_{OH12j}	I_{OH}=-1μA, #1, #2	SEG-n	-0.2			V
	V_{OH3j}	I_{OH}=-1μA, #3		-0.2			V
Output ″M1″ Voltage	V_{OM12j}	$I_{OI/H}$=±10μA, #1, #2		-1.4		-1.0	V
	V_{OM13j}	$I_{OI/H}$=±10μA, #1, #2		-2.2		-1.8	V
Output ″M2″ Voltage	V_{OM22j}	$I_{OI/H}$=±10μA, #1, #2		-2.6		-2.2	V
	V_{OM23j}	$I_{OI/H}$=±10μA, #1, #2		-4.2		-3.8	V
Output ″L″ Voltage	V_{OL2j}	I_{OL}=1μA, #2				-3.4	V
	V_{OL3j}	I_{OL}=1μA, #3				-5.8	V
Output ″H″ Voltage	V_{OH2k}	I_{OH}=-10μA, #2	COM-n	-0.2			V
	V_{OH3k}	I_{OH}=-10μA, #3		-0.2			V
Output ″M1″ Voltage	V_{OM12k}	$I_{OI/H}$=±10μA, #1, #2		-1.4		-1.0	V
	V_{OM13k}	$I_{OI/H}$=±10μA, #3		-2.2		-1.8	V
Output ″M2″ Voltage	V_{OM22k}	$I_{OI/H}$=±10μA, #1, #2		-2.6		-2.2	V
	V_{OM23k}	$I_{OI/H}$=±10μA, #3		-4.2		-3.8	V
Output ″L″ Voltage	V_{OL2k}	I_{OL}=1μA, #2				-3.4	V
	V_{OL3k}	I_{OL}=1μA, #3				-5.8	V

Note: #1: V_{SS1}= -1.2V (Ag), #2: V_{SS2}= -2.4V (Li), #3: V_{SS2}= -4V (ExtV).

Instruction Table

Instruction	Machine Code	Function	Remark	Flag
NOP	000 0000 0000 0000	No Operation		
LCT Y,X	000 00YY YYXX XXXX	(Ly) ← (Rx)	Y=000- No Use	
OPPS X,D	000 1110 1DXX XXXX	P1,2,3,4 ← (Rx0,1),D,Pulse		
MRA X	000 1101 01XX XXXX	CF ← (Rx3)		

Instruction	Machine Code	Function	Remark	Flag
OPP X	000 1110 00XX XXXX	Port(P) ← (Rx)		
OPA X	000 0100 01XX XXXX	Port(A) ← (Rx)		
OPB X	000 1000 01XX XXXX	Port(B) ← (Rx)		
LCB Y,X	000 01YY YYXX XXXX	(Ly) ← (Rx)	Y=000- No Use	
LCP Y,X	001 10YY YYXX XXXX	abcd,efgh ← (Rx),(AC)	Y=000- No Use	
ADC X	001 0000 00XX XXXX	(AC) ← (Rx)+(AC)+(CF)		CF
ADC* X	001 0000 10XX XXXX	(AC),(Rx) ← (Rx)+(AC)+(CF)		CF
SBC X	001 0001 00XX XXXX	(AC) ← (Rx)+(AC)B+(CF)		CF
SBC* X	001 0001 10XX XXXX	(AC),(Rx) ← (Rx)+(AC)B+(CF)		CF
ADD X	001 0010 00XX XXXX	(AC) ← (Rx)+(AC)		CF
ADD* X	001 0010 10XX XXXX	(AC),(Rx) ← (Rx)+(AC)		CF
SUB X	001 0011 00XX XXXX	(AC) ← (Rx)+(AC) B+1		CF
SUB* X	001 0011 10XX XXXX	(AC),(Rx) ← (Rx)+(AC) B+1		CF
ADN X	001 0100 00XX XXXX	(AC) ← (Rx)+(AC)		
ADN* X	001 0100 10XX XXXX	(AC),(Rx) ← (Rx)+(AC)		
AND X	001 0101 00XX XXXX	(AC) ← (Rx) AND (AC)		
AND* X	001 0101 10XX XXXX	(AC),(Rx) ← (Rx) AND (AC)		
EOR X	001 0110 00XX XXXX	(AC) ← (Rx) EOR (AC)		
EOR* X	001 0110 10XX XXXX	(AC),(Rx) ← (Rx) EOR (AC)		
OR X	001 0111 00XX XXXX	(AC) ← (Rx) OR (AC)		
OR* X	001 0111 10XX XXXX	(AC),(Rx) ← (Rx) OR (AC)		
ADCI Y,D	001 1000 0DDD DYYY	(AC) ← (Ry)+(D)+(CF)		CF
ADCI* Y,D	001 1000 1DDD DYYY	(AC),(Ry) ← (Ry)+(D)+(CF)		CF
SBCI Y,D	001 1001 0DDD DYYY	(AC) ← (Ry)+(D)B+(CF)		CF
SBCI* Y,D	001 1001 1DDD DYYY	(AC),(Ry) ← (Ry)+(D)B+(CF)		CF
ADDI Y,D	001 1010 0DDD DYYY	(AC) ← (Ry)+(D)		CF
ADDI* Y,D	001 1010 1DDD DYYY	(AC),(Ry) ← (Ry)+(D)		CF
SUBI Y,D	001 1011 0DDD DYYY	(AC) ← (Ry)+(D)B+1		CF
SUBI* Y,D	001 1011 1DDD DYYY	(AC),(Ry) ← (Ry)+(D)B+1		CF
ADNI Y,D	001 1100 0DDD DYYY	(AC) ← (Ry)+(D)		
ADNI* Y,D	001 1100 1DDD DYYY	(AC),(Ry) ← (Ry)+(D)		
ANDI Y,D	001 1101 0DDD DYYY	(AC) ← (Ry) AND (D)		
ANDI* Y,D	001 1101 1DDD DYYY	(AC),(Ry) ← (Ry) AND (D)		
EORI Y,D	001 1110 0DDD DYYY	(AC) ← (Ry) EOR (D)		
EORI* Y,D	001 1110 1DDD DYYY	(AC),(Ry) ← (Ry) EOR (D)		
ORI Y,D	001 1111 0DDD DYYY	(AC) ← (Ry) OR (D)		
ORI* Y,D	001 1111 1DDD DYYY	(AC),(Ry) ← (Ry) OR (D)		
MRW Y,X	011 100Y YYXX XXXX	(AC),(Ry) ← (Rx)		
MWR X,Y	011 110Y YYXX XXXX	(AC),(Rx) ← (Ry)		
LDS X,D	010 01DD DDXX XXXX	(AC),(Rx) ← (D)		
IPS X	010 0000 00XX XXXX	(AC),(Rx) ← Port(S)		
IPM X	010 0000 10XX XXXX	(AC),(Rx) ← Port(M)		

Instruction	Machine Code	Function	Remark	Flag
IPA X	010 0001 00XX XXXX	(AC),(Rx) ← Port(A)		
IPA* X	010 0001 01XX XXXX	(AC),(Rx) ← Port(A)	I/OA ← I/P	
IPB X	010 0001 10XX XXXX	(AC),(Rx) ← Port(B)		
IPB* X	010 0001 11XX XXXX	(AC),(Rx) ← Port(B)	I/OB ← I/P	
MAF X	011 0001 00XX XXXX	(AC),(Rx) ← STS1	TF2: AC=0 TF3: CF	
MSB X	010 0010 00XX XXXX	(AC),(Rx) ← STS2	B0: BCF B1: SCF1(MPT) B2: SCF2(HRF) B3: SCF3(SPT)	
MSC X	011 0000 00XX XXXX	(AC),(Rx) ← STS3	B0: SCF4(INT) B1: SCF5(TMR) B2: PH15 B3: SCF7(PDV)	
STA X	010 0010 10XX XXXX	(Rx) ← (AC)		
SR0 X	010 0011 00XX XXXX	(ACn),(Rxn) ← (Rxn+1) (AC3),(Rx3) ← 0		
SR1 X	010 0011 01XX XXXX	(ACn),(Rxn) ← (Rxn+1) (AC3),(Rx3) ← 1		
SL0 X	010 0011 10XX XXXX	(ACn),(Rxn) ← (Rxn-1) (AC0),(Rx0) ← 0		
SL 1 X	010 0011 11XX XXXX	(ACn),(Rxn) ← (Rxn-1) (AC0),(Rx0) ← 1		
LDA X	011 0111 10XX XXXX	(AC) ← (Rx)		
JB0 X	100 00XX XXXX XXXX	(PC) ← X	if (AC0)=1	
JB1 X	100 01XX XXXX XXXX	(PC) ← X	if (AC1)=1	
JB2 X	100 10XX XXXX XXXX	(PC) ← X	if (AC2)=1	
JB3 X	100 11XX XXXX XXXX	(PC) ← X	if (AC3)=1	
JNZ X	101 00XX XXXX XXXX	(PC) ← X	if (AC) ≠ 0	
JNC X	101 01XX XXXX XXXX	(PC) ← X	if (CF)=0	
JZ X	101 10XX XXXX XXXX	(PC) ← X	if (AC)=0	
JC X	101 11XX XXXX XXXX	(PC) ← X	if (CF)=1	
JMP X	110 00XX XXXX XXXX	(PC) ← X		
CALL X	110 01XX XXXX XXXX	(STACK) ← (PC)+1 (PC) ← X		
RTS	110 1000 0000 0000	(PC) ← (STACK)		
SMS X	111 0000 000X XXXX	SEF0~3 ← X0~3 SEF4 ← X4	S1~4 is Enabled M1~4 Enable	SCF3 SCF1 HRF0
TMS X	111 0010 00XX XXXX	TIMER ← X		HRF1
SF X	111 0100 0XXX XXXX	X6: M-PORT Pull-Low X5: S-PORT Pull-Low X3: HALT After Light X2: LIGHT ON X1: BCF Set X0: CF Set		BCF CF

Instruction	Machine Code	Function				Remark	Flag
RF X	111 0110 0XXX XXXX	X6: M-PORT Low-L-H X5: S-PORT Low-L-H X2: LIGHT OFF X1: BCF Reset X0: CF Reset					
ALM X	111 0111 XXXX XXXX	X7,X6	0 , 1	1 , 0	1 , 1		
		Signal	DC	1K/2K	4kHz		
		Xn=1	X5	X4	X3		
		Signal	1Hz	2Hz	4Hz		
		Xn=1	X2	X1	X0		
		Signal	8Hz	16Hz	32Hz		
SIE X	111 1000 XXXX XXXX	X5~7: HEF1~3 is Enabled X0~3: IEF0~3 is Enabled					
SIE* X	111 1010 0000 XXXX	X0~3: IEF0~3 is Enabled					
PLC X	111 110X XXXX XXXX	X0~3: Reset HRF0~3 X8: Reset PH11~15					
HALT	111 1111 1111 1111						

Symbol description

AC:	Accumulator	CF:	Carry Flag
ACn:	Accumulator Bit N	BCF:	Backup Flag
Rx:	Memory of Address X	IEFn:	Interrupt Enable Flag
Rxn:	Memory Bit N of Address X	HEFn:	HALT Release Enable Flag
Ry:	Memory of Working Register Y	HRFn:	HALT Release Flag
D:	Immediate Data	SEFn:	Switch Enable Flag
PC:	Program Counter	SCFn:	Start Condition Flag
:	LCD Latch		