

## 4-Bit Micro-Controller with LCD Driver, 1K Word

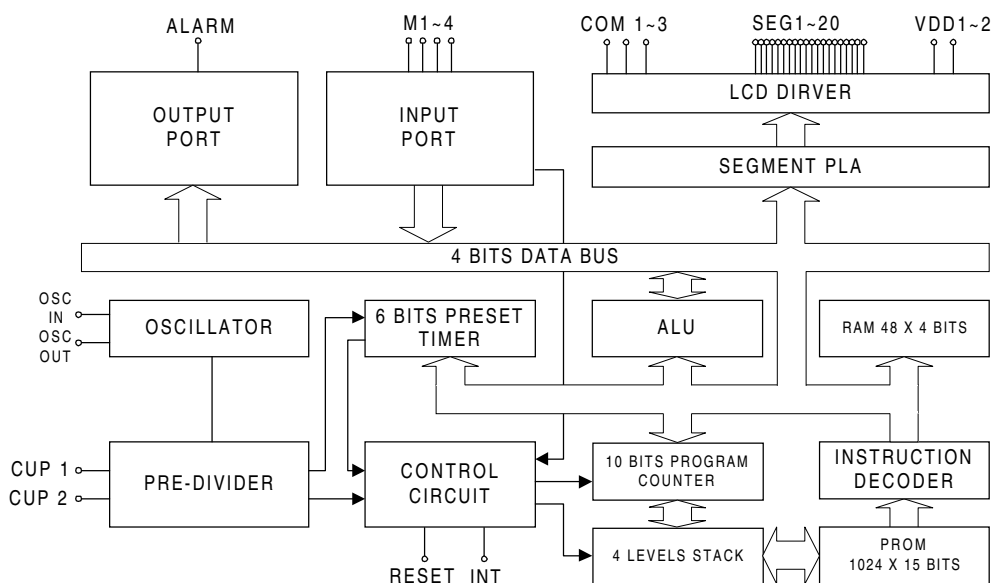
### FEATURES

- Very low current dissipation.
- Wide operating voltage range.
- Supports both Ag and Li batteries.
- Powerful instruction set.
- 4-level subroutine nesting (including interrupt).
- 4 event driven interrupts, 2 external and 2 internal.
- ROM size: 1024 x 15 bits.
- RAM size: 48 x 4 bits.
- Input ports: 1 port/ 4 pins (M-PORT).
- Control output: ALARM.
- LCD driver outputs (can drive up to 60 LCD segments).
- Mask option to select 3 LCD drive modes: static, duplex 1/2 duty 1/2 bias, 1/3 duty 1/2 bias.
- Mask option permits LCD driver output pins to be used for DC output ports. Up to 20 pins are available. SEG13-SEG20 can be selected by open-drain output.
- Segment PLA circuit permits any layout on the LCD panel.
- Built-in clock generator (crystal or RC).
- Built-in voltage doubler, halver.

### GENERAL DESCRIPTION

The APU4006 is a single-chip 4-bit microcontroller with LCD drivers. It can drive up to 3 common time 20 segments, i.e. 60 segments LCD driver. This 4-bit microcontroller contains a 4-bit parallel processing ALU, 1024 x 15-bit program ROM, 48 x 4-bit data RAM, input ports, alarm driver, timer, clock generator, crystal and RC oscillator circuit, LCD driver and 70 powerful instructions in a single chip. It uses HALT instruction to stop all internal operations other than the timer, clock generator, crystal/RC oscillator and LCD driver. Very low current dissipation can be easily achieved by combining 4 types of interrupt function and HALT instruction to minimize the operation cycle.

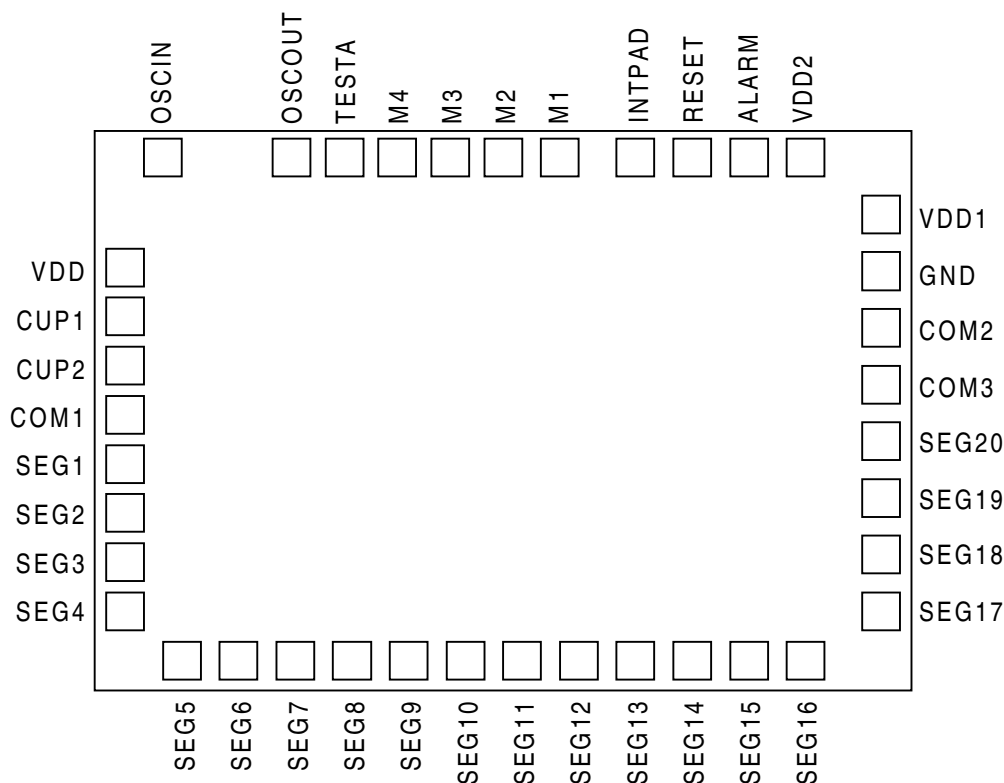
### BLOCK DIAGRAM



## 1.0 PACKAGE & CHIP INFORMATION

Chip Size 1995 x 1590 (  $\mu\text{m}^2$  )  
 Pad Pitch min. 140  $\mu\text{m}$

### Bounding Diagram



## 2.0 PIN/PAD ASSIGNMENT

Unit :  $\mu\text{m}$

Pad No.	Name	Coordinate		Pad No.	Name	Coordinate	
		X	Y			X	Y
1	GND	1909.5	1128.60	21	SEG4	85.50	199.50
2	VDD1	1909.5	1275.60	22	SEG5	234.00	88.50
3	VDD2	1757.40	1500.60	23	SEG6	381.00	88.50
4	ALARM	1610.40	1500.60	24	SEG7	519.00	88.50
5	RESET	1465.80	1500.60	25	SEG8	657.00	88.50
6	INT	1327.80	1500.60	26	SEG9	795.00	88.50
7	M1	1152.00	1500.60	27	SEG10	933.00	88.50
8	M2	1023.00	1500.60	28	SEG11	1071.00	88.50
9	M3	894.00	1500.60	29	SEG12	1209.00	88.50
10	M4	765.00	1500.60	30	SEG13	1347.00	88.50
11	TESTA	636.00	1500.60	31	SEG14	1485.00	88.50
12	OSCOUT	498.00	1500.60	32	SEG15	1623.00	88.50

13	OSCIN	155.10	1500.60	33	SEG16	1761.00	88.50
14	VDD	85.50	1132.50	34	SEG17	1909.50	219.60
15	CUP1	85.50	994.50	35	SEG18	1909.50	375.60
16	CUP2	85.50	865.50	36	SEG19	1909.50	527.10
17	COM1	85.50	736.50	37	SEG20	1909.50	678.60
18	SEG1	85.50	607.50	38	COM3	1909.50	830.10
19	SEG2	85.50	478.50	39	COM2	1909.50	981.60
20	SEG3	85.50	349.50				

\*Note: The substrate must connect to GND.

### 3.0 PIN DESCRIPTION

Name	Type	Description								
OSCIN OSCOOUT	I O	Typical 32.768kHz crystal is connected across OSCIN/OSCOOUT for oscillation, R/C oscillation mode is also available.								
M1 - 4	I	Input pins with pull-down Tr or "L-level hold" Tr.								
INT	I	External interrupt request control input pin.								
RESET	I	System reset pin with pull-down resistance.								
ALARM	O	Output only for outputting 4kHz/2kHz/1kHz modulation signal. Also can be used to output non-modulation signal.								
VDD		Power supply pin for logic unit inside LSI. When using Li version, a capacitor must be connected across GND and VDD to prevent logic unit from malfunctioning.								
VDD1		For Ag-B mode positive power supply pin.								
VDD2		For Li-B(EXTV) mode positive power supply pin.								
GND		Negative power supply pin.								
CUP1 - 2	O	Pins for connecting voltage step-up (step-down) capacitor.								
COM1 - 3	O	Output pins for LCD panel common plate. The following pins are used in each case. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th></th> <th>Static</th> <th>1/2 duty</th> <th>1/3 duty</th> </tr> </thead> <tbody> <tr> <td>COM1 COM2 COM3 Alternating frequency</td> <td>32Hz*</td> <td>32Hz*</td> <td>43Hz*</td> </tr> </tbody> </table>		Static	1/2 duty	1/3 duty	COM1 COM2 COM3 Alternating frequency	32Hz*	32Hz*	43Hz*
	Static	1/2 duty	1/3 duty							
COM1 COM2 COM3 Alternating frequency	32Hz*	32Hz*	43Hz*							
SEG1 - 20	O	Output pins for LCD panel segments. * Also used as output ports with mask option.								
TESTA	*	Test pin (for internal testing only).								

## 4.0 ABSOLUTE MAXIMUM RATINGS

at  $T_a = 0$  to  $70^{\circ}\text{C}$ ,  $\text{GND} = 0\text{V}$

Name	Symbol	Range	Unit
Maximum Supply Voltage	VDD1	+1.3 to +5.5	V
	VDD2	+2.5 to +5.5	V
Maximum Input Voltage	Vin1	-0.3 to VDD1+0.3	V
Maximum Output Voltage	Vout1	-0.3 to VDD1+0.3	V
	Vout2	-0.3 to VDD2+0.3	V
Maximum Operating Temperature	Topg	0 to +70	$^{\circ}\text{C}$
Maximum Storage Temperature	Tstg	-25 to +125	$^{\circ}\text{C}$

## 5.0 ALLOWABLE OPERATING CONDITIONS

at  $T_a = 0$  to  $70^{\circ}\text{C}$ ,  $\text{GND} = 0\text{V}$

Name	Symb.	Condition	Min.	Max.	Unit
Supply Voltage	VDD1	External RC Mode	1.5	5.25	V
	VDD2		3.5	5.25	V
Supply Voltage	VDD1	Crystal Mode	1.2	5.25	V
	VDD2		2.4	5.25	V
Oscillator Start-Up Supply Voltage	Vss1	Crystal Mode	1.2V		V
	Vss2		1.2V		V
Input "H" Voltage	Vih1	Ag Battery Mode	VDD1-0.3	VDD1+0.3	V
Input "L" Voltage	Vil1		-0.5	0.2	V
Input "H" Voltage	Vih2	Li Battery Mode	VDD2-0.6	VDD2+0.6	V
Input "L" Voltage	Vil2		-0.7	0.7	V
Input "H" Voltage	Vih3	OSCIN at Ext. RC & Ag Battery Mode	$0.8 \times \text{VDD1}$	VDD1	V
Input "L" Voltage	Vil3		0	$0.2 \times \text{VDD1}$	V
Input "H" Voltage	Vih4	OSCIN at Ext. RC & Li Battery Mode	$0.8 \times \text{VDD2}$	VDD2	V
Input "L" Voltage	Vil4		0	$0.2 \times \text{VDD2}$	V
Operating Freq.	Fopg1	Ag Battery Mode	32	32	KHz
	Fopg2	Li Battery Mode	32	100	KHz
	Fopg3	External RC Mode	32	1000	KHz

## 6.0 ELECTRICAL CHARACTERISTICS

at #1 : VDD1 = 1.2V ( Ag ); #2 : VDD2 = 2.4V ( Li ); #3 : VDD2 = 4V (ExtV).

### 6.1 Input Resistance

Name	Symb.	Condition	Min.	Typ.	Max.	Unit
M-Port L-Level Hold Tr	Rllh1	$V_i = 0.2\text{VDD1}$ , #1	10	40	100	Kohm
	Rllh2	$V_i = 0.2\text{VDD1}$ , #2	10	40	100	Kohm
	Rllh3	$V_i = 0.2\text{VDD1}$ , #3	5	20	50	Kohm
M-Port Pull-Down Tr	Rmsd1	$V_i = \text{VDD1}$ , #1	200	700	2000	Kohm
	Rmsd2	$V_i = \text{VDD2}$ , #2	200	500	1000	Kohm
	Rmsd3	$V_i = \text{VDD2}$ , #3	100	250	500	Kohm
INT Pull-Up Tr	Rintu1	$V_i = \text{VDD1}$ , #1	200	700	2000	Kohm

	Rintu2	Vi = VDD2, #2	200	500	1000	Kohm
	Rintu3	Vi = VDD2, #3	100	250	500	Kohm
INT Pull-Down Tr	Rintd1	Vi = GND, #1	200	700	2000	Kohm
	Rintd2	Vi = GND, #2	200	500	1000	Kohm
	Rintd3	Vi = GND, #3	100	250	500	Kohm
RES Pull-Down R	Rres1	Vi = GND or VDD1, #1	5	20	50	Kohm
	Rres2	Vi = GND or VDD2, #2	5	20	50	Kohm
	Rres3	Vi = GND or VDD2, #3	5	20	50	Kohm

## 6.2 DC Output Characteristics

Name	Symb.	Condition	for	Min.	Typ.	Max.	Unit
Output "H" Voltage	Voh1a	Ioh = 200 A, #1	Alarm	0.8	0.9	1.0	V
	Voh2a	Ioh = 500 A, #2		1.5	1.8	2.1	V
	Voh3a	Ioh = 1mA, #3		2.5	3	3.5	V
Output "L" Voltage	Vol1a	Iol = 400 A, #1		0.2	0.3	0.4	V
	Vol2a	Iol = 1mA, #2		0.3	0.6	0.9	V
	Vol3a	Iol = 2mA, #3		0.5	1	1.5	V

## 6.3 Segment Driver Output Characteristics

Name	Symb.	Condition	for	Min.	Typ.	Max.	Unit
<b>CMOS Output Mode</b>							
Output "H" Voltage	Voh1c	Ioh = -10uA, #1	SEGn	0.8	0.9	1.0	V
	Voh2c	Ioh = -50uA, #2		1.5	1.8	2.1	V
	Voh3c	Ioh = -200uA, #3		2.5	3	3.5	V
Output "L" Voltage	Vol1c	Iol = 20uA, #1		0.2	0.3	0.4	V
	Vol2c	Iol = 100uA, #2		0.3	0.6	0.9	V
	Vol3c	Iol = 400uA, #3		0.5	1	1.5	V
<b>Static Display Mode</b>							
Output "H" Voltage	Voh1d	Ioh = -1uA, #1	SEGn			1.0	V
	Voh2d	Ioh = -1uA, #2				2.2	V
	Voh3d	Ioh = -1uA, #3				3.8	V
Output "L" Voltage	Vol1d	Iol = 1uA, #1		0.2			V
	Vol2d	Iol = 1uA, #2		0.2			V
	Vol3d	Iol = 1uA, #3		0.2			V
Output "H" Voltage	Voh1e	Ioh = -10uA, #1	COMn			1.0	V
	Voh2e	Ioh = -10uA, #2				2.2	V
	Voh3e	Ioh = -10uA, #3				3.8	V
Output "L" Voltage	Vol1e	Iol = 10uA, #1		0.2			V
	Vol2e	Iol = 10uA, #2		0.2			V
	Vol3e	Iol = 10uA, #3		0.2			V
<b>Duplex (1/2 Bias, 1/2 Duty) Display Mode</b>							
Output "H" Voltage	Voh12f	Ioh = -1uA, #1, #2	SEGn			2.2	V
	Voh3f	Ioh = -1uA, #3				3.8	V
Output "L" Voltage	Vol12f	Iol = 1uA, #1, #2		0.2			V
	Vol3f	Iol = 1uA, #3		0.2			V
Output "H" Voltage	Voh12g	Ioh = -10uA, #1, #2	COMn			2.2	V
	Voh3g	Ioh = -10uA, #3				3.8	V

Output "M" Voltage	Vom12g	Iol/h= +/-10uA, #1, #2		1.0		1.4	V
	Vom3g	Iol/h= +/-10uA, #3		1.8		2.2	V
Output "L" Voltage	Vol12g	Iol = 10uA, #1		0.2			V
	Vol3g	Iol = 10uA, #3		0.2			V
<b>1/2 Bias, 1/3 Duty Display Mode</b>							
Output "H" Voltage	Voh12h	Ioh = -1uA, #1, #2	SEgN				V
	Voh3h	Ioh = -1uA, #3					V
Output "L" Voltage	Vol12h	Iol = 1uA, #1, #2	SEgN	0.2			V
	Vol3h	Iol = 1uA, #3		0.2			V
Output "H" Voltage	Voh12i	Ioh = -10uA, #1, #2	COMn			2.2	V
	Voh3i	Ioh = -10uA, #3				3.8	V
Output "M" Voltage	Vom12i	Iol/h= +/-10uA, #1, #2	COMn	1.0		1.4	V
	Vom3i	Iol/h= +/-10uA, #3		1.8		2.2	V
Output "L" Voltage	Vol12i	Iol = 10uA, #1, #2	COMn	0.2			V
	Vol3i	Iol = 10uA, #3		0.2			V

## 6.4 Instruction Table

Note: Rx=28~37 not used

Instruction	Machine Code	Function	Remark	Flag
NOP	000 0000 0000 0000	No Operation		
LCT Y,X	000 00YY YYXX XXXX	(Ly) <= (Rx)	Y=000- No Use	
MRA X	000 1101 01XX XXXX	CF <= (Rx3)		
LCB Y,X	000 01YY YYXX XXXX	(Ly) <= (Rx)	Y=000- No Use	
LCP Y,X	000 10YY YYXX XXXX	abcd,efgh <= (Rx),(AC)	Y=000- No Use	
ADC X	001 0000 00XX XXXX	(AC) <= (Rx)+(AC)+(CF)		CF
ADC* X	001 0000 10XX XXXX	(AC),(Rx) <= (Rx)+(AC)+(CF)		CF
SBC X	001 0001 00XX XXXX	(AC) <= (Rx)+(AC)B+(CF)		CF
SBC* X	001 0001 10XX XXXX	(AC),(Rx) <= (Rx)+(AC)B+(CF)		CF
ADD X	001 0010 00XX XXXX	(AC) <= (Rx)+(AC)		CF
ADD* X	001 0010 10XX XXXX	(AC),(Rx) <= (Rx)+(AC)		CF
SUB X	001 0011 00XX XXXX	(AC) <= (Rx)+(AC)B+1		CF
SUB* X	001 0011 10XX XXXX	(AC),(Rx) <= (Rx)+(AC)B+1		CF
ADN X	001 0100 00XX XXXX	(AC) <= (Rx)+(AC)		
ADN* X	001 0100 10XX XXXX	(AC),(Rx) <= (Rx)+(AC)		
AND X	001 0101 00XX XXXX	(AC) <= (Rx) AND (AC)		
AND* X	001 0101 10XX XXXX	(AC),(Rx) <= (Rx) AND (AC)		
EOR X	001 0110 00XX XXXX	(AC) <= (Rx) EOR (AC)		
EOR* X	001 0110 10XX XXXX	(AC),(Rx) <= (Rx) EOR (AC)		
OR X	001 0111 00XX XXXX	(AC) <= (Rx) OR (AC)		
OR* X	001 0111 10XX XXXX	(AC),(Rx) <= (Rx) OR (AC)		
ADCI Y,D	001 1000 0DDD DYYY	(AC) <= (Ry)+(D)+(CF)		CF
ADCI* Y,D	001 1000 1DDD DYYY	(AC),(Ry) <= (Ry)+(D)+(CF)		CF
SBCI Y,D	001 1001 0DDD DYYY	(AC) <= (Ry)+(D)B+(CF)		CF
SBCI* Y,D	001 1001 1DDD DYYY	(AC),(Ry) <= (Ry)+(D)B+(CF)		CF
ADDI Y,D	001 1010 0DDD DYYY	(AC) <= (Ry)+(D)		CF
ADDI* Y,D	001 1010 1DDD DYYY	(AC),(Ry) <= (Ry)+(D)		CF
SUBI Y,D	001 1011 0DDD DYYY	(AC) <= (Ry)+(D)B+1		CF
SUBI* Y,D	001 1011 1DDD DYYY	(AC),(Ry) <= (Ry)+(D)B+1		CF
ADNI Y,D	001 1100 0DDD DYYY	(AC) <= (Ry)+(D)		
ADNI* Y,D	001 1100 1DDD DYYY	(AC),(Ry) <= (Ry)+(D)		

# APLUS

# APU4006

Instruction	Machine Code	Function	Remark	Flag
ANDI Y,D	001 1101 0DDD DYYY	(AC) <= (Ry) AND (D)		
ANDI* Y,D	001 1101 1DDD DYYY	(AC),(Ry) <= (Ry) AND (D)		
EORI Y,D	001 1110 0DDD DYYY	(AC) <= (Ry) EOR (D)		
EORI* Y,D	001 1110 1DDD DYYY	(AC),(Ry) <= (Ry) EOR (D)		
ORI Y,D	001 1111 0DDD DYYY	(AC) <= (Ry) OR (D)		
ORI* Y,D	001 1111 1DDD DYYY	(AC),(Ry) <= (Ry) OR (D)		
MRW Y,X	011 100Y YYXX XXXX	(AC),(Ry) <= (Rx)		
MWR X,Y	011 110Y YYXX XXXX	(AC),(Rx) <= (Ry)		
LDS X,D	010 01DD DDXX XXXX	(AC),(Rx) <= (D)		
IPM X	010 0000 10XX XXXX	(AC),(Rx) <= Port(M)		
MAF X	011 0001 00XX XXXX	(AC),(Rx) <= STS1	TF2 : ZERO TF3 : CF	
MSB X	010 0010 00XX XXXX	(AC),(Rx) <= STS2	B0 : BCF B1 : SCF1(MPT) B2 : SCF2(HRF)	
MSC X	011 0000 00XX XXXX	(AC),(Rx) <= STS3	B0 : SCF4(INT) B1 : SCF5(TMR) B2 : PH15 B3 : SCF7(PDV)	
STA X	010 0010 10XX XXXX	(Rx) <= (AC)		
SR0 X	010 0011 00XX XXXX	(ACn),(Rxn) <= (Rxn+1) (AC3),(Rx3) <= 0		
SR1 X	010 0011 01XX XXXX	(ACn),(Rxn) <= (Rxn+1) (AC3),(Rx3) <= 1		
SL0 X	010 0011 10XX XXXX	(ACn),(Rxn) <= (Rxn-1) (AC0),(Rx0) <= 0		
SL1 X	010 0011 11XX XXXX	(ACn),(Rxn) <= (Rxn-1) (AC0),(Rx0) <= 1		
LDA X	011 0111 10XX XXXX	(AC) <= (Rx)		
JB0 X	100 00XX XXXX XXXX	(PC) <= X	if (AC0) = 1	
JB1 X	100 01XX XXXX XXXX	(PC) <= X	if (AC1) = 1	
JB2 X	100 10XX XXXX XXXX	(PC) <= X	if (AC2) = 1	
JB3 X	100 11XX XXXX XXXX	(PC) <= X	if (AC3) = 1	
JNZ X	101 00XX XXXX XXXX	(PC) <= X	if AC = 0	
JNC X	101 01XX XXXX XXXX	(PC) <= X	if (CF) = 0	
JZ X	101 10XX XXXX XXXX	(PC) <= X	if AC = 0	
JC X	101 11XX XXXX XXXX	(PC) <= X	if (CF) = 1	
JMP X	110 00XX XXXX XXXX	(PC) <= X		
CALL X	110 01XX XXXX XXXX	(STACK) <= (PC)+1 (PC) <= X		
RTS	110 1000 0000 0000	(PC) <= (STACK)		
SMS X	111 0000 000X 0000	SEF4 <= X4	M1-4 Enable	HRF0
TMS X	111 0010 00XX XXXX	TIMER <= X		HRF1
SF X	111 0100 0X00 00XX	X6 : M-PORT Pull-Low X1 : BCF Set X0 : CF Set		BCF CF
RF X	111 0110 0X00 00XX	X6 : M-PORT Low-L-H X1 : BCF Reset X0 : CF Reset		

# APLUS

# APU4006

Instruction		Machine Code	Function				Remark	Flag
ALM	X	111 0111 XXXX XXXX	X7,X6	0, 1	1, 0	1, 1		
			Signal	DC	1K/2K	4K Hz		
			Xn = 1	X5	X4	X3		
			Signal	1 Hz	2 Hz	4 Hz		
			Xn = 1	X2	X1	X0		
			Signal	8 Hz	16 Hz	32 Hz		
SIE	X	111 1000 XXXX XXXX	X5-7 : HEF1-3 is Enabled X0-3 : IEF0-3 is Enabled					
SIE*	X	111 1010 0000 XXXX	X0-3 : IEF0-3 is Enabled					
PLC	X	111 110X XXXX XXXX	X0-3 : Reset HRF0-3 X8 : Reset PH11-15					
HALT		111 1111 1111 1111						

## 6.5 Symbol Description

AC	: Accumulator	CF	: Carry Flag
ACn	: Accumulator Bit N	BCF	: Backup Flag
Rx	: Memory of Address X	IEFn	: Interrupt Enable Flag
Rxn	: Memory Bit N of Address X	HEFn	: Halt Release Enable Flag
Ry	: Memory of Working Register Y	HRFn	: Halt Release Flag
D	: Immediate Data	SCFn	: Start Condition Flag
PC	: Program Counter	Ly	: LCD Latch