

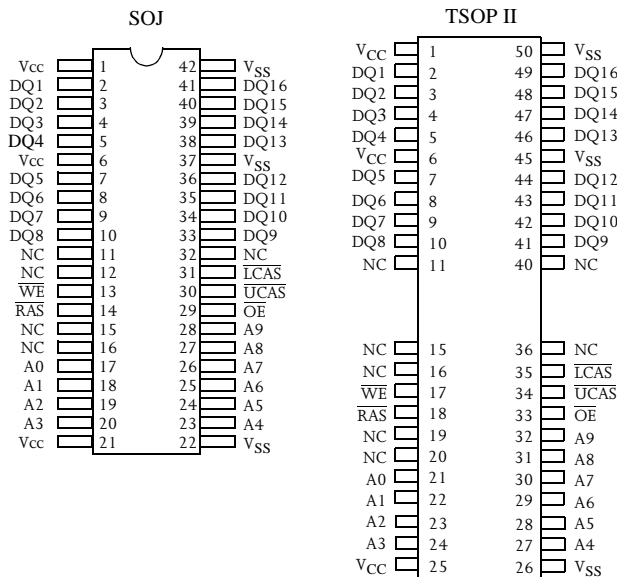


3V 1M×16 CMOS DRAM (EDO)

Features

- Organization: 1,048,576 words × 16 bits
- High speed
 - 50/60 ns $\overline{\text{RAS}}$ access time
 - 20/25 ns hyper page cycle time
 - 12/15 ns $\overline{\text{CAS}}$ access time
- Low power consumption
 - Active: 500 mW max (-60)
 - Standby: 3.6 mW max, CMOS DQ
- Extended data out
- 1024 refresh cycles, 16 ms refresh interval
 - $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh or self-refresh
- Read-modify-write
- TTL-compatible, three-state DQ
- JEDEC standard package and pinout
 - 400 mil, 42-pin SOJ
 - 400 mil, 44/50-pin TSOP II
- 3V power supply (AS4LC1M16E5)
- 5V tolerant I/Os; 5.5V maximum V_{IH}
- Industrial and commercial temperature available

Pin arrangement



Pin designation

| Pin(s) | Description |
|--------------------------|-----------------------------------|
| A0 to A9 | Address inputs |
| $\overline{\text{RAS}}$ | Row address strobe |
| DQ1 to DQ16 | Input/output |
| $\overline{\text{OE}}$ | Output enable |
| $\overline{\text{WE}}$ | Write enable |
| $\overline{\text{UCAS}}$ | Column address strobe, upper byte |
| $\overline{\text{LCAS}}$ | Column address strobe, lower byte |
| V_{CC} | Power |
| V_{SS} | Ground |

Selection guide

| | Symbol | -50 | -60 | Unit |
|--------------------------------------------------------------|-----------|-----|-----|------|
| Maximum $\overline{\text{RAS}}$ access time | t_{RAC} | 50 | 60 | ns |
| Maximum column address access time | t_{AA} | 25 | 30 | ns |
| Maximum $\overline{\text{CAS}}$ access time | t_{CAC} | 10 | 12 | ns |
| Maximum output enable ($\overline{\text{OE}}$) access time | t_{OEA} | 10 | 12 | ns |
| Minimum read or write cycle time | t_{RC} | 80 | 100 | ns |
| Minimum hyper page mode cycle time | t_{HPC} | 20 | 25 | ns |
| Maximum operating current | I_{CC1} | 140 | 120 | mA |
| Maximum CMOS standby current | I_{CC5} | 1.0 | 1.0 | mA |

Shaded areas indicate advance information.



Functional description

The AS4LC1M16E5 is a high performance 16-megabit CMOS Dynamic Random Access Memory (DRAM) organized as 1,048,576 words \times 16 bits. The device is fabricated using advanced CMOS technology and innovative design techniques resulting in high speed, extremely low power and wide operating margins at component and system levels. The Alliance 16Mb DRAM family is optimized for use as main memory in personal and portable PCs, workstations, and multimedia and router switch applications.

The AS4LC1M16E5 features hyper page mode operation where read and write operations within a single row (or page) can be executed at very high speed by toggling column addresses within that row. Row and column addresses are alternately latched into input buffers using the falling edge of $\overline{\text{RAS}}$ and $\overline{\text{xCAS}}$ inputs, respectively. Also, $\overline{\text{RAS}}$ is used to make the column address latch transparent, enabling application of column addresses prior to $\overline{\text{xCAS}}$ assertion. The AS4LC1M16E5 provides dual $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ for independent byte control of read and write access.

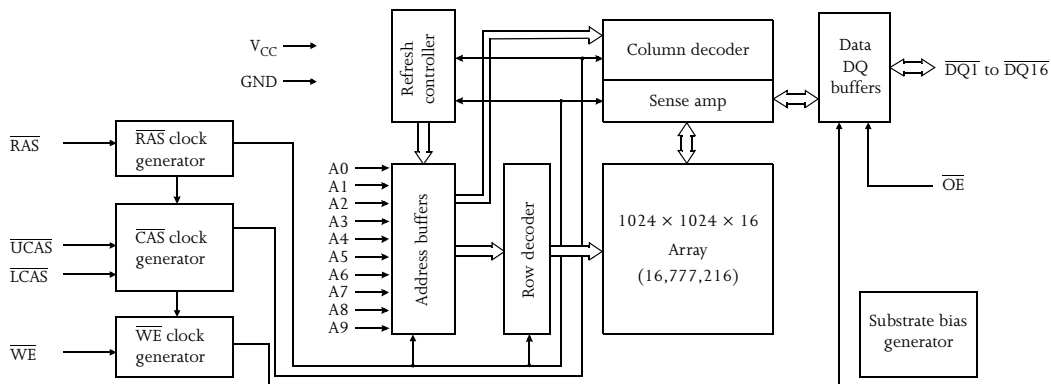
Extended data out (EDO), also known as 'hyper-page mode,' enables high speed operation. In contrast to 'fast-page mode' devices, data remains active on outputs after $\overline{\text{xCAS}}$ is de-asserted high, giving system logic more time to latch the data. Use $\overline{\text{OE}}$ and $\overline{\text{WE}}$ to control output impedance and prevent bus contention during read-modify-write and shared bus applications. Outputs also go to high impedance at the last occurrence of $\overline{\text{RAS}}$ and $\overline{\text{xCAS}}$ going high.

Refresh on the 1024 address combinations of A0 to A9 must be performed every 16 ms using:

- $\overline{\text{RAS}}$ -only refresh: $\overline{\text{RAS}}$ is asserted while $\overline{\text{xCAS}}$ is held high. Each of the 1024 rows must be strobed. Outputs remain high impedance.
- Hidden refresh: $\overline{\text{xCAS}}$ is held low while $\overline{\text{RAS}}$ is toggled. Outputs remain low impedance with previous valid data.
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh (CBR): At least one $\overline{\text{xCAS}}$ is asserted prior to $\overline{\text{RAS}}$. Refresh address is generated internally. Outputs are high-impedance ($\overline{\text{OE}}$ and $\overline{\text{WE}}$ are don't care).
- Normal read or write cycles refresh the row being accessed.
- Self-refresh cycles

The AS4LC1M16E5 is available in the standard 42-pin plastic SOJ and 44/50-pin TSOP II packages, respectively. The AS4LC1M16E5 device operates with a single power supply of $3\text{V} \pm 0.3\text{V}$ and provides TTL compatible inputs and outputs.

Logic block diagram



Recommended operating conditions

| Parameter | Symbol | Min | Nominal | Max | Unit |
|-------------------------------|------------|------------------|---------|-----|--------------------|
| Supply voltage | V_{CC} | 3.0 | 3.3 | 3.6 | V |
| | GND | 0.0 | 0.0 | 0.0 | V |
| Input voltage | V_{IH} | 2.0 | – | 5.5 | V |
| | V_{IL} | -0.5^{\dagger} | – | 0.8 | V |
| Ambient operating temperature | Commercial | 0 | – | 70 | $^{\circ}\text{C}$ |
| | Industrial | T_A | –40 | – | 85 |

$^{\dagger}V_{IL}$ min -3.0V for pulse widths less than 5 ns.

Recommended operating conditions apply throughout this document unless otherwise specified.



Absolute maximum ratings

| Parameter | Symbol | Min | Max | Unit |
|-------------------------------|--------------|------|----------|----------|
| Input voltage | V_{DQ} | -1.0 | +5.5 | V |
| Power supply voltage | V_{CC} | -1.0 | +4.0 | V |
| Storage temperature (plastic) | T_{STG} | -65 | +150 | °C |
| Soldering temperature × time | T_{SOLDER} | – | 260 × 10 | °C × sec |
| Power dissipation | P_D | – | 0.6 | W |
| Short circuit output current | I_{out} | – | 50 | mA |

Truth table

| Operation | \overline{RAS} | \overline{LCAS} | \overline{UCAS} | \overline{WE} | \overline{OE} | Addresses | | DQ0 to DQ15 | Notes | |
|-------------------------------|------------------|-------------------|-------------------|-----------------|-----------------|-----------|-------|-----------------------------------------|-------------------|-----|
| | | | | | | t_R | t_C | | | |
| Standby | H | H to X | H to X | X | X | X | X | High-Z | | |
| Word read | L | L | L | H | L | ROW | COL | Data out | | |
| Lower byte read | L | L | H | H | L | ROW | COL | Lower byte, Upper byte, Data out | | |
| Upper byte read | L | H | L | H | L | ROW | COL | Lower byte, Data out, Upper byte | | |
| Word (early) write | L | L | L | L | X | ROW | COL | Data in | | |
| Lower byte (early) write | L | L | H | L | X | ROW | COL | Lower byte, Data in, Upper byte, High-Z | | |
| Upper byte (early) write | L | H | L | L | X | ROW | COL | Lower byte, High-Z, Upper byte, Data in | | |
| Read write | L | L | L | H to L | L to H | ROW | COL | Data out, Data in | 1,2 | |
| EDO read | 1st cycle | L | H to L | H to L | H | L | ROW | COL | Data out | 2 |
| | 2nd cycle | L | H to L | H to L | H | L | n/a | COL | Data out | 2 |
| | Any cycle | L | L to H | L to H | H | L | n/a | n/a | Data out | 2 |
| EDO write | 1st cycle | L | H to L | H to L | L | X | ROW | COL | Data in | 1 |
| | 2nd cycle | L | H to L | H to L | L | X | n/a | COL | Data in | 1 |
| EDO read write | 1st cycle | L | H to L | H to L | H to L | L to H | ROW | COL | Data out, Data in | 1,2 |
| | 2nd cycle | L | H to L | H to L | H to L | L to H | n/a | COL | Data out, Data in | 1,2 |
| \overline{RAS} only refresh | L | H | H | X | X | ROW | n/a | High Z | | |
| CBR refresh | H to L | L | L | H | X | X | X | High Z | 3 | |
| Self refresh | H to L | L | L | H | X | X | X | High Z | 3 | |



DC electrical characteristics

| Parameter | Symbol | Test conditions | -50 | | -60 | | Unit | Notes |
|---------------------------------------------------------------------------|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|-----|---------------|-------|
| | | | Min | Max | Min | Max | | |
| Input leakage current | I_{IL} | $0V \leq V_{in} \leq V_{CC} \text{ (max)}$ Pins not under test = 0V | -2 | +2 | -2 | +2 | μA | |
| Output leakage current | I_{OL} | D_{OUT} disabled, $0V \leq V_{out} \leq V_{CC} \text{ (max)}$ | -2 | +2 | -2 | +2 | μA | |
| Operating power supply current | I_{CC1} | $\overline{\text{RAS}}$, $\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$, Address cycling; $t_{RC} = \text{min}$ | - | 140 | - | 130 | mA | 4, 5 |
| TTL standby power supply current | I_{CC2} | $\overline{\text{RAS}} = \overline{\text{UCAS}} = \overline{\text{LCAS}} \geq V_{IH}$, all other inputs at V_{IH} or V_{IL} | - | 2.0 | - | 2.0 | mA | |
| Average power supply current, $\overline{\text{RAS}}$ refresh mode or CBR | I_{CC3} | $\overline{\text{RAS}}$ cycling, $\overline{\text{UCAS}} = \overline{\text{LCAS}} \geq V_{IH}$, $t_{RC} = \text{min}$ of $\overline{\text{RAS}}$ low after $\overline{\text{XCAS}}$ low. | - | 80 | - | 70 | mA | 4 |
| EDO page mode average power supply current | I_{CC4} | $\overline{\text{RAS}} = V_{IL}$, $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$, address cycling: $t_{HPC} = \text{min}$ | - | 85 | - | 75 | mA | 4, 5 |
| CMOS standby power supply current | I_{CC5} | $\overline{\text{RAS}} = \overline{\text{UCAS}} = \overline{\text{LCAS}} = V_{CC} - 0.2V$, $F = 0$ | - | 1 | - | 1 | mA | |
| Output voltage | V_{OH} | $I_{OUT} = -5.0 \text{ mA}$ | 2.4 | - | 2.4 | - | V | |
| | V_{OL} | $I_{OUT} = 4.2 \text{ mA}$ | - | 0.4 | - | 0.4 | V | |
| $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current | I_{CC6} | $\overline{\text{RAS}}$, $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ cycling, $t_{RC} = \text{min}$ | - | 80 | - | 70 | mA | |
| Self refresh current | I_{CC7} | $\overline{\text{RAS}} = \overline{\text{UCAS}} = \overline{\text{LCAS}} \leq 0.2V$, $\overline{\text{WE}} = \overline{\text{OE}} \geq V_{CC} - 0.2V$, all other inputs at 0.2V or $V_{CC} - 0.2V$ | - | 0.5 | - | 0.5 | mA | |

Shaded areas indicate advance information.



AC parameters common to all waveforms

| Symbol | Parameter | -50 | | -60 | | Unit | Notes |
|-----------|-----------------------------------------------------|-----|-----|-----|-----|------|-------|
| | | Min | Max | Min | Max | | |
| t_{RC} | Random read or write cycle time | 80 | – | 100 | – | ns | |
| t_{RP} | \overline{RAS} precharge time | 30 | – | 40 | – | ns | |
| t_{RAS} | \overline{RAS} pulse width | 50 | 10K | 60 | 10K | ns | |
| t_{CAS} | \overline{CAS} pulse width | 8 | 10K | 10 | 10K | ns | |
| t_{RCD} | \overline{RAS} to \overline{CAS} delay time | 15 | 35 | 15 | 43 | ns | 9 |
| t_{RAD} | \overline{RAS} to column address delay time | 9 | 25 | 10 | 30 | ns | 10 |
| t_{RSH} | \overline{CAS} to \overline{RAS} hold time | 10 | – | 10 | – | ns | |
| t_{CSH} | \overline{RAS} to \overline{CAS} hold time | 40 | – | 50 | – | ns | |
| t_{CRP} | \overline{CAS} to \overline{RAS} precharge time | 5 | – | 5 | – | ns | |
| t_{ASR} | Row address setup time | 0 | – | 0 | – | ns | |
| t_{RAH} | Row address hold time | 8 | – | 10 | – | ns | |
| t_T | Transition time (rise and fall) | 1 | 50 | 1 | 50 | ns | 7,8 |
| t_{REF} | Refresh period | – | 16 | – | 16 | ms | 6 |
| t_{CP} | CAS precharge time | 8 | – | 10 | – | ns | |
| t_{RAL} | Column address to \overline{RAS} lead time | 25 | – | 30 | – | ns | |
| t_{ASC} | Column address setup time | 0 | – | 0 | – | ns | |
| t_{CAH} | Column address hold time | 8 | – | 10 | – | ns | |

Shaded areas indicate advance information.

Read cycle

| Symbol | Parameter | -50 | | -60 | | Unit | Notes |
|-----------|--------------------------------------------|-----|-----|-----|-----|------|-------|
| | | Min | Max | Min | Max | | |
| t_{RAC} | Access time from \overline{RAS} | – | 50 | – | 60 | ns | 9 |
| t_{CAC} | Access time from \overline{CAS} | – | 12 | – | 15 | ns | 9,16 |
| t_{AA} | Access time from address | – | 25 | – | 30 | ns | 10,16 |
| t_{RCS} | Read command setup time | 0 | – | 0 | – | ns | |
| t_{RCH} | Read command hold time to \overline{CAS} | 0 | – | 0 | – | ns | 12 |
| t_{RRH} | Read command hold time to \overline{RAS} | 0 | – | 0 | – | ns | 12 |

Shaded areas indicate advance information.



Write cycle

| Symbol | Parameter | -50 | | -60 | | Unit | Notes |
|-----------|---------------------------------------------|-----|-----|-----|-----|------|-------|
| | | Min | Max | Min | Max | | |
| t_{WCS} | Write command setup time | 0 | – | 0 | – | ns | 14 |
| t_{WCH} | Write command hold time | 10 | – | 10 | – | ns | 14 |
| t_{WP} | Write command pulse width | 10 | – | 10 | – | ns | |
| t_{RWL} | Write command to \overline{RAS} lead time | 10 | – | 10 | – | ns | |
| t_{CWL} | Write command to \overline{CAS} lead time | 8 | – | 10 | – | ns | |
| t_{DS} | Data-in setup time | 0 | – | 0 | – | ns | 15 |
| t_{DH} | Data-in hold time | 8 | – | 10 | – | ns | 15 |

Shaded areas indicate advance information.

Read-modify-write cycle

| Symbol | Parameter | -50 | | -60 | | Unit | Notes |
|-----------|------------------------------------------------|-----|-----|-----|-----|------|-------|
| | | Min | Max | Min | Max | | |
| t_{RWC} | Read-write cycle time | 113 | – | 135 | – | ns | |
| t_{RWD} | \overline{RAS} to \overline{WE} delay time | 67 | – | 77 | – | ns | 14 |
| t_{CWD} | \overline{CAS} to \overline{WE} delay time | 32 | – | 35 | – | ns | 14 |
| t_{AWD} | Column address to \overline{WE} delay time | 42 | – | 47 | – | ns | 14 |

Shaded areas indicate advance information.

Refresh cycle

| Symbol | Parameter | -50 | | -60 | | Unit | Notes |
|-----------|----------------------------------------------------------------------------|-----|-----|-----|-----|------|-------|
| | | Min | Max | Min | Max | | |
| t_{CSR} | \overline{CAS} setup time (\overline{CAS} -before- \overline{RAS}) | 5 | – | 5 | – | ns | 6 |
| t_{CHR} | \overline{CAS} hold time (\overline{CAS} -before- \overline{RAS}) | 8 | – | 10 | – | ns | 6 |
| t_{RPC} | \overline{RAS} precharge to \overline{CAS} hold time | 0 | – | 0 | – | ns | |
| t_{CPT} | \overline{CAS} precharge time (CBR counter test) | 10 | – | 10 | – | ns | |

Shaded areas indicate advance information.



Hyper page mode cycle

| Symbol | Parameter | -50 | | -60 | | Unit | Notes |
|-------------|----------------------------------------------------------|-----|------|-----|------|------|-------|
| | | Min | Max | Min | Max | | |
| t_{CPWD} | \overline{CAS} precharge to \overline{WE} delay time | 45 | – | 52 | – | ns | |
| t_{CPA} | Access time from \overline{CAS} precharge | – | 28 | – | 35 | ns | 16 |
| t_{RASP} | \overline{RAS} pulse width | 50 | 100K | 60 | 100K | ns | |
| t_{DOH} | Previous data hold time from \overline{CAS} | 5 | – | 5 | – | ns | |
| t_{REZ} | Output buffer turn off delay from \overline{RAS} | 0 | 13 | 0 | 15 | ns | |
| t_{WEZ} | Output buffer turn off delay from \overline{WE} | 0 | 13 | 0 | 15 | ns | |
| t_{OEZ} | Output buffer turn off delay from \overline{OE} | 0 | 13 | 0 | 15 | ns | |
| t_{HPC} | Hyper page mode cycle time | 20 | – | 25 | – | ns | |
| t_{HPRWC} | Hyper page mode RMW cycle | 47 | – | 56 | – | ns | |
| t_{RHCP} | \overline{RAS} hold time from \overline{CAS} | 30 | – | 35 | – | ns | |

Shaded areas indicate advance information.

Output enable

| Symbol | Parameter | -50 | | -60 | | Unit | Notes |
|-----------|----------------------------------------------------------|-----|-----|-----|-----|------|-------|
| | | Min | Max | Min | Max | | |
| t_{CLZ} | \overline{CAS} to output in Low Z | 0 | – | 0 | – | ns | 11 |
| t_{ROH} | \overline{RAS} hold time referenced to \overline{OE} | 8 | – | 10 | – | ns | |
| t_{OEA} | \overline{OE} access time | – | 13 | – | 15 | ns | |
| t_{OED} | \overline{OE} to data delay | 13 | – | 15 | – | ns | |
| t_{OEZ} | Output buffer turnoff delay from \overline{OE} | 0 | 13 | 0 | 15 | ns | 11 |
| t_{OEH} | \overline{OE} command hold time | 10 | – | 10 | – | ns | |
| t_{OLZ} | \overline{OE} to output in Low Z | 0 | – | 0 | – | ns | |
| t_{OFF} | Output buffer turn-off time | 0 | 13 | 0 | 15 | ns | 11,13 |

Shaded areas indicate advance information.

Self refresh cycle

| Std Symbol | Parameter | -50 | | -60 | | Unit | Notes |
|------------|-------------------------------------------------------|-----|-----|-----|-----|---------|-------|
| | | Min | Max | Min | Max | | |
| t_{RASS} | \overline{RAS} pulse width (CBR self refresh) | 100 | – | 100 | – | μ s | |
| t_{RPS} | \overline{RAS} precharge time (CBR self refresh) | 90 | – | 105 | – | ns | |
| t_{CHS} | \overline{CAS} hold time (CBR self refresh) | 8 | – | 10 | – | ns | |

Shaded areas indicate advance information.



Notes

- 1 Write cycles may be byte write cycles (either $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$ active).
- 2 Read cycles may be byte read cycles (either $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$ active).
- 3 One $\overline{\text{CAS}}$ must be active (either $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$).
- 4 I_{CC1} , I_{CC3} , I_{CC4} , and I_{CC6} are dependent on frequency.
- 5 I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
- 6 An initial pause of 200 μs is required after power-up followed by any 8 $\overline{\text{RAS}}$ cycles before proper device operation is achieved. In the case of an internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ initialization cycles instead of 8 $\overline{\text{RAS}}$ cycles are required. 8 initialization cycles are required after extended periods of bias without clocks (greater than 8 ms).
- 7 AC Characteristics assume $t_{\text{T}} = 2$ ns. All AC parameters are measured with a load as described in AC test conditions below.
- 8 V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} .
- 9 Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC} .
- 10 Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA} .
- 11 Assumes three state test load (5 pF and a 380 Ω Thevenin equivalent).
- 12 Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
- 13 t_{OFF} (max) defines the time at which the output achieves the open circuit condition; it is not referenced to output voltage levels. t_{OFF} is referenced from rising edge of $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$, whichever occurs last.
- 14 t_{WCS} , t_{WCH} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the datasheet as electrical characteristics only. If $t_{\text{WS}} \geq t_{\text{WS}}$ (min) and $t_{\text{WH}} \geq t_{\text{WH}}$ (min), the cycle is an early write cycle and data out pins will remain open circuit, high impedance, throughout the cycle. If $t_{\text{RWD}} \geq t_{\text{RWD}}$ (min), $t_{\text{CWD}} \geq t_{\text{CWD}}$ (min) and $t_{\text{AWD}} \geq t_{\text{AWD}}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data out at access time is indeterminate.
- 15 These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in read-write cycles.
- 16 Access time is determined by the longest of t_{CAA} or t_{CAC} or t_{CPA}
- 17 $t_{\text{ASC}} \geq t_{\text{CP}}$ to achieve t_{PC} (min) and t_{CPA} (max) values.
- 18 These parameters are sampled and not 100% tested.

AC test conditions

- Access times are measured with output reference levels of $V_{\text{OH}} = 2.4\text{V}$ and $V_{\text{OL}} = 0.4\text{V}$, $V_{\text{IH}} = 2.0\text{V}$ and $V_{\text{IL}} = 0.8\text{V}$
- Input rise and fall times: 2 ns

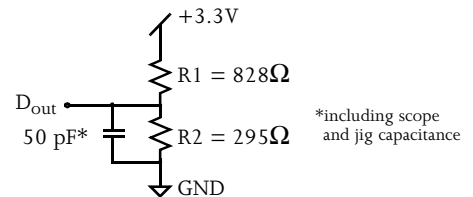


Figure B: Equivalent output load (AS4LC1M16E5)

Key to switching waveforms



Rising input



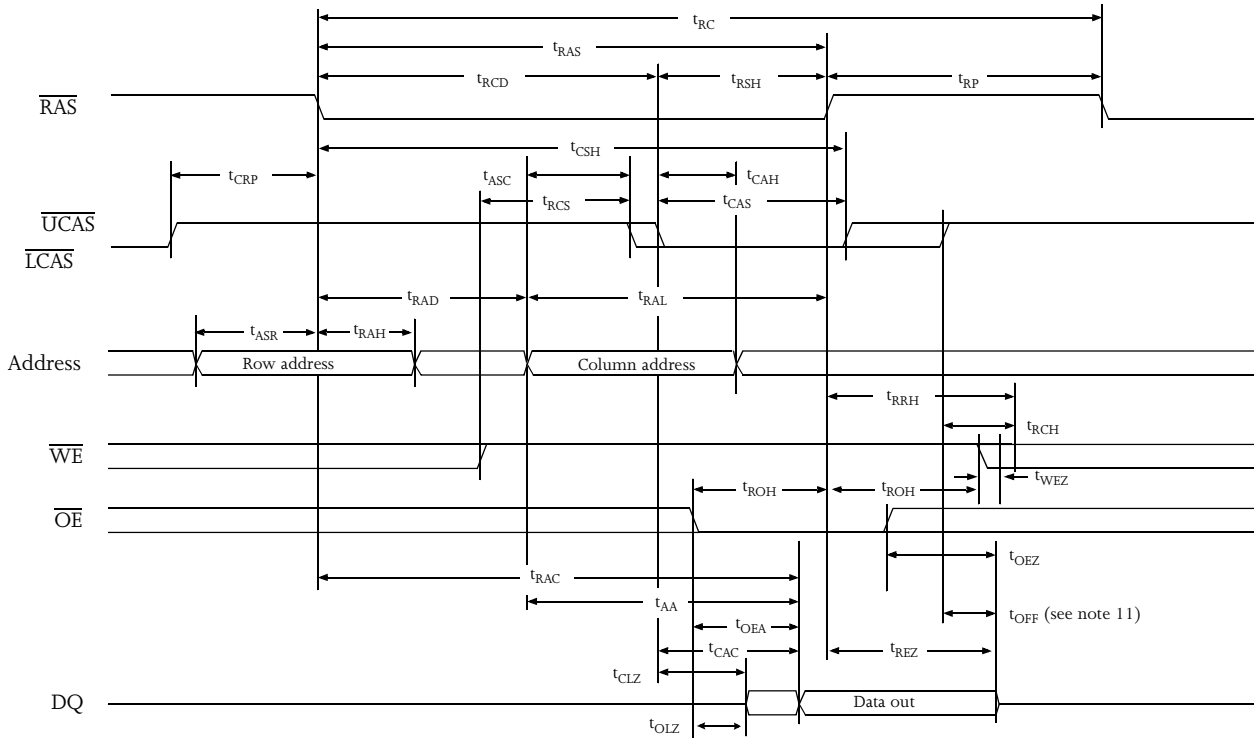
Falling input



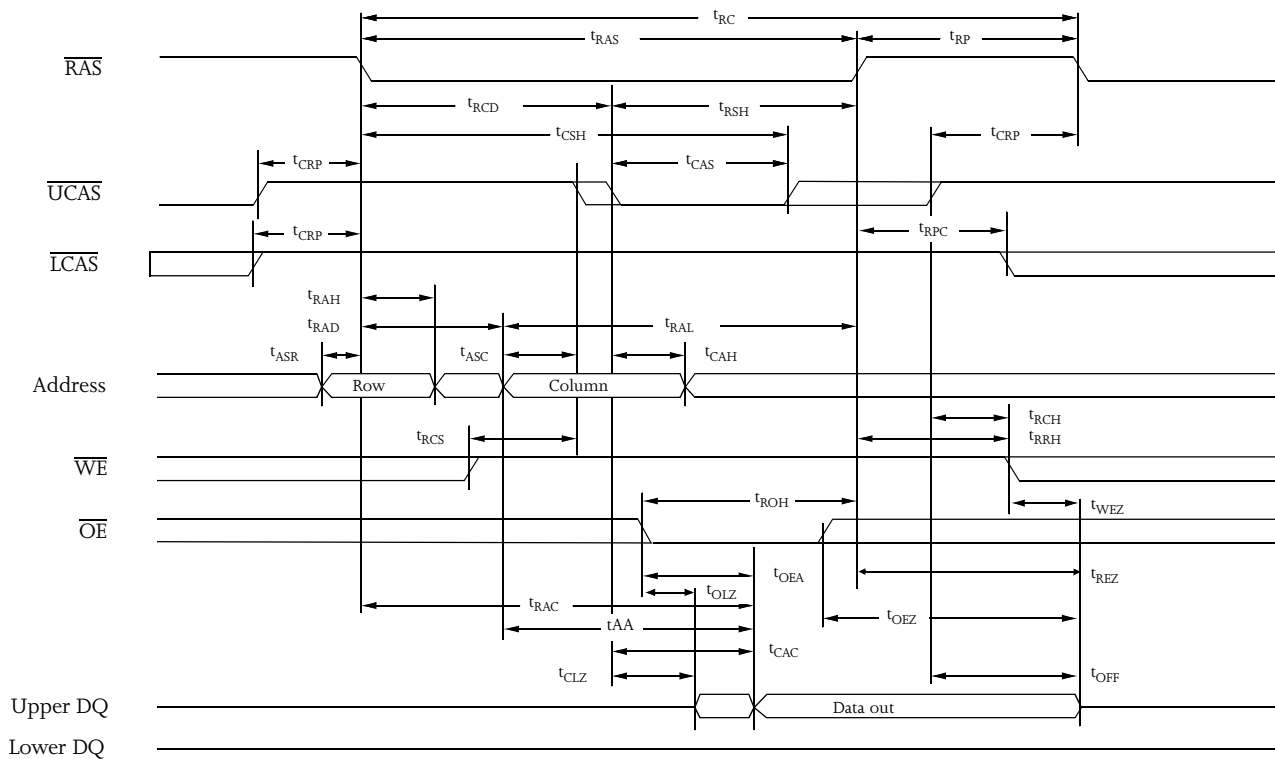
Undefined output/don't care



Read waveform

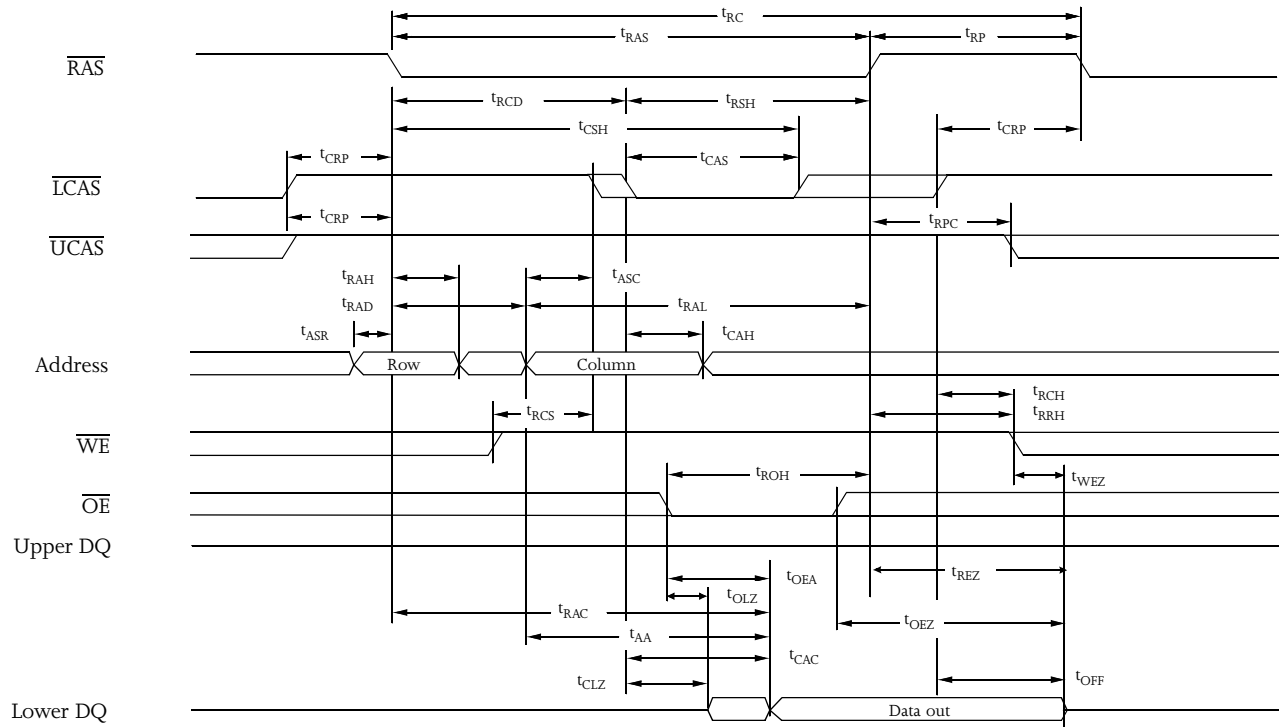


Upper byte read waveform

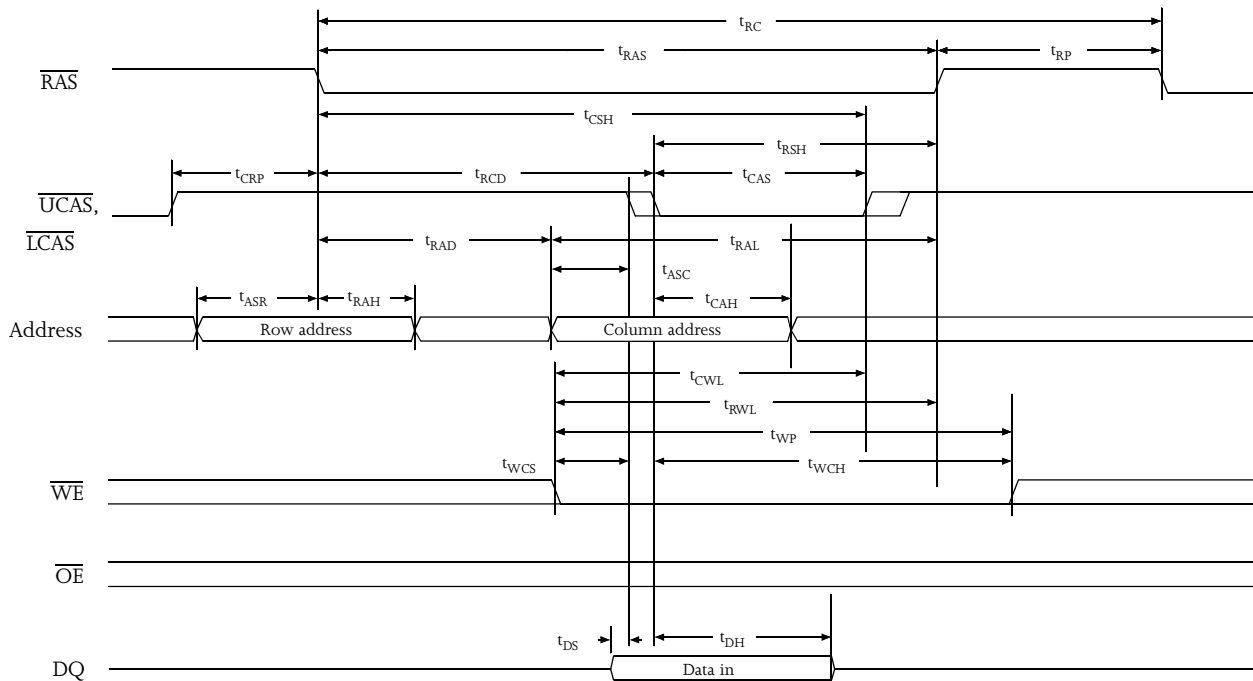




Lower byte read waveform

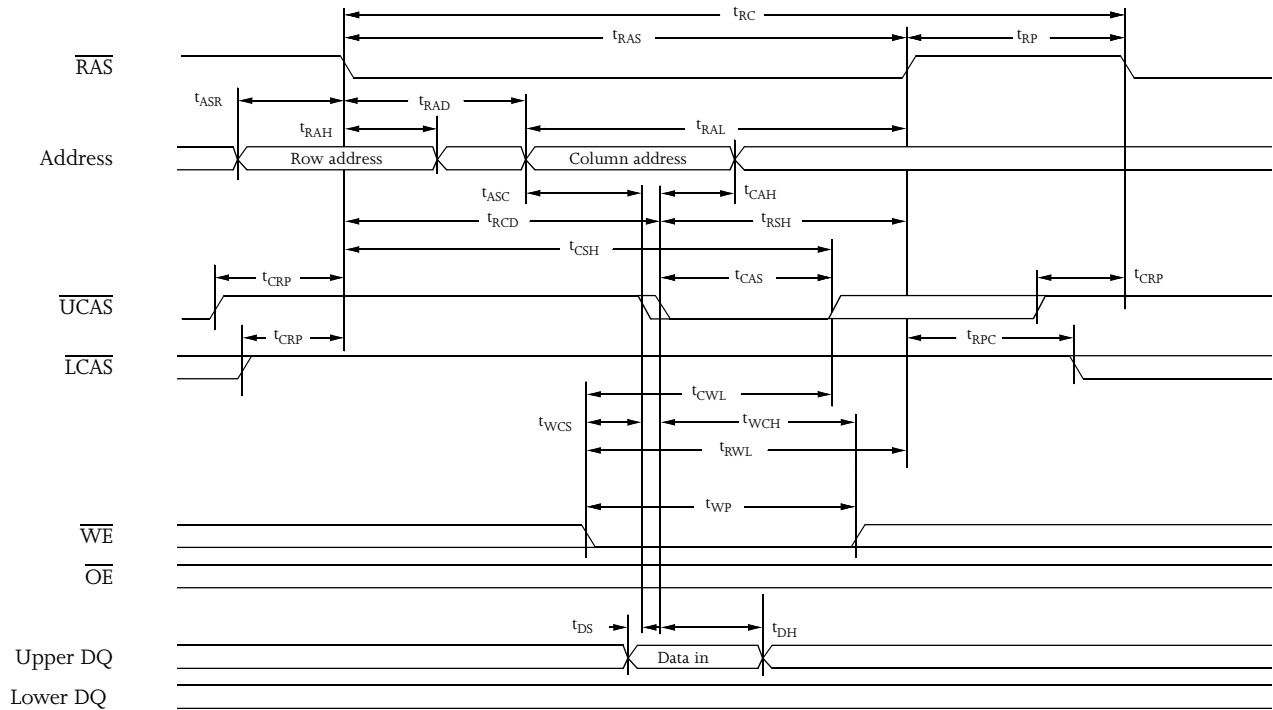


Early write waveform

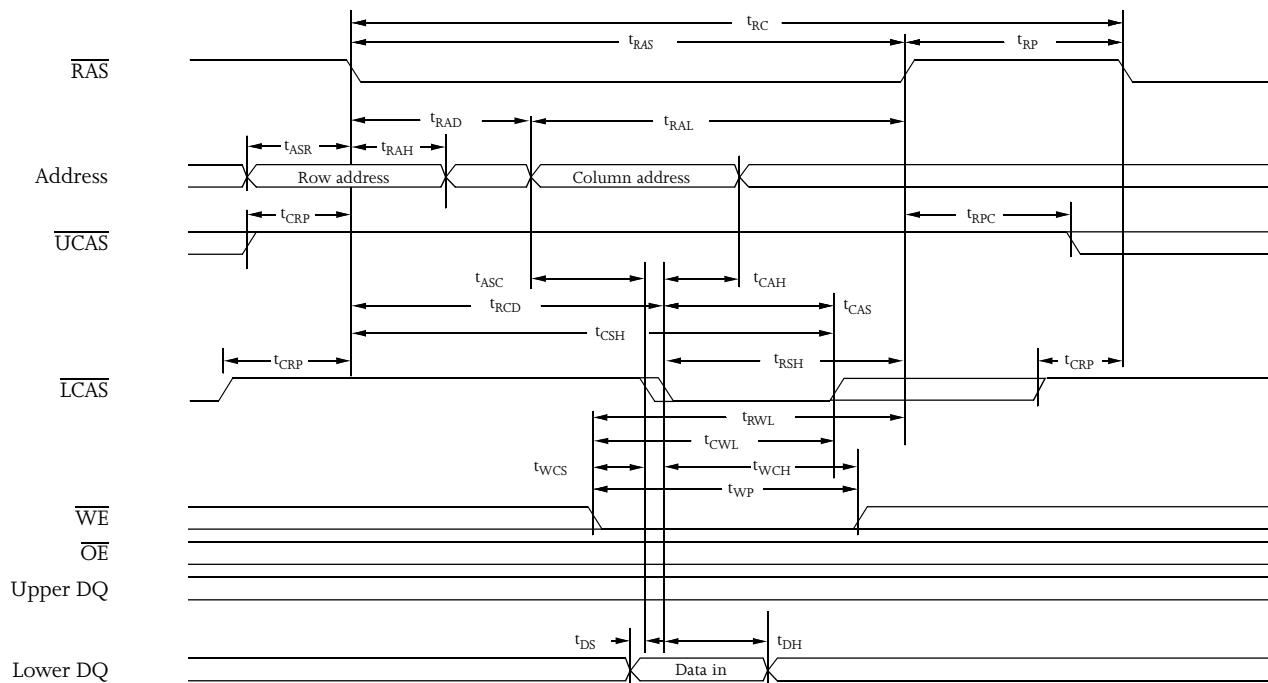




Upper byte early write waveform



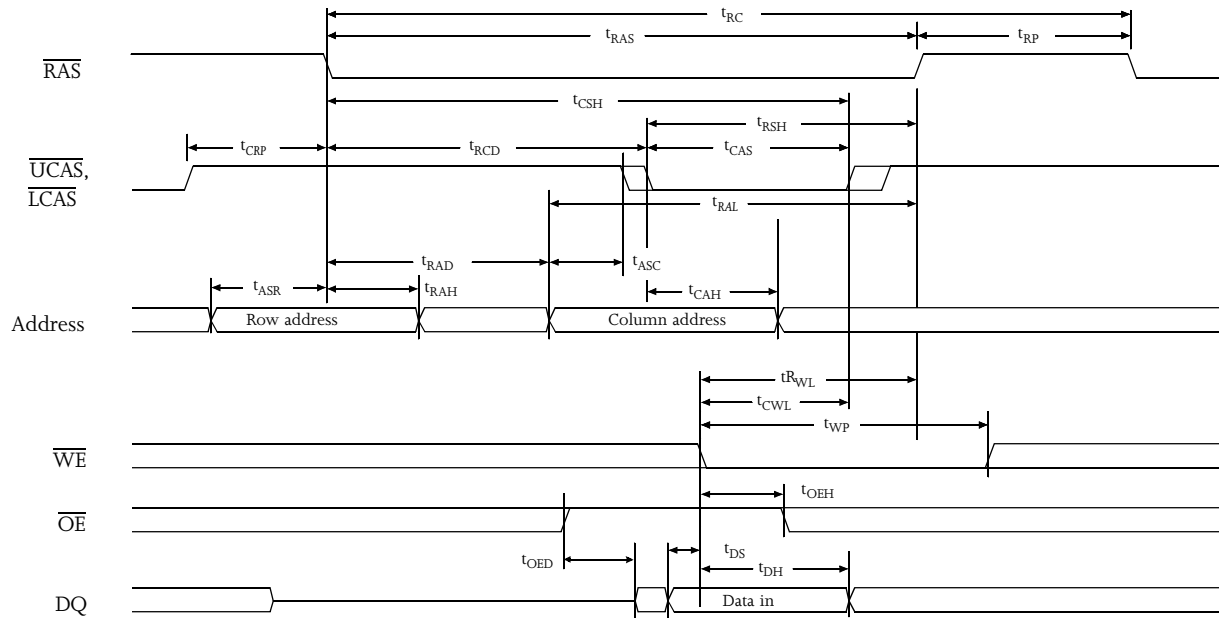
Lower byte early write waveform





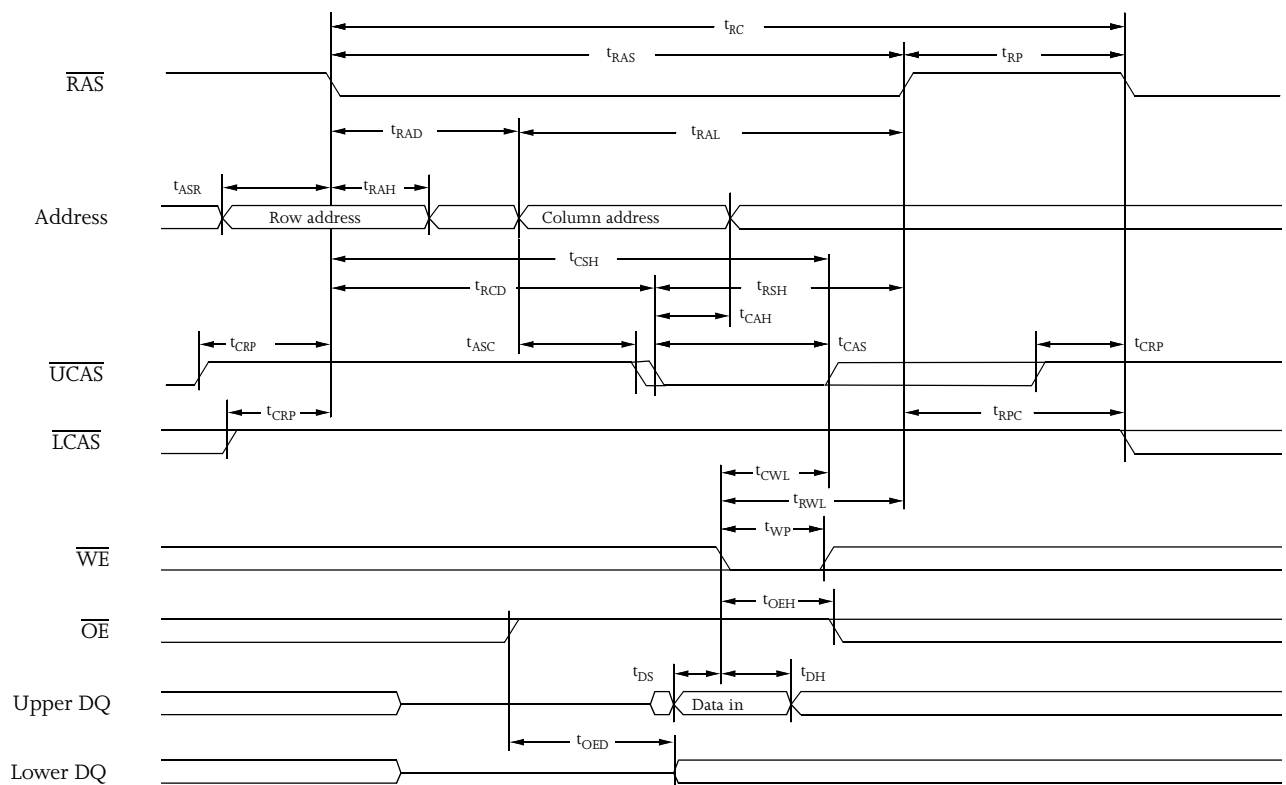
Write waveform

\overline{OE} controlled



Upper byte write waveform

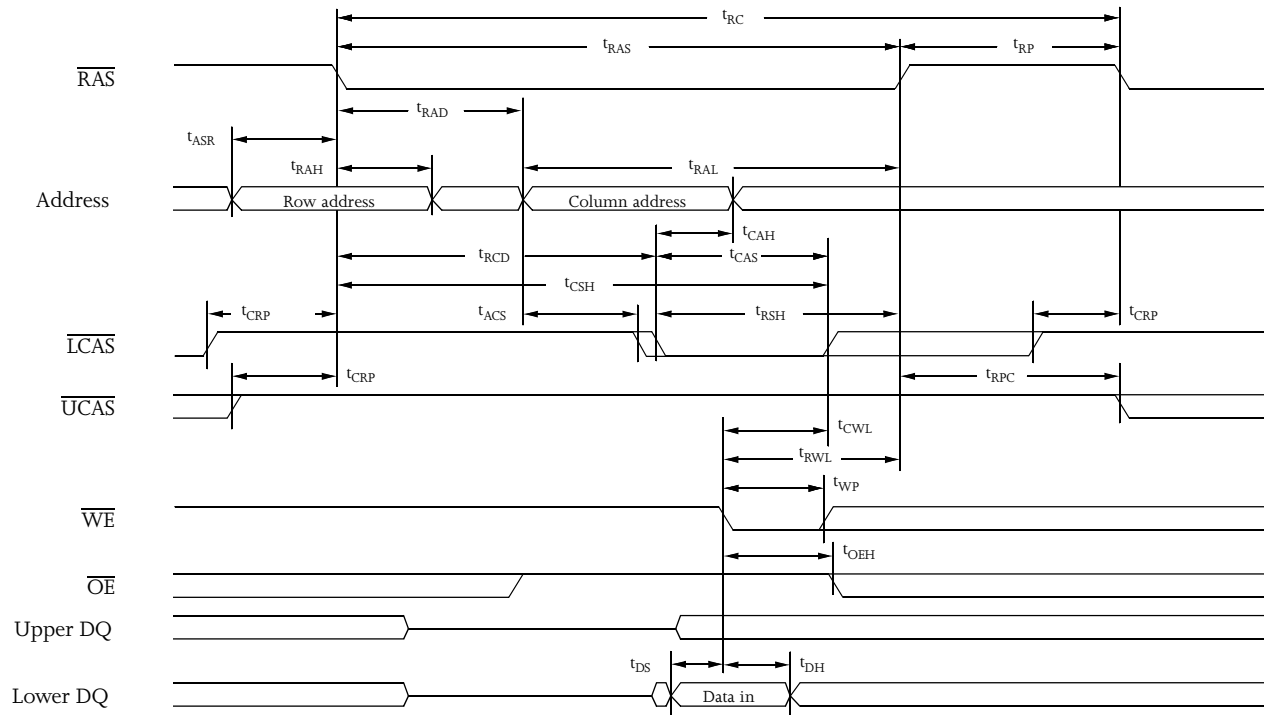
\overline{OE} controlled



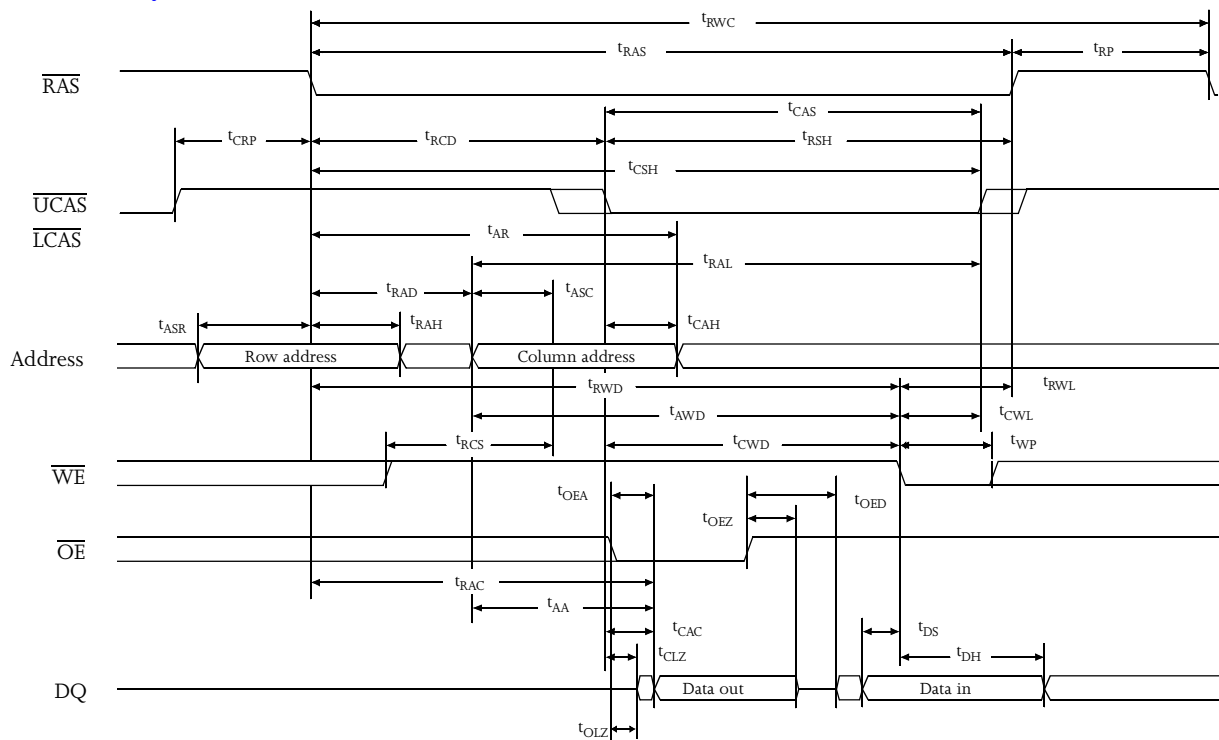


Lower byte write waveform

\overline{OE} controlled

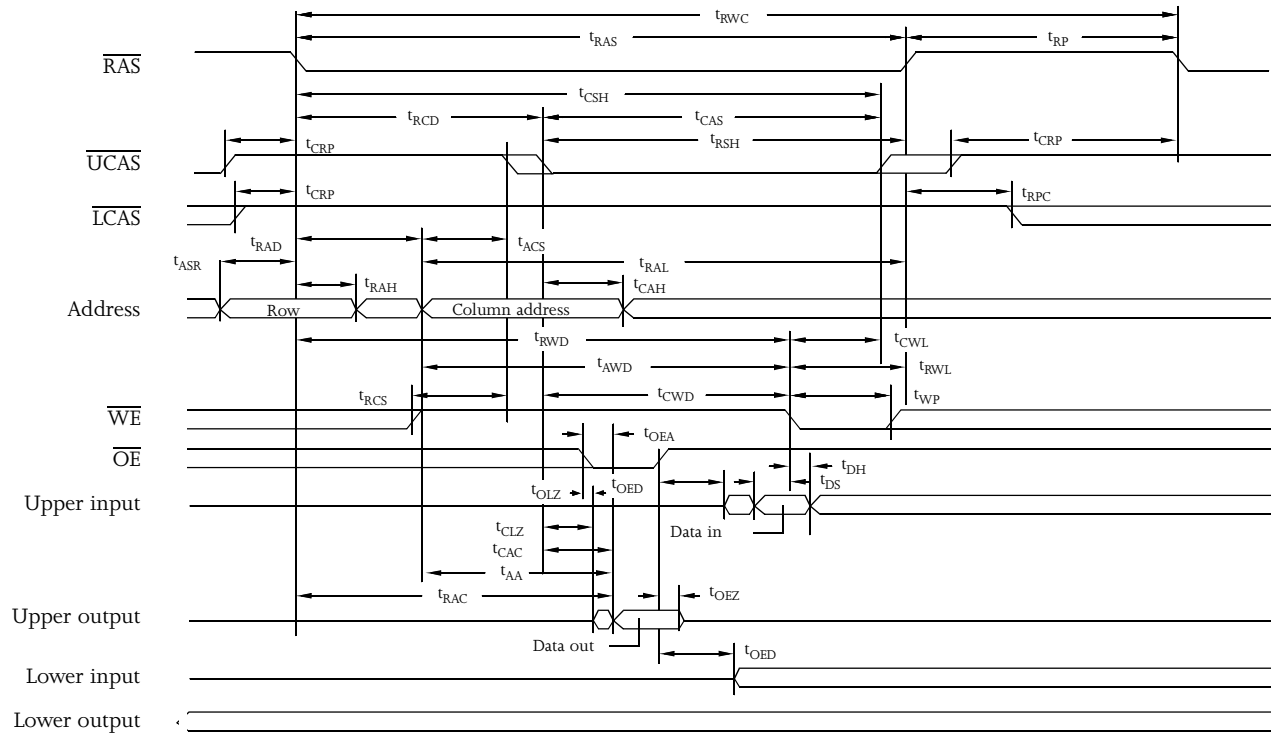


Read-modify-write waveform

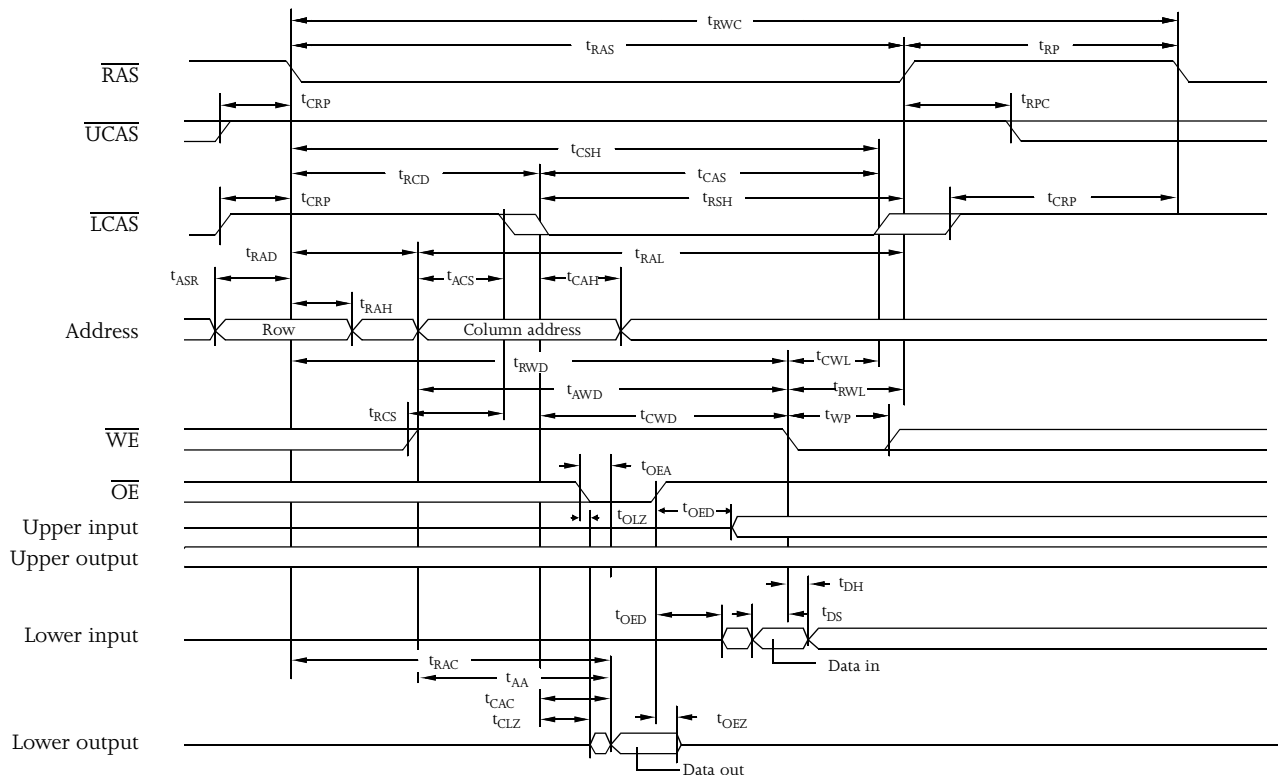




Upper byte read-modify-write waveform

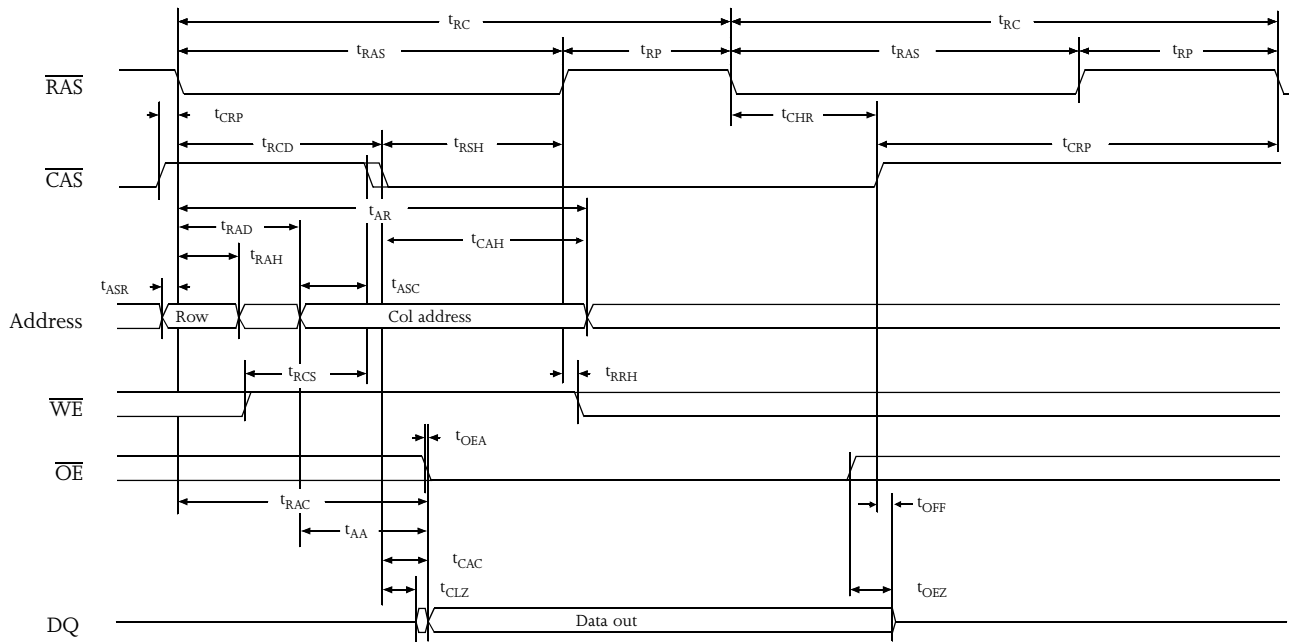


Lower byte read-modify-write waveform

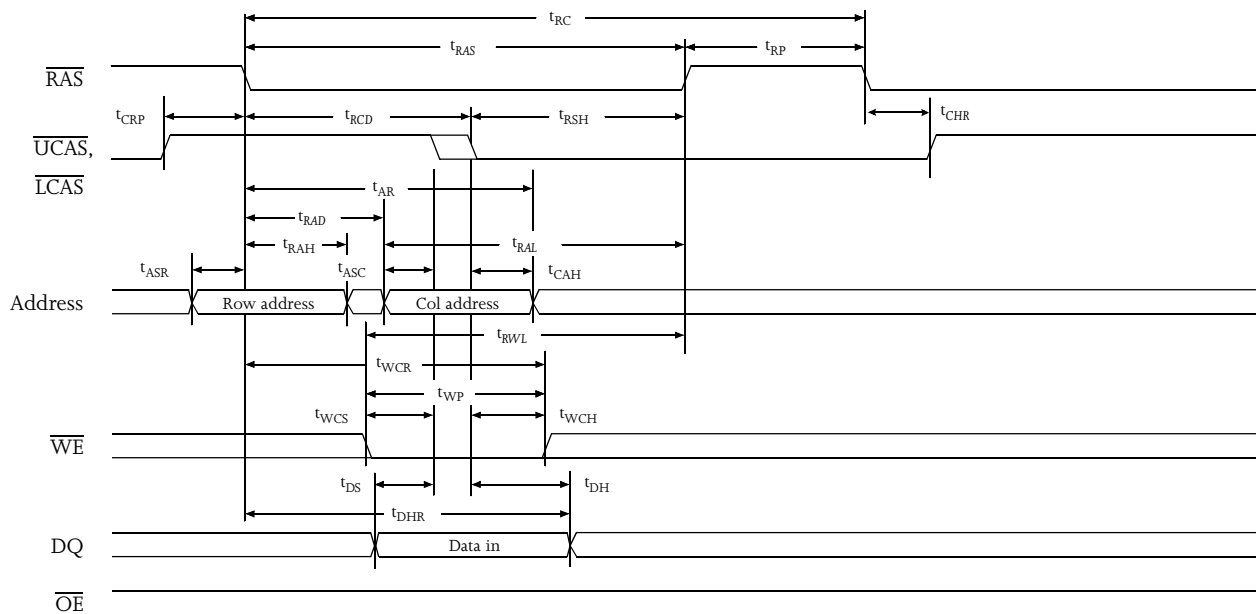




Hidden refresh waveform (read)

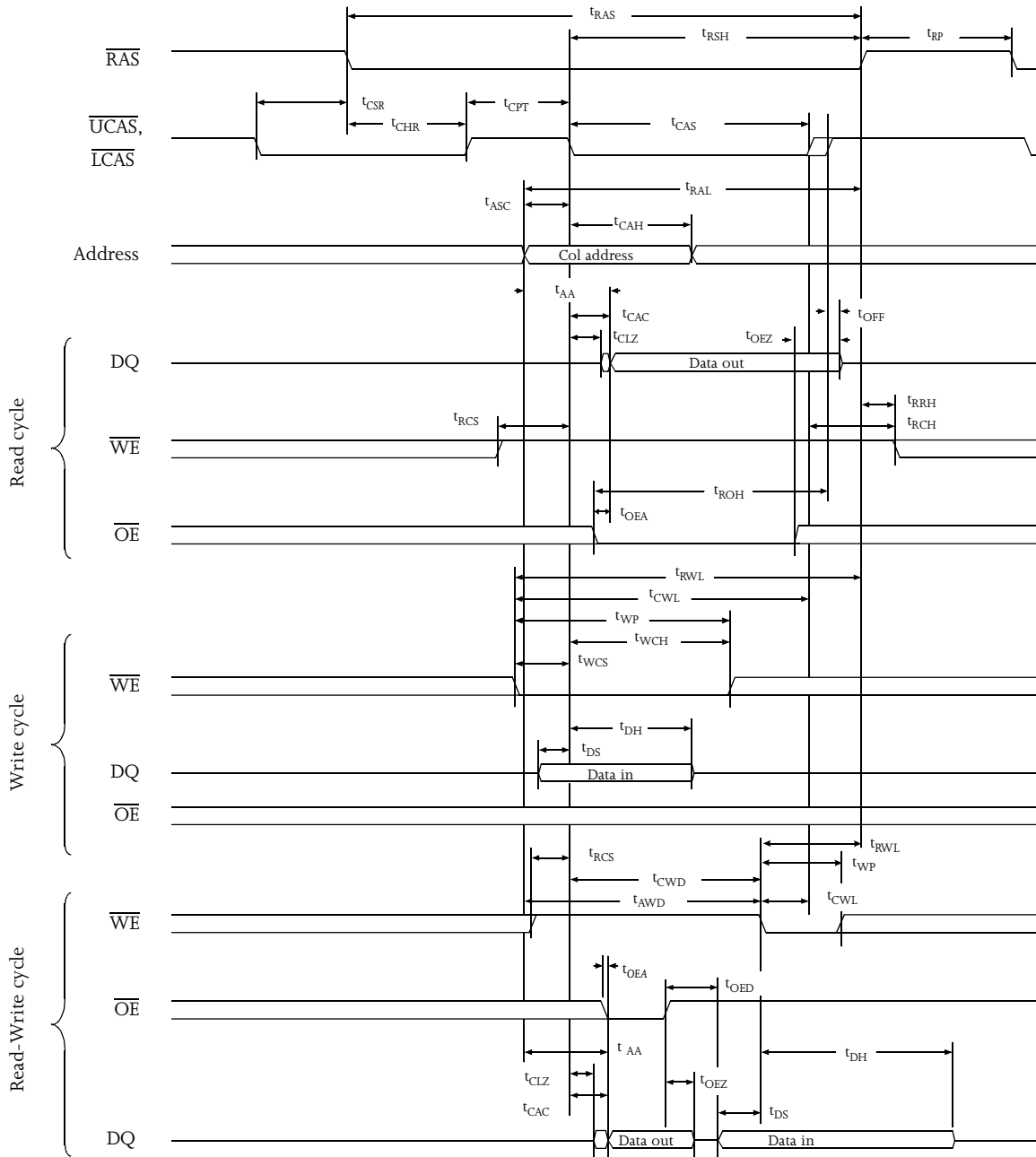


Hidden refresh waveform (write)



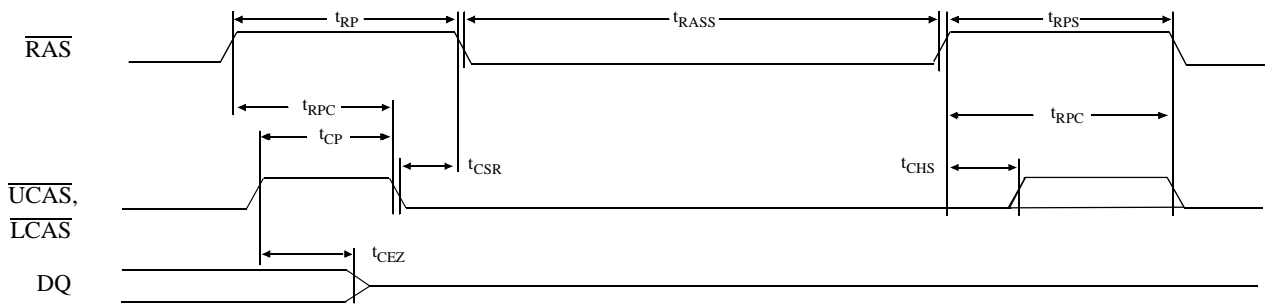


CAS before RAS refresh counter test waveform

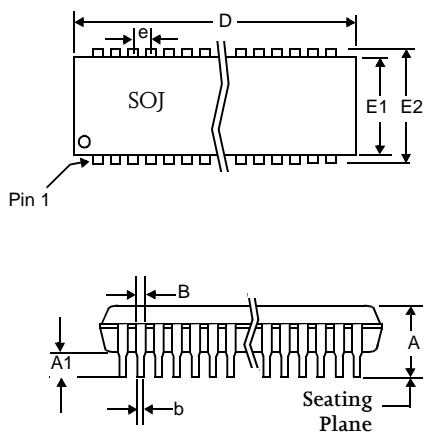




CAS-before-RAS self refresh cycle

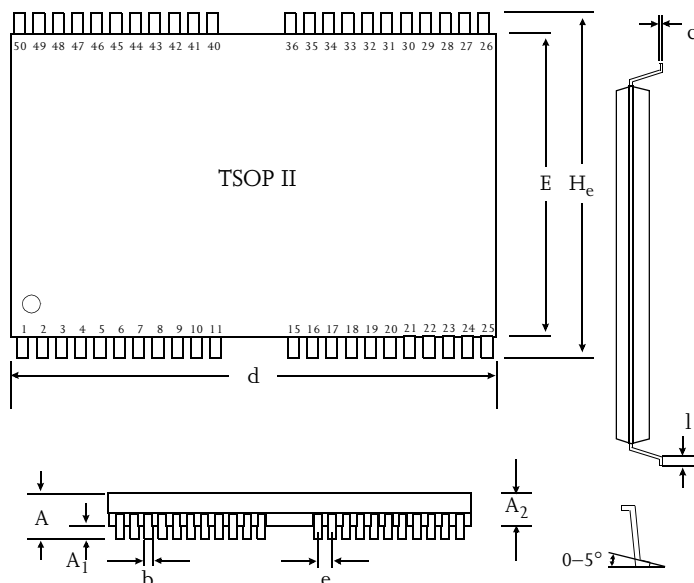


Package dimensions



42-pin SOJ

| | Min | Max |
|----|-----------|-------|
| A | 0.128 | 0.148 |
| A1 | 0.025 | - |
| A2 | 0.105 | 0.115 |
| B | 0.026 | 0.032 |
| b | 0.015 | 0.020 |
| c | 0.007 | 0.013 |
| D | 1.070 | 1.080 |
| E | 0.370 NOM | |
| E1 | 0.395 | 0.405 |
| E2 | 0.435 | 0.445 |
| e | 0.050 NOM | |



50-pin TSOP II

| | Min (mm) | Max (mm) |
|-------|----------------|----------|
| A | 1.2 | |
| A1 | 0.05 | |
| A2 | 0.95 | 1.05 |
| b | 0.30 | 0.45 |
| c | 0.12 | 0.21 |
| d | 20.85 | 21.05 |
| E | 10.03 | 10.29 |
| H_e | 11.56 | 11.96 |
| e | 0.80 (typical) | |
| l | 0.40 | 0.60 |



Capacitance ¹⁵

 $f = 1 \text{ MHz}, T_a = \text{Room temperature}$

| Parameter | Symbol | Signals | Test conditions | Max | Unit |
|-------------------|-----------|----------------------------------------------------------------------------------------------|-------------------------|-----|------|
| Input capacitance | C_{IN1} | A0 to A9 | $V_{in} = 0V$ | 5 | pF |
| | C_{IN2} | \overline{RAS} , \overline{UCAS} , \overline{LCAS} , \overline{WE} , \overline{OE} | $V_{in} = 0V$ | 7 | pF |
| DQ capacitance | C_{DQ} | DQ0 to DQ15 | $V_{in} = V_{out} = 0V$ | 7 | pF |

AS4LC1M16E5 ordering information

| Package \ \overline{RAS} access time | 50 ns | 60 ns |
|----------------------------------------|------------------|------------------|
| Plastic SOJ, 400 mil, 42-pin | AS4LC1M16E5-50JC | AS4LC1M16E5-60JC |
| | AS4LC1M16E5-50JI | AS4LC1M16E5-60JI |
| TSOP II, 400 mil, 44/50-pin | AS4LC1M16E5-50TC | AS4LC1M16E5-60TC |
| | AS4LC1M16E5-50TI | AS4LC1M16E5-60TI |

Shaded areas indicate advance information.

AS4LC1M16E5 part numbering system

| AS4 | LC | 1M16E5 | -XX | X | X |
|-------------|-------------------------------|---------------|------------------------------|---------------------------------------------------------------------|-------------------------------------------------------------------------------|
| DRAM prefix | C = 5V CMOS LC = 3.3V CMOS | Device number | \overline{RAS} access time | Package: J = 42-pin SOJ 400 mil T = 44/50-pin TSOP II 400 mil | Temperature range C=Commercial, 0°C to 70°C I=Industrial, -40°C to 85°C |