AS5050

Low Power 10-Bit Magnetic Rotary Encoder

1 General Description

The AS5050 is a single-chip magnetic rotary encoder IC with low voltage and low power features.

It includes 4 integrated Hall elements, a high resolution ADC and a smart power management controller.

The angle position, alarm bits and magnetic field information are transmitted over a standard 3-wire or 4-wire SPI interface to the host processor.

The AS5050 is available in a small QFN 16-pin 4x4x0.85mm package and specified over an operating temperature of -40ºC to 80ºC.

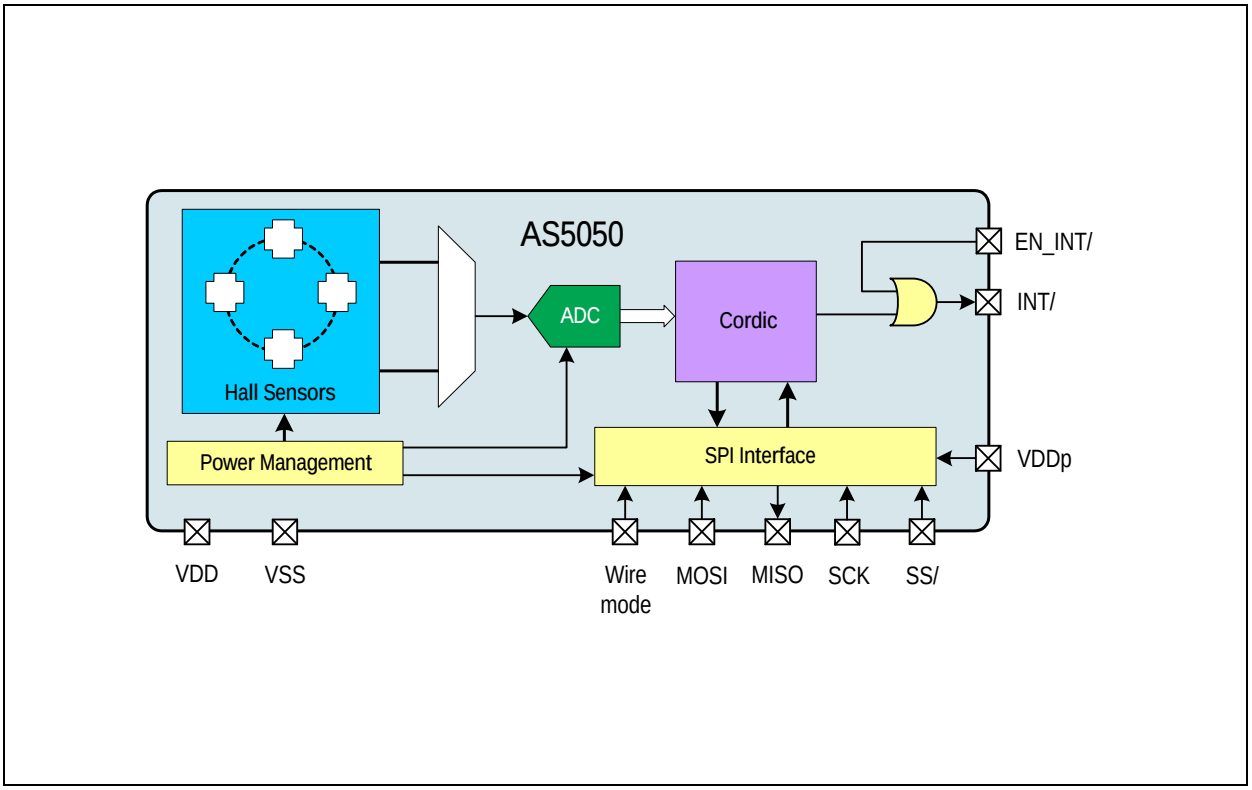
2 Key Features

- 10-bit resolution
- Standard SPI interface, 3 or 4 wire
- 3.0 to 3.6 V core voltage, 1.8 to 3.6 V peripheral supply voltage
- Automatic wakeup over SPI interface
- Interrupt output for conversion complete indication
- Low power mode:
  - < 8mA (avg) @ 620µs readout interval
  - < 5mA (avg) @ 1ms readout interval
  - < 500µA (avg) @ 10ms readout interval
  - < 53µA (avg) @ 100ms readout interval
- Small size 16-pin QFN (4x4x0.85mm)

3 Applications

The device is ideal for Servo motor control, Input device for battery operated portable devices, and Robotics.

Figure 1. AS5050 Block Diagram



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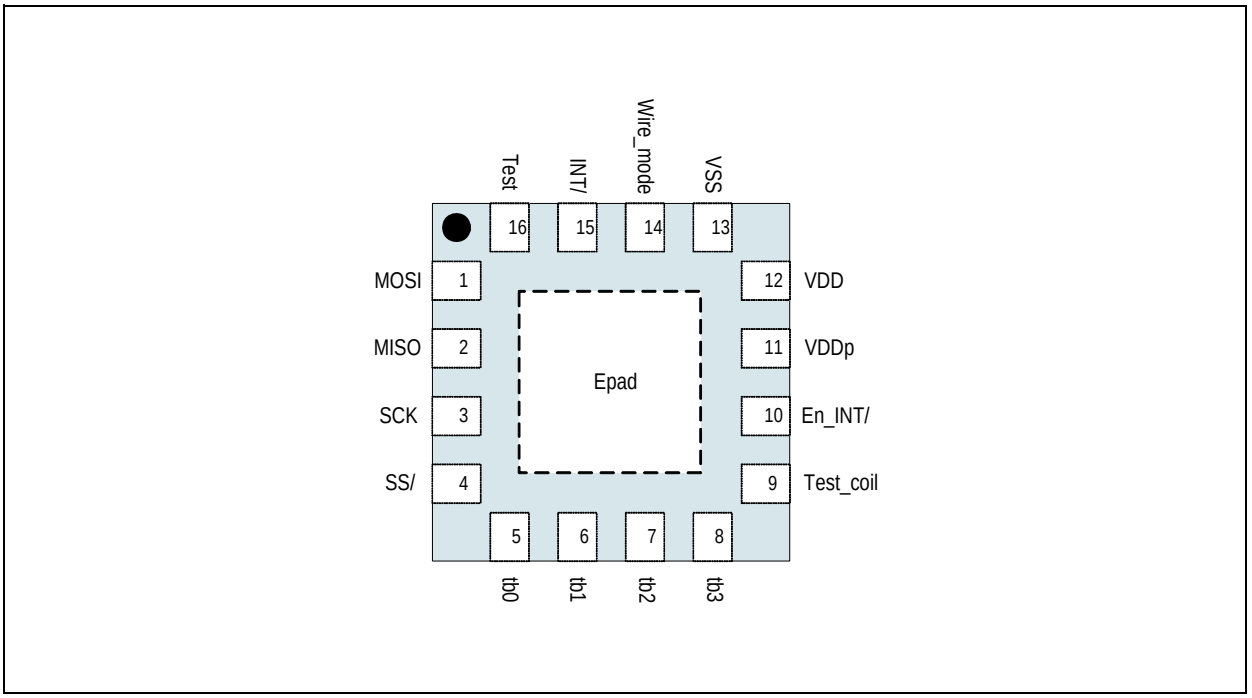
4 Pin Assignments

Figure 2. Pin Assignments (Top View)



4.1 Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Pin Name	Pin Type	Description
1	MOSI	Digital input	SPI bus data input
2	MISO	Digital output, tri-state buffer	SPI bus data output
3	SCK	Digital input Schmitt trigger	SPI Clock Schmitt trigger
4	SS/	Digital input	SPI Slave Select, active LOW
5	tb0	Analog I/O	Test pin, leave unconnected
6	tb1		
7	tb2		
8	tb3		
9	Test coil	Supply	Test pin, connect to VSS
10	En_INT/	Digital input	Enable / disable Interrupt
11	VDDp	Supply	Peripheral power supply, 1.8V ~ VDD
12	VDD		Analog and digital power supply, 3.0 ~ 3.6 V
13	VSS		Supply ground
14	Wire_mode	Digital I/O	0: 3-wire mode 1: 4-wire mode
15	INT/	Digital output, tri-state buffer	Interrupt output. Active LOW, when conversion is finished
16	Test	Digital I/O	Test pin, leave unconnected
Epad	-	-	Center pad not connected

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 5 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
VDD	DC supply voltage	-0.3	5.0	V	Value of these process dependent parameters are according to Process Parameter document, current version
VDDp	Peripheral supply voltage	-0.3	VDD+0.3	V	
V_{in}	Input pin voltage	-0.3	5.0	V	
I_{scr}	Input current (latchup immunity)	-100	100	mA	Norm: Jedec 78
Electrostatic Discharge					
ESD	Electrostatic discharge	±1	-	kV	Norm: MIL 883 E method 3015
Theta_JA	Package thermal resistance	-	33.5	°C/W	Velocity=0, Multi Layer PCB; Jedec Standard Testboard
Continuous Power Dissipation					
P_t	Total power dissipation		36	mW	
Temperature Ranges and Storage Conditions					
T_{strg}	Storage temperature	-55	125	°C	
T_{body}	Package body temperature		260	°C	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).
	Humidity non-condensing	5	85	%	
MSL	Moisture Sensitive Level	3			Represents a maximum floor life time of 168h

6 Electrical Characteristics

6.1 Operating Conditions

Table 3. Operating Conditions

Parameter	Conditions	Min	Typ	Max	Units
DC supply voltage	VDD	3.0		3.6	V
Peripheral supply voltage[1]	VDDp	1.8		VDD	V
Input pin voltage	V_{in}	-0.3		VDDp +0.3	V
Ambient operating temperature		-40		80	°C
External component	Power supply filter, pin VDD (refer to Power Supply Filter on page 6)	2.2		4.7	µF
		15		33	Ω
	Ceramic capacitor, pin VDDp to VSS	100			nF

1. VDDp must not exceed VDD (protection diode between VDDp and VDD)

6.2 System Parameters

Table 4. System Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_10	Operating current	Average current @ 10 ms readout rate[1]			0.5	mA
I_100	Operating current	Average current @ 100 ms readout rate			53	µA
I_max	Operating current	Maximum readout rate			8.5	mA
	Readout rate	Time between READ ANGLE command and INTERRUPT	320		430	µs
	Power down current	Power down current			3	µA
Rd	Lateral displacement range	Centre of the magnet to the centre of the die	-		± 0.5	mm
B_Z	Magnetic field strength		30	-	80	mT
	Serial interface	SPI mode 0 (CPOL = 0 / CPHA =0)				
	Resolution; angle			10		bit
	INL	Best-fit line - over supply, displacement and temperature – but without quantization	-1.41		1.41	degree
	IC package		QFN 4x4x0.85			

1. Without the time for the SPI interface

6.3 DC/AC Characteristics

Digital pads: MISO, MOSI, SCK, SS/, EN_INT/, INT/, Wire_mode

Table 5. DC/AC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High level input voltage		0.7 * VDDp			V
V_{IL}	Low level input voltage	VDDp > 2.7V			0.3 * VDDp	V
V_{IL}	Low level input voltage	VDDp < 2.7V			0.25 * VDDp	V
I_{LEAK}	Input leakage current				1	µA
V_{OH}	High level output voltage		VDDp - 0.5			V
V_{OL}	Low level output voltage				VSS + 0.4	V
C_L	Capacitive load				35	pF

7 Detailed Description

User Programming.

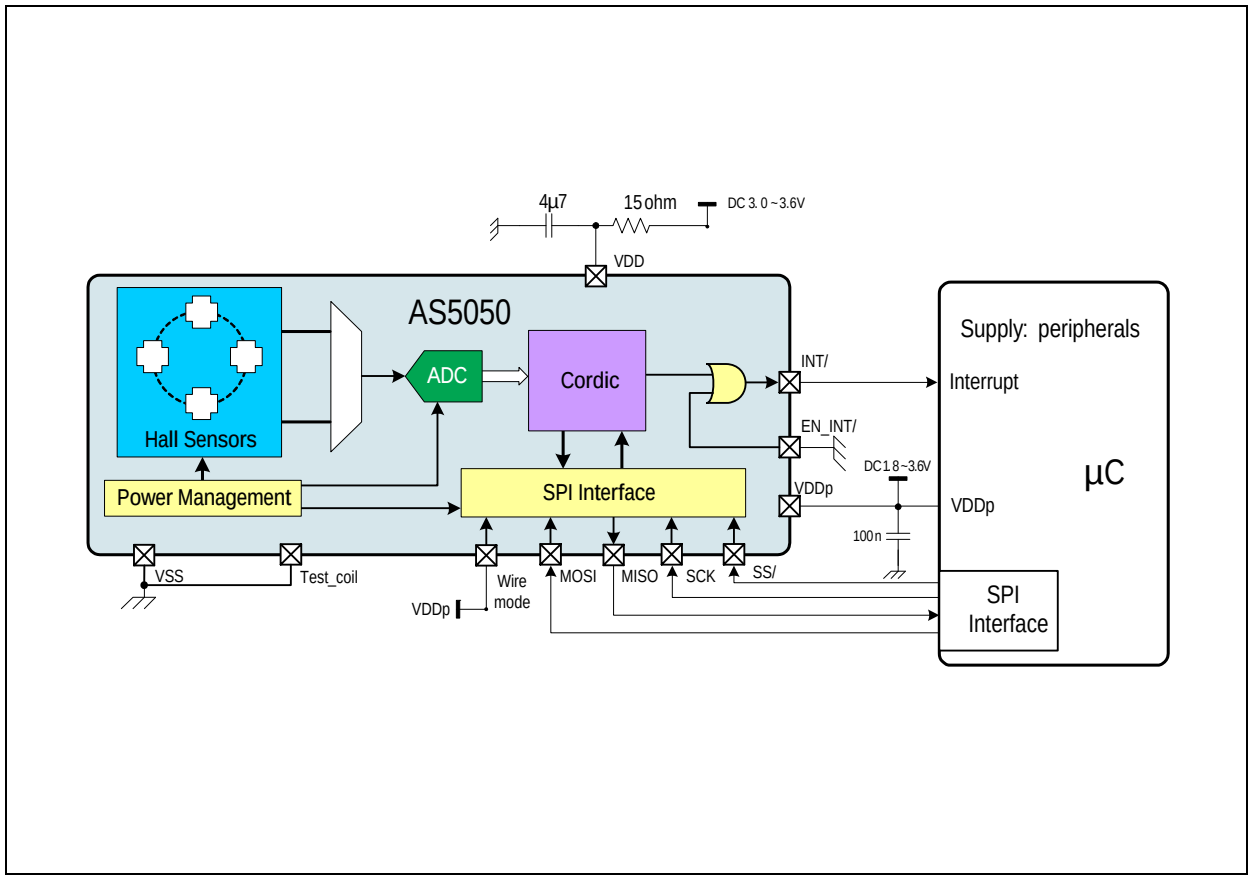
The AS5050 does not require any programming by the user. A dedicated on-chip zero position programming is not implemented. If a zero position programming is required, it is recommended to store the zero position offset in the host controller.

7.1 Operating Modes

Typical Application.

The AS5050 requires only a few external components in order to operate immediately when connected to the host microcontroller. Only 6 wires are needed for a simple application using a single power supply: two wires for power and four wires for the SPI communication. A seventh connection can be added in order to send an interrupt to the host CPU to inform that a new valid angle can be read.

Figure 3. Typical Application Using SPI 4-Wire Mode and INT/ Output



Upon power-up, the AS5050 performs a full power-up sequence including one angle measurement. The completion of this cycle is indicated at the INT/ output pin and the angle value is stored in an internal register. Once this output is set, the AS5050 suspends to sleep mode.

7.1.1 Power Supply Filter

Due to the sequential internal sampling of the Hall sensors, fluctuations on the analog power supply (pin#12: VDD) may cause additional jitter of the measured angle. This jitter can be avoided by providing a stable VDD supply.
The easiest way to achieve that is to add a RC filter: 15Ω + 4.7µF in the power supply line as shown in Figure 3.

Alternatively, a filter: 33Ω + 2.2µF may be used. However with this configuration, the minimum supply voltage is 3.15V.

7.1.2 Reading an Angle

The external microcontroller can respond to the INT request by reading the angle value from the AS5050 over the SPI interface. Once the angle value is read, the INT output is cleared again.

Sending a “read angle” command by the SPI interface also automatically powers up the chip and starts another angle measurement. As soon ad the microcontroller has completed reading of the angle value, the INT output is cleared and a new result is stored in the angle register. The completion of the angle measurement is again indicated by setting the INT output and a corresponding flag in the status register.

Reducing the Angle Jitter. Due to the measurement principle of the chip, only a single angle measurement is performed in very short time (~600µs) after each power-up sequence. As soon as the measurement of one angle is completed, the chip suspends to power-down state. An on-chip filtering of the angle value by digital averaging is not implemented, as this would require more than one angle measurement and consequently, a longer power- up time which is not desired in low-power applications.

The angle jitter can be reduced by averaging of several angle samples in the external microcontroller. For example, an averaging of 4 samples reduces the jitter by 6dB (50%).

7.1.3 Low Power Mode

After completing the readout of an angle value, the device is in very low power condition. The AS5050 remains in sleep mode until it receives another angle reading request over the SPI interface. The average power consumption therefore depends on the interval, at which the external controller reads an angle over the SPI Interface. The timing ratio between active and sleep phase:

(EQ 1)

$$I_{avg} = \frac{t_{on} * I_{on} + t_{off} * I_{off}}{t_{on} + t_{off}}$$

Where:

t_{on} = Minimum on-time for power-up and angle measurement 600µs

t_{off} = Pause interval between measurements, determined by the polling rate of the external microcontroller

I_{on} = Current consumption in active mode 8mA avg.

I_{off} = Current consumption in sleep mode 3µA

Examples:

3000 measurements per second (continuous mode)	I = 8mA
1000 measurements per second	Iavg = 5mA
100 measurements per second	Iavg = 500µA
10 measurements per second	Iavg = 53µA

Note: Even in low power mode, the power supply must be capable of supporting the active current at least for the time T_{on}, until the AS5050 is suspended to sleep mode.

7.1.4 Interrupt Chaining

Every chip contains a configurable gate to combine its own internally generated interrupt signal with a signal applied externally over the XENINT-pin. The INT-mode register is preset via an OTP register can be overwritten by the SPI interface.

Case A.

Device A is set to mode 0

Device B is set to mode 0

The micro controller recognizes an interrupt if both devices signalize that the computation is finished.

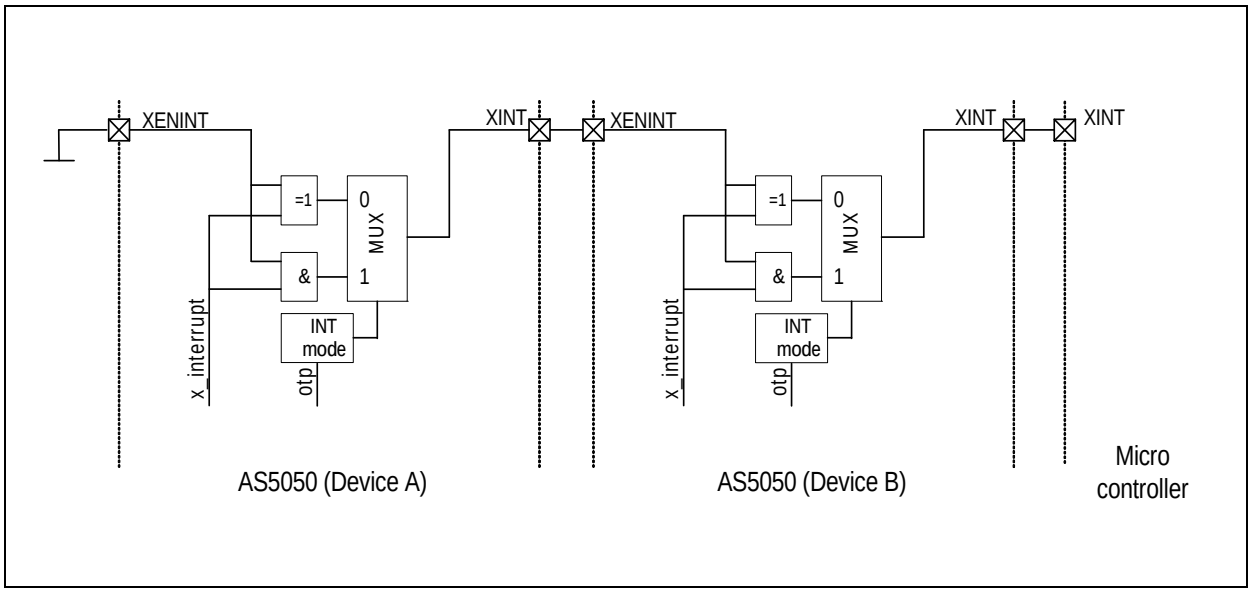
Case B.

Device A is set to mode 0

Device B is set to mode 1

The micro controller recognizes an interrupt if one of the two devices signalize that the computation is finished.

Figure 4. Interrupt Chaining



7.2 SPI Communication

The transmitted data consists of 14-bit data, an Error-Flag and a Parity bit. When writing data to the chip, the Error-Flag is not applicable. The Parity is generated from the upper 15-bit and forms an even parity over the whole frame. The Error-Flag indicates that a failure occurred in a previous transmission.

7.2.1 Command Package

Every command sent to the AS5050 is represented with the following layout.

Table 6. Command Package

Bit	MSB	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB
	RWn	Address <13:0>														PAR

Bit	Description
RWn	Indicates read or write command
Address	14-bit address code
PAR	Parity bit (EVEN)

7.2.2 Read Package (Value Read from AS5050)

The read frame always contains two alarm bits, the error and parity flags and the addressed data of the previous read command.

Table 7. Read Package

Bit	MSB	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB
	Data <13:0>														EF	PAR

Bit	Description
Data	14-bit addressed data
EF	Error flag indicating a transmission error in a previous host transmission
PAR	Parity bit (EVEN)

7.2.3 Write Data Package (Value Written to AS5050)

The write frame is compatible to the read frame and contains two additional bits, the don't care and parity flag.

If the previous command was a write command a second package has to be transmitted.

Table 8. Write Package

Bit	MSB	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB
	Data <13:0>														Don't care	PAR

Bit	Description
Data	14-bit data to write to former selected address
PAR	Parity bit (EVEN)

7.2.4 Register Block

Table 9. Register Block

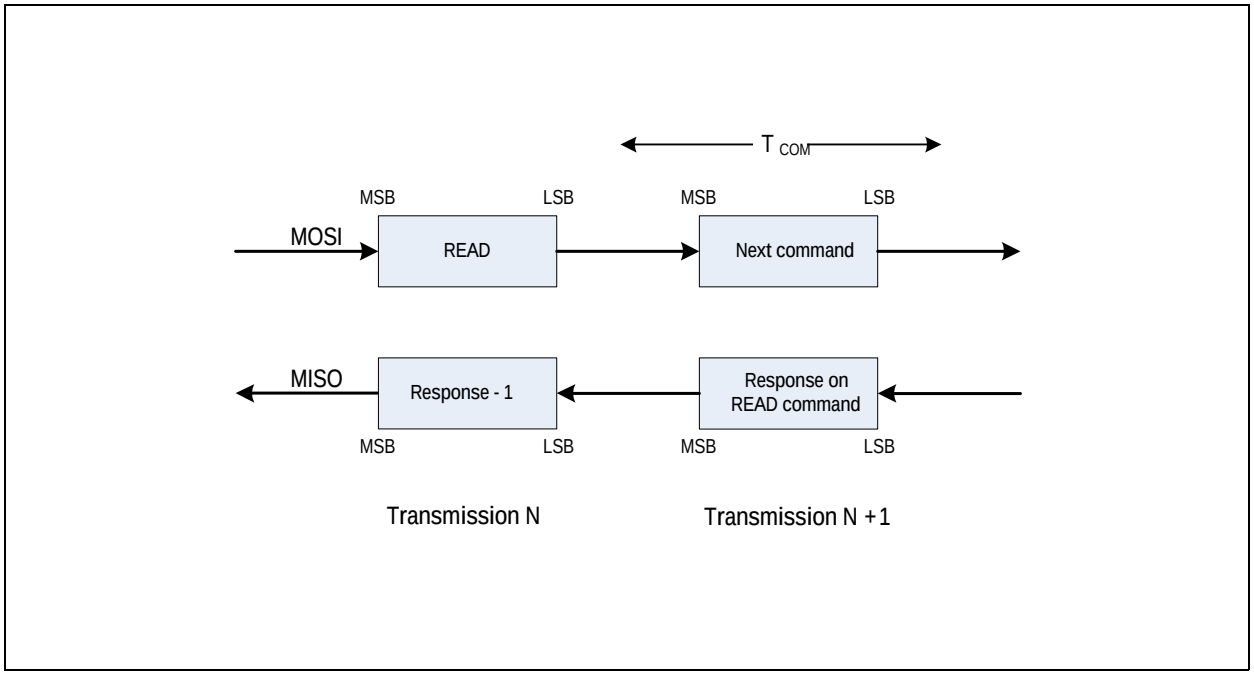
Register	Bit	Mode	Reset Value	Bit	Description
Power ON Reset (POR) Register - [0x3F22]					
POR_OFF	8	R/W	0x00	<7:0>	The POR cell is deactivated when the value 0x5A is written to this register (30µA reduction of current consumption)
Software Reset Register - [0x3C00]					
software_reset	14	W	0x0	<13:0>	Refer to SOFTWARE RESET Command on page 12
Clear Error Flag Register - [0x3380]					
clr_error_flag	14	R	0x0	<13:0>	Refer to CLEAR ERROR FLAG Command on page 11
No Operation Register - [0x0000]					
NOP	14	w	0x0	<13:0>	Refer to NOP Command on page 13
Automatic Gain Control (AGC) Register - [0x03FF8]					
AGC	6	R/W	0x20	<5:0>	Automatic gain control: low values = strong magnetic field high values = weak magnetic field
Angular Data - [0x3FFF]					
Angle Value	10	R	0x000	<9:0>	Measured angular value, 10-bit
Alarm LO	1	R	0	<12>	Alarm bit indicating a too low magnetic field, active HIGH[1]
Alarm HI	1	R	0	<13>	Alarm bit indicating a too high magnetic field, active HIGH[1]
break_offset_loop	1	R/W	0	<1>	Breaks the offset compensation loop to use the offset registers in a static mode
interrupt_mode	1	R/W	0	<0>	Interrupt gate mode 0 = mode 0 1 = mode1

1. Both bits High: Alarm LO = Alarm Hi = 1 indicate a major system error (DAC overflow, CORDIC overflow or Hall current error).

7.2.5 SPI Interface Commands

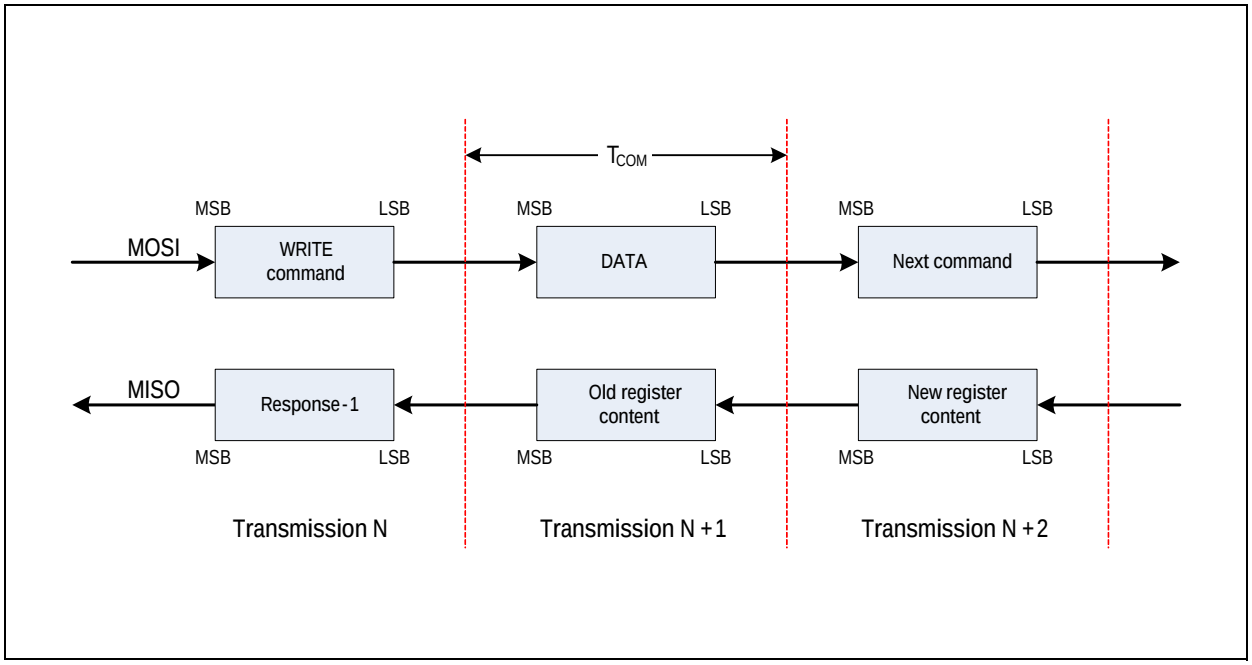
READ Command. For a single READ command two transmission sequences are necessary. The first package written to the AS5050 contains the READ command (MSB high) and the address the chip has to access, the second package transmitted to the AS5050 device can be any command the chip has to process next. The content of the desired register is available in the MISO register of the master device at the end of the second transmission cycle.

Figure 5. READ Command



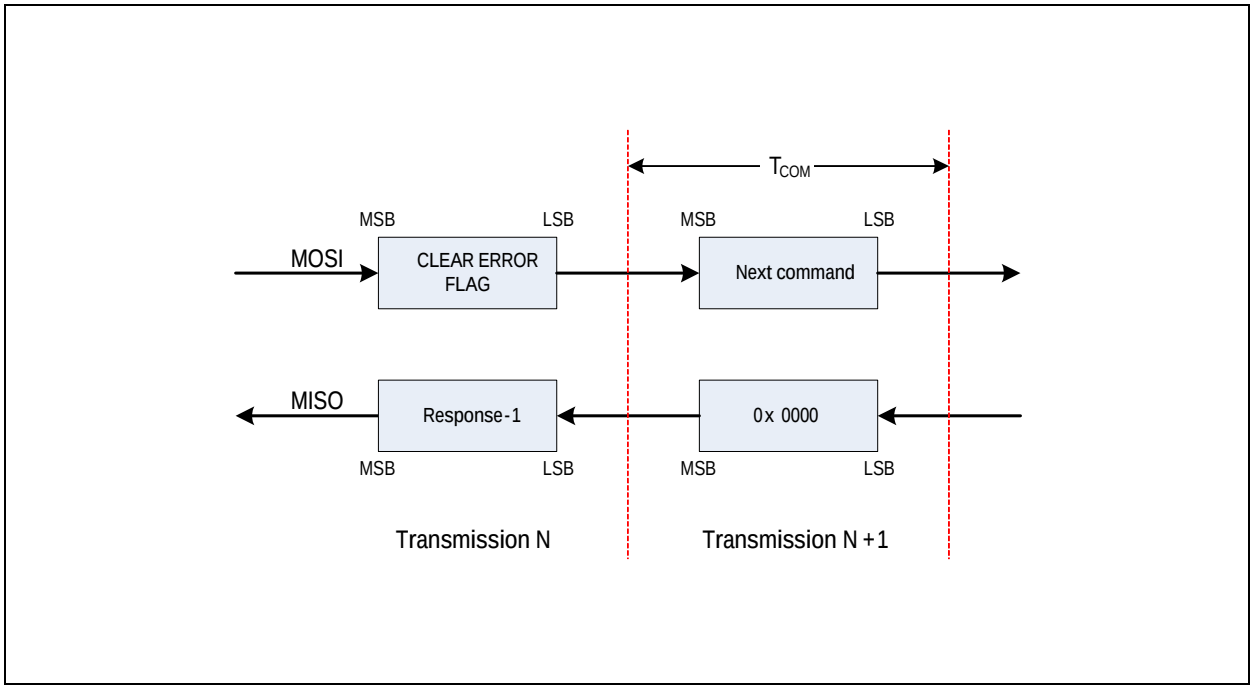
WRITE Command. A single WRITE command takes two transmission cycles. With a NOP command after the WRITE command you can verify the sent data with three transmission cycles because the data will be send back during the NOP command.

Figure 6. WRITE Command



CLEAR ERROR FLAG Command. The CLEAR ERROR FLAG command is implemented as READ command. This command clears the ERROR FLAG which is contained in every READ frame. The READ data are 0x0000, which indicates a successful clear command.

Figure 7. CLEAR ERROR FLAG Command



The package necessary to perform a CLEAR ERROR FLAG is built up as follows.

Table 10. CLEAR ERROR FLAG Command

Bit	MSB	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB
	1	1	1	0	0	1	1	1	0	0	0	0	0	0	0	PAR
	CLEAR ERROR FLAG command															PAR

Possible conditions which force the ERROR FLAG to be set:

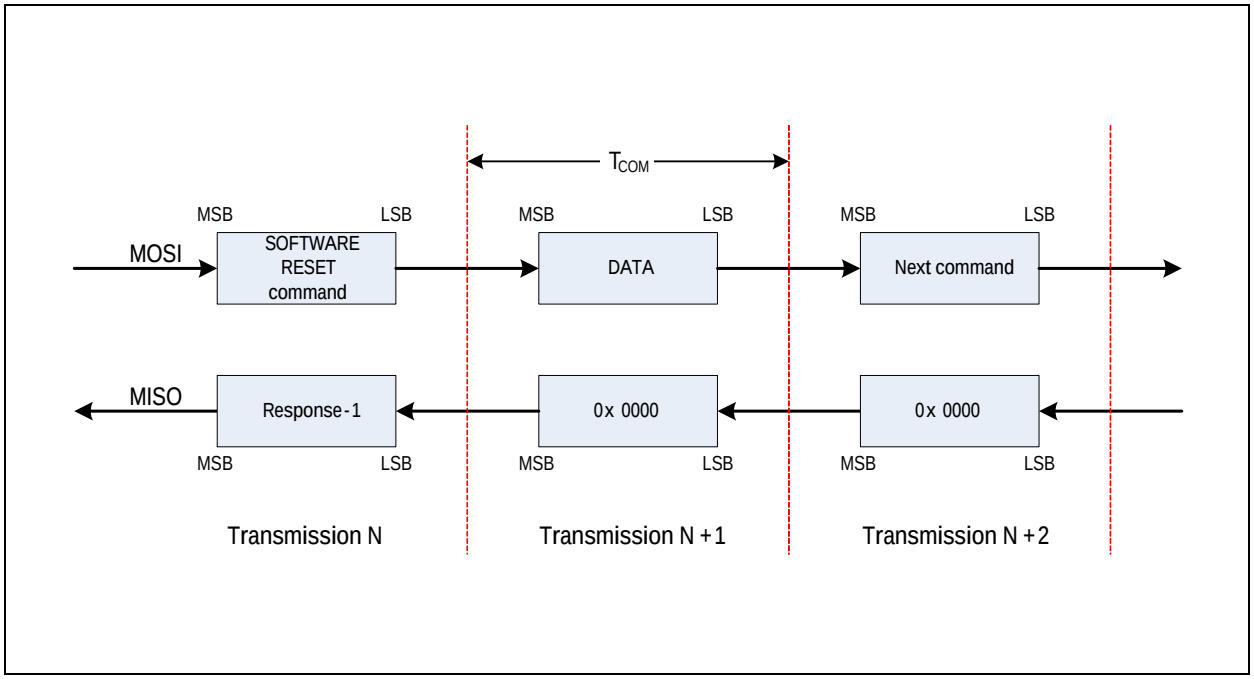
- Wrong parity
- Wrong command
- Wrong number of clocks (no full transmission cycle or too many clocks)

Note: If the error flag is set to high because of a communication problem the flag remains set until it will be cleared by an external command.

SOFTWARE RESET Command. The SOFTWARE RESET command is implemented as WRITE command. The bit 'RES SPI' of the DATA package indicates if the SPI registers should be reset as well. The soft reset resets the digital part ('RES SPI' is set to one) as well as the PPTRIM. A new PPTRIM auto-load is initiated and the reset values stored in the PPTRIM are loaded into the configuration registers. The command following the SOFTWARE RESET command can be any of the commands specified in this chapter.

After the data package is sent, the soft reset is generated. The fuses of the PPTRIM are loaded into the registers and a new conversion cycle will be started. If the device is in sleep mode the oscillator will be started first.

Figure 8. SOFTWARE RESET Command



In order to invoke a software reset on the AS5050 the following bit pattern has to be sent.

Table 11. SOFTWARE RESET Command

Bit	MSB	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB
	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	PAR
	SOFTWARE RESET command															PAR

Table 12. Data Package

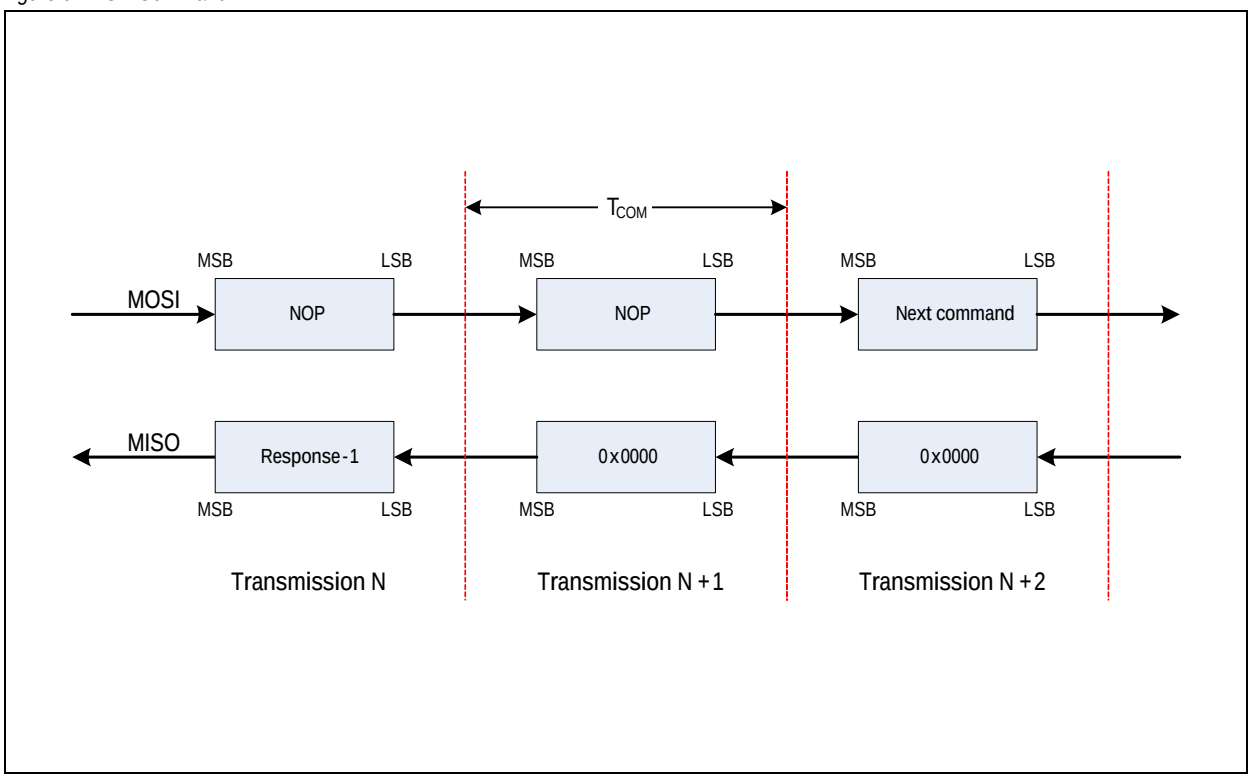
Bit	MSB	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB
	Don't care													RES SPI	Don't care	PAR

Bit	Description
RES SPI	If set to one, SPI registers are reset as well[1]
PAR	Parity bit (EVEN)

1. After a power on reset, the OTP will be read and hence OTP related registers are changed independent on the RES SPI flag.

NOP Command. The NOP command represents a dummy write to the AS5050.

Figure 9. NOP Command



The NOP command frame looks like follows.

Table 13. NOP Command

Bit	MSB	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	NOP command (0x0000)															

The chip's response on this command is 0x0000 – if no error happens.

8 Application Information

The benefits of the AS5050 device are as follows:

- Complete system-on-chip
- Low power consumption
- Low operating voltage
- Easy to use SPI interface

8.1 SPI Interface

The 16-bit SPI Interface enables read / write access to the register blocks and is compatible to a standard micro controller interface. The SPI module is active as soon as /SS pin is pulled low. The AS5050 then reads the digital value on the MOSI (master out slave in) input with every falling edge of SCK and writes on its MISO (master in slave out) output with the rising edge. After 16 clock cycles /SS has to be set back to a high status in order to reset some parts of the interface core.

The SPI Interface can be set into two different modes - 3-wire mode or 4-wire mode.

Note: The wire mode selection is read during the POWER-UP state and can be changed with a power on reset or a software reset command.

The SPI Interface can be set into two different modes: 3-wire mode or 4-wire mode.

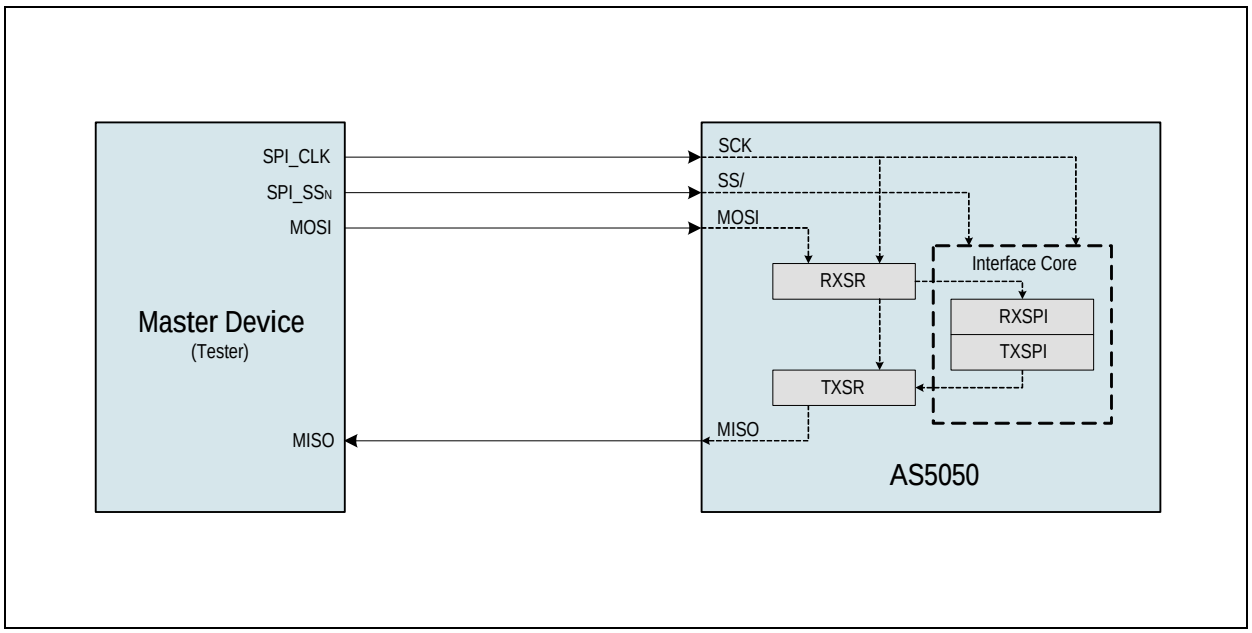
Table 14. Wire Mode Selection

Wire Mode Selection (pad 14)	
wire_mode = LO	3-wire mode
wire_mode = HI	4-wire mode

8.1.1 SPI Interface Signals (4-Wire Mode, Wire_mode = 1)

The AS5050 only supports slave operation mode. Therefore SCK for the communication as well as the /SS signal has to be provided by the test equipment. The following picture shows a basic interconnection diagram with one master and an AS5050 device and a principle schematic of the interface core.

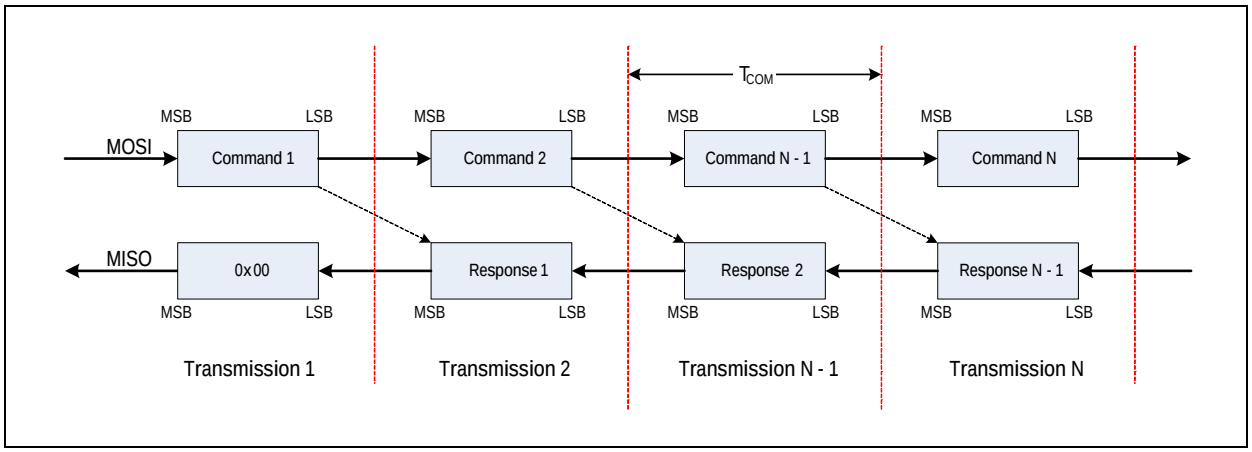
Figure 10. SPI Interface Connection



Because the interface has to decode the sent command before it can react and provide data the response of the chip to a specific command applied at a time T can be accessed in the next transmission cycle ending at T + TCOM.

The data are sent and read with MSB first. Every time the chip is accessed it is sending and receiving data.

Figure 11. SPI Command / Response Data Flow



8.1.2 SPI Timing

Figure 12. SPI Timing Diagram

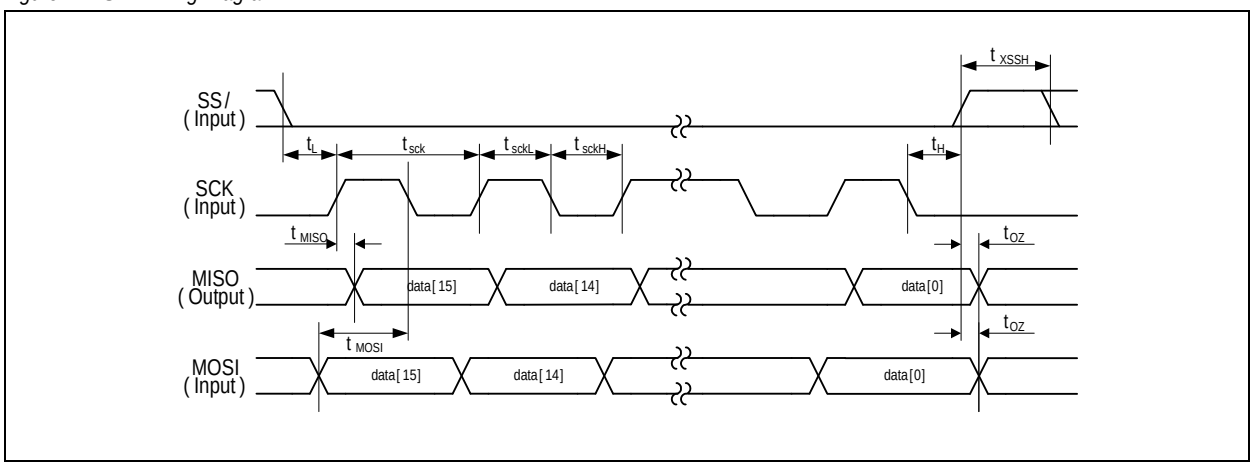


Table 15. SPI Timing Characteristics

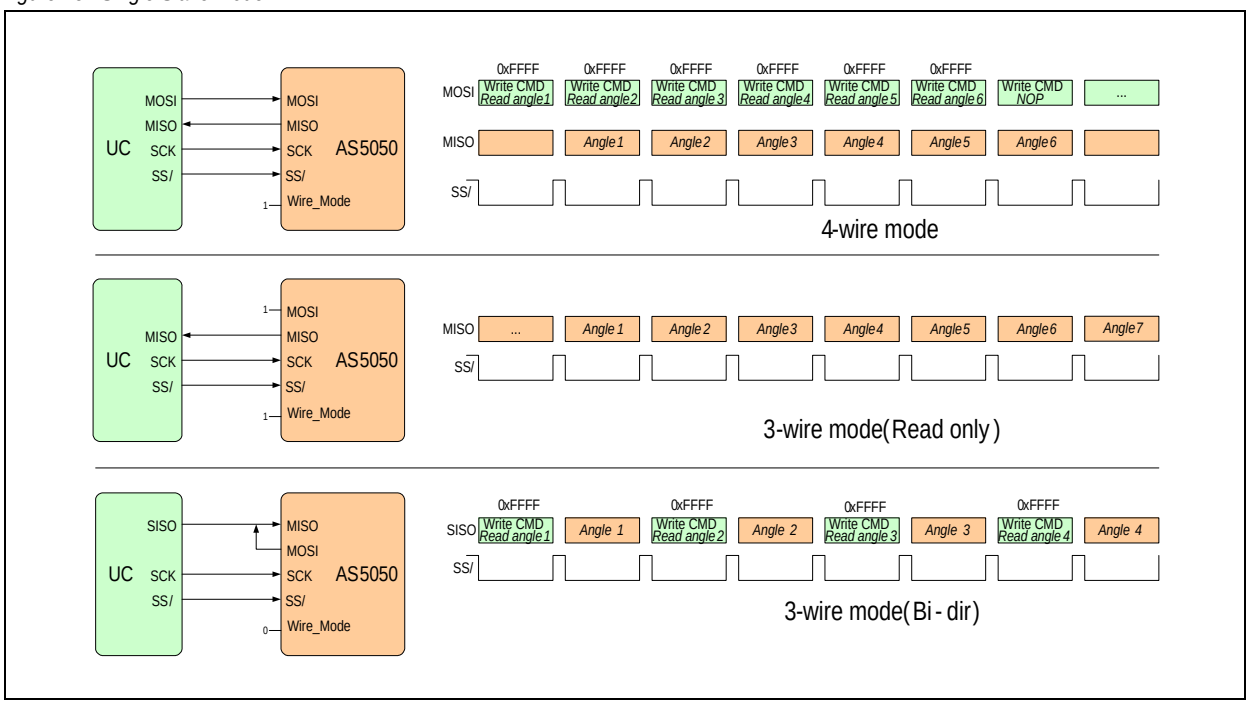
Parameter	Description	Min	Max	Unit
t_L	Time between SS/ falling edge and SCK rising edge	10[1]		ns
t_L	Time between SS/ falling edge and SCK rising edge	350[2]		ns
t_{SCK}	Serial clock period	100		ns
t_{SCKL}	Low period of serial clock	50		ns
t_{SCKH}	High period of serial clock	50		ns
t_H	Time between last falling edge of SCK and rising edge of SS/	t_{SCK} / 2		ns
t_{XSSH}	High time of SS/ between two transmissions	10[1]		ns
t_{XSSH}	High time of SS/ between two transmissions	350[2]		ns
t_{MOSI}	Data input valid to clock edge	20		ns
t_{MISO}	SCK edge to data output valid		20	ns

1. No synchronization needed because the internal clock is inactive
2. Synchronization with the internal clock → 2 * t_{CLK_SYS} + 10 ns (e.g. at 8 MHz → 253 ns)

8.1.3 SPI Connection to the Host µC

Single Slave Mode.

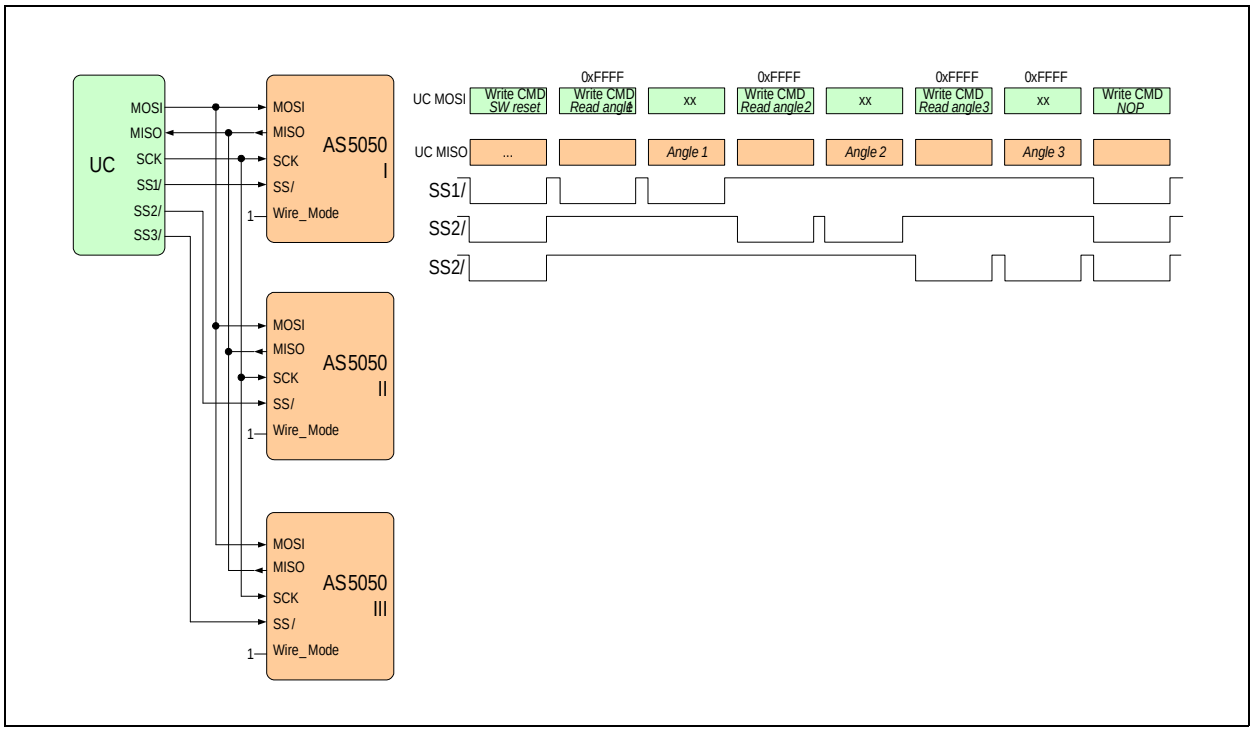
Figure 13. Single Slave Mode



Note: 3-Wire Mode (read only): If the ERROR FLAG is set the device must be externally reset.

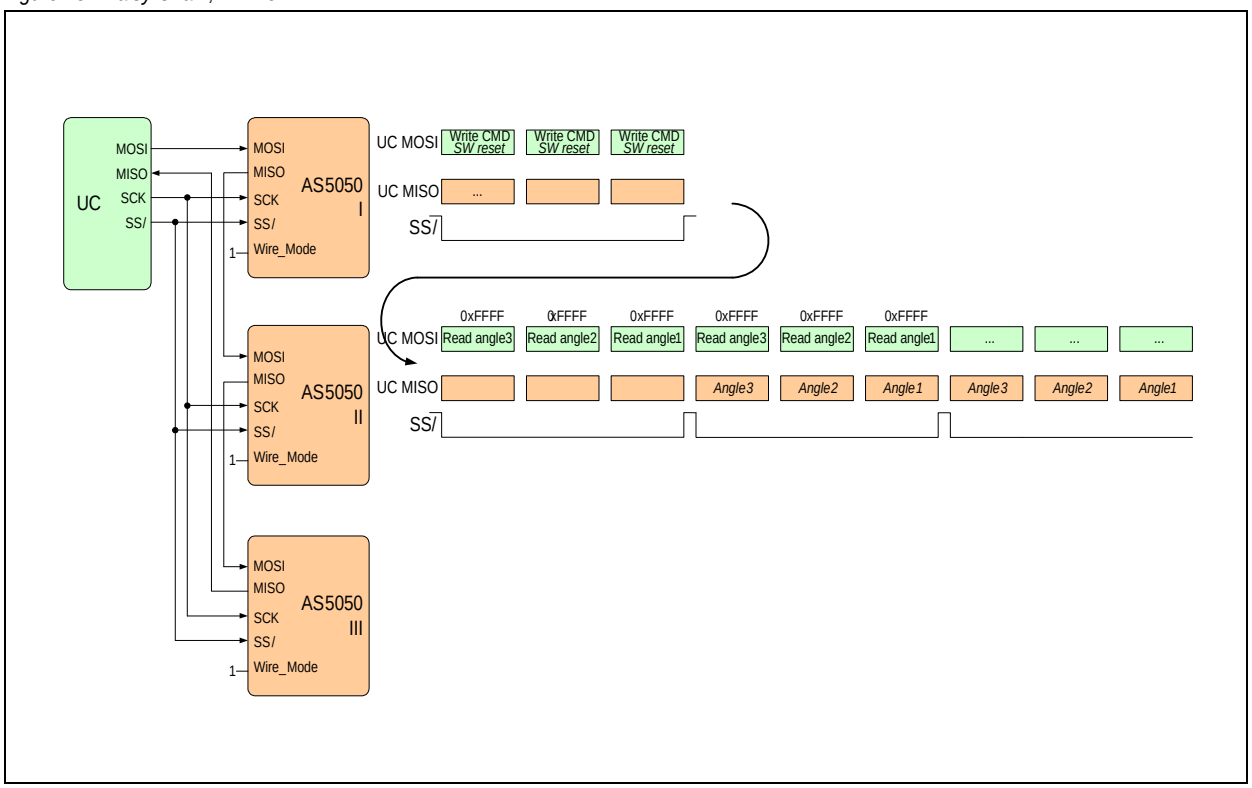
Multiple Slave, n+3 Wire (Separate ChipSelect).

Figure 14. Multiple Slave, n+3 Wire (Separate ChipSelect)



Daisy Chain, 4 Wire.

Figure 15. Daisy Chain, 4-Wire



8.2 Placement of the Magnet

Non-Linearity Error over Displacement.

As shown in Figure 17, the recommended horizontal position of the magnet axis is over the diagonal center of the IC.

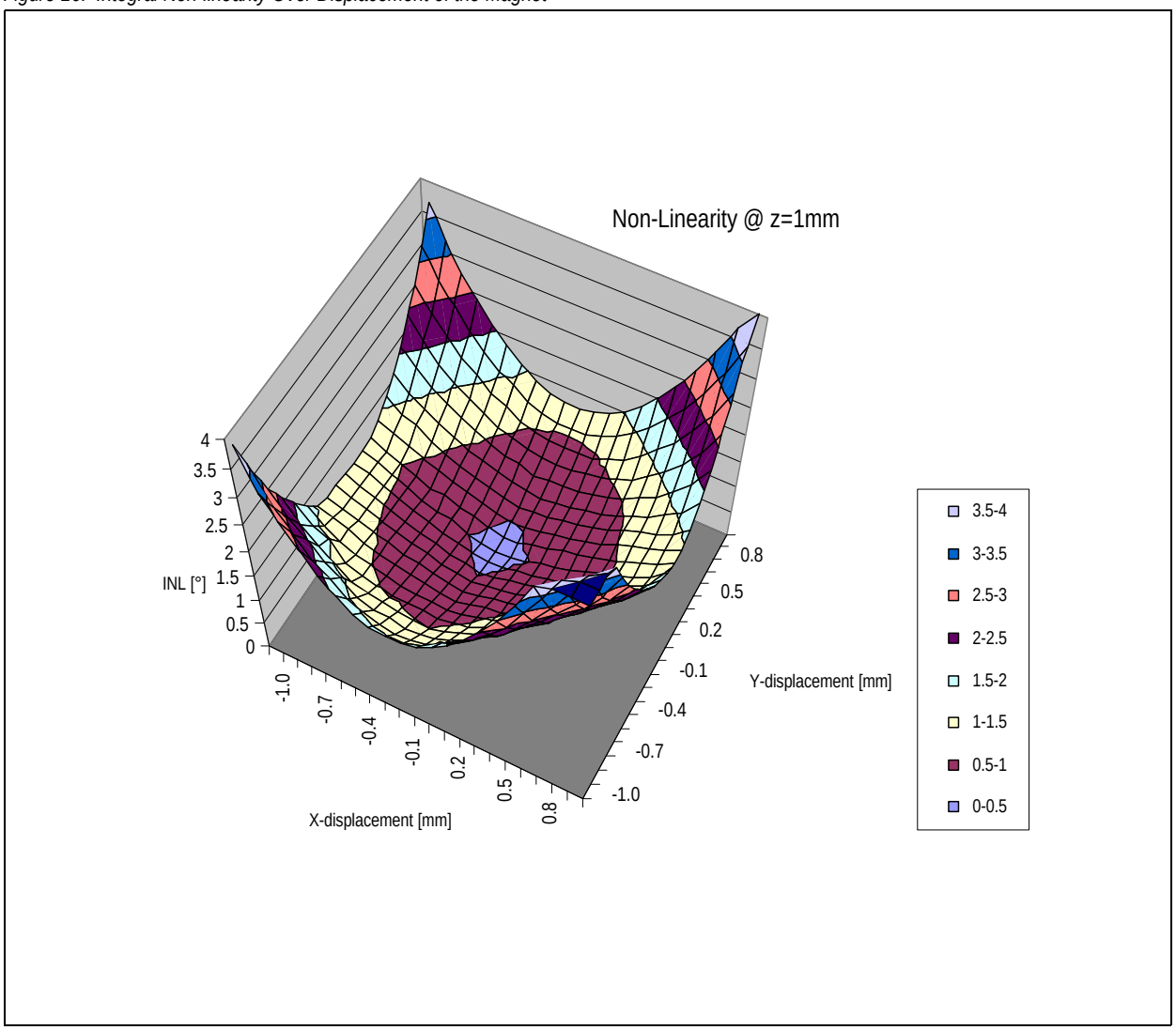
Figure 16 shows a typical error curve at a vertical magnet distance of 1.0mm, measured with a NdFeB N35H magnet with 6mm diameter and 2.5mm height.

The X- and Y- axis of the graph indicate the lateral displacement of the magnet center with respect to the IC center.

At X = Y = 0, the magnet is perfectly centered over the IC. The total displacement plotted on the graph is for ±1mm in both directions.

The Z-axis displays the worst case INL error over a full turn at each given X-and Y- displacement. The error includes the quantization error of ±½ LSB. At the sample shown in Figure 16, the accuracy for a centered magnet is better than 0.5°. Within a radius of 0.5mm, the accuracy is about 1.0° (spec = 1.41° over temperature).

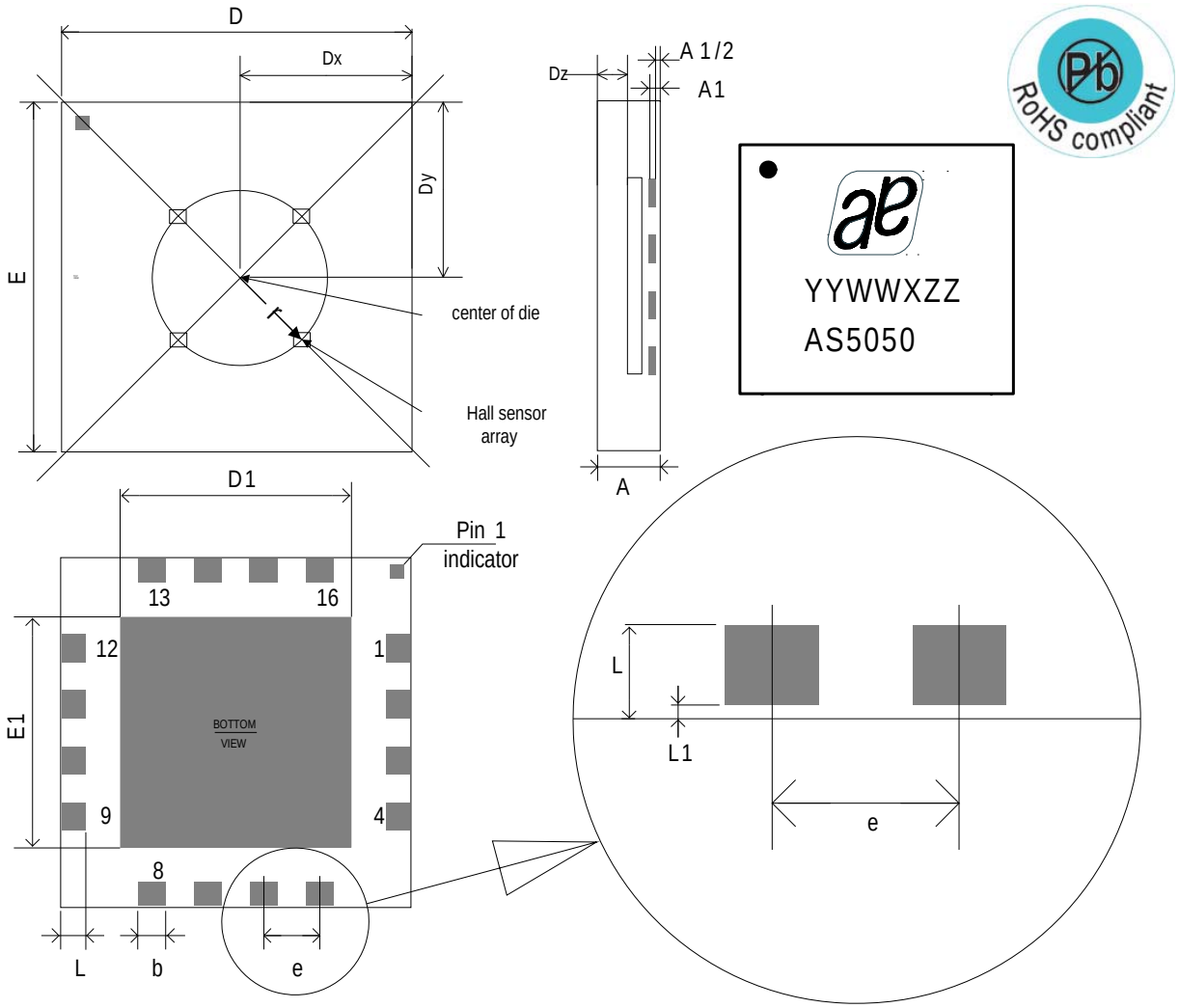
Figure 16. Integral Non-linearity Over Displacement of the Magnet



9 Package Drawings and Markings

The device is available in a 16-pin QFN (4x4x0.85mm) package.

Figure 17. Package Drawing and Hall Sensor Location



Symbol	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00		0.05
b	0.25	0.30	0.35
D		4.00 BSC	
E		4.00 BSC	
D1	2.50	2.60	2.70
E1	2.50	2.60	2.70

Symbol	Min	Nom	Max	Notes
e	-	0.65 BSC	-	
L	0.40	0.45	0.50	
L1			0.10	
Dx	1.85	2.00	2.15	1
Dy	1.85	2.00	2.15	2
Dz	0.323	0.383	0.443	3
r		1.00		4

Notes:

1. Center of die to package edge
2. Center of die to package edge
3. Surface of die to package surface
4. Radius of Hall array

Marking: YYWWXZZ.

YY	WW	X	ZZ
Year (i.e. 04 for 2004)	Week	Assembly plant identifier	Assembly traceability code

Revision History

Revision	Date	Owner	Description
1.12	17 Feb, 2011	mub	Latest draft

Note: Typos may not be explicitly mentioned under revision history.

10 Ordering Information

The devices are available as the standard products shown in Table 16.

Table 16. Ordering Information

Ordering Code	Description	Delivery Form	Package
AS5050-EQFT	10-bit low power magnetic rotary encoder	Tape & Reel	16-pin QFN (4x4x0.85mm)

Note: All products are RoHS compliant and Pb-free.
Buy our products or get free samples online at ICdirect: http://www.austriamicrosystems.com/ICdirect

Technical Support is available at http://www.austriamicrosystems.com/Technical-Support

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or find your local distributor at http://www.austriamicrosystems.com/distributor

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