AS5403A/D/E

3D Hall Position Sensor for Linear and Off-Axis Applications

General Description

The AS5403 can measure magnetic fields components in all three dimensions and converts the magnetic field information into absolute position information.

Only a simple 2-pole magnet is required as the magnetic field source.

Using two 3D-Hall cells allows absolute (single pixel) as well as differential (double pixel) 3D magnetic field measurement.

The differential measurement makes the AS5403 ideal for use in rough automotive position sensing applications that include not only dust, dirt or moisture but also unwanted magnetic stray fields.

All the signal conditioning, including compensation of temperature effects as well as linearization of the output is included in the IC.

The absolute position information of the magnet is directly accessible over a SPI interface and a programmable PWM or analog output. The build in diagnostic functions makes the AS5403 suitable for safety critical applications.

The AS5403 is available in a 14-pin TSSOP package and is qualified according AEC-Q100 for an ambient temperature range from -40°C to 150°C. It operates at a supply voltage of 5V ±10%.

The programming of the AS5403 is done over the single wire UART interface.

The AS5403 is overvoltage protected up to 18V on the supply and output pins. In addition the supply pins are reverse polarity protected up to -18V.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS5403A/D/E, 3D Hall Position Sensor for Linear and Off-Axis Applications are listed below:

Figure 1:
Added Value of Using AS5403A/D/E

Benefits	Features
High flexibility in magnet selection	High magnetic input range
Suppression against magnetic stray fields	Dual 3D pixel principle
Suitable for high temperature applications	Temperature range from -40 to 150°C (ambient)
Flexibility in choice of interface	Analog or PWM output, SPI as alternative
Best in class performance parameters	Offset and sensitivity accuracy over temperature
Flexible mechanical arrangement of magnet	Flexible configuration registers
External calculations of raw data	3D raw data assessment possible
High linearity after teaching	33 linearization points
Supporting safety critical applications	Integrated diagnostic functions

Applications

Linear position:

- Clutch/brake pedal
- Gearbox sensor

Off-Axis:

- Steering angle sensor
- Gearbox shift link

Figure 2:
Typical Set-Up of AS5403A/D With Magnet (Linear)

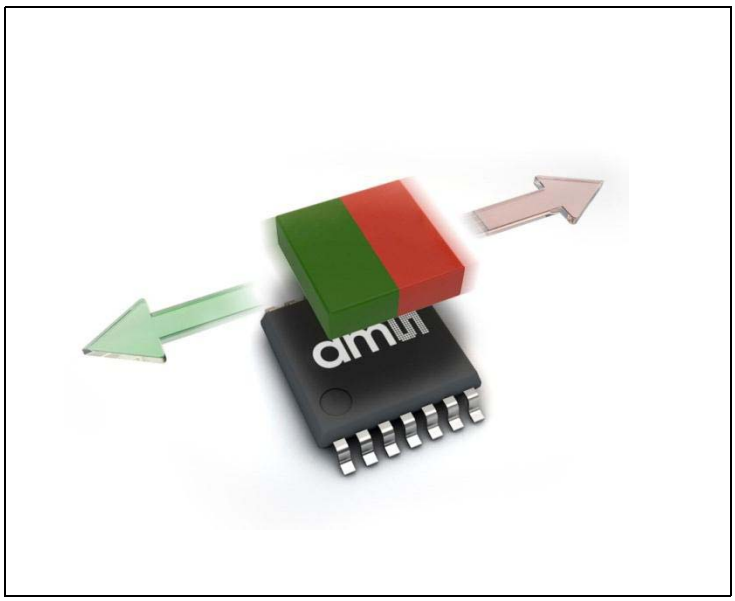
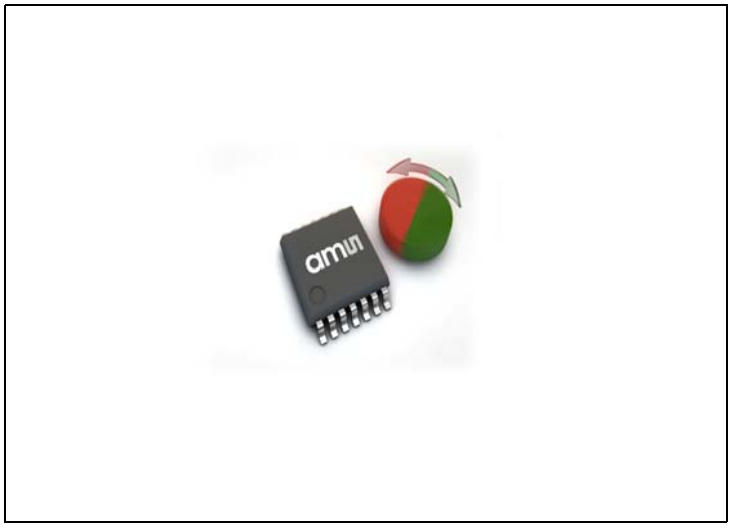


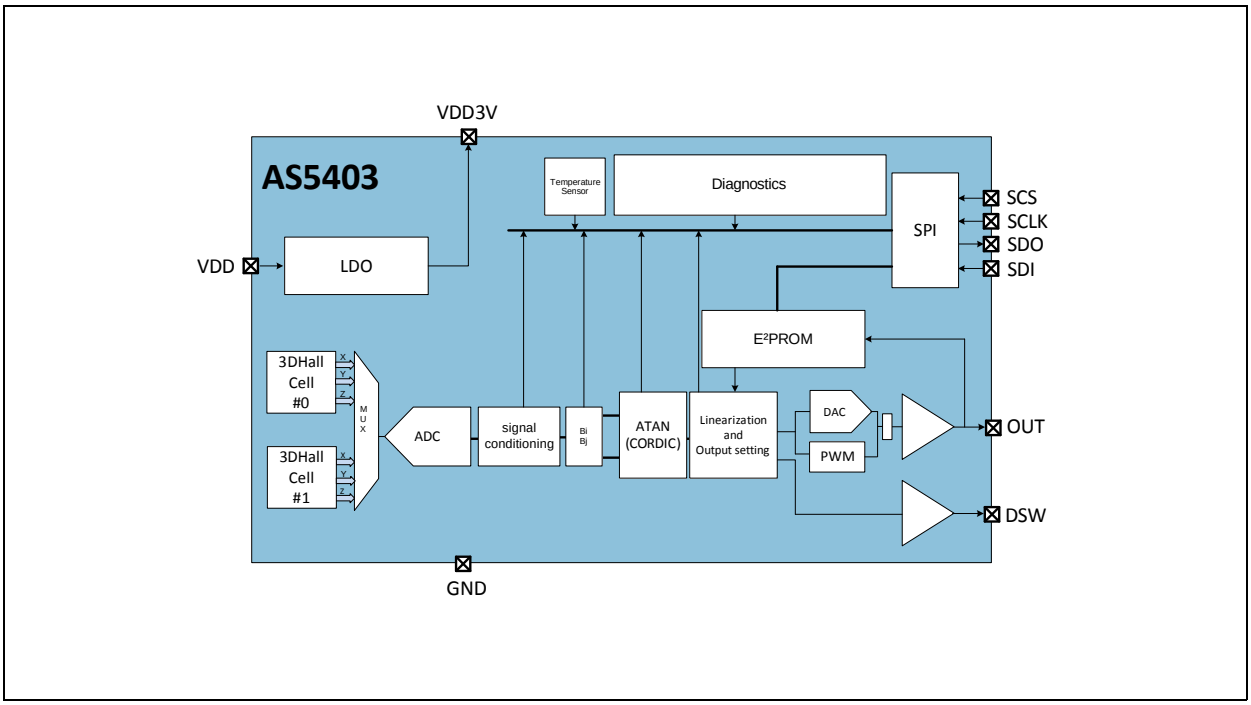
Figure 3:
Typical Set-Up of AS5403E With Magnet (Off-Axis)



Block Diagram

The functional blocks of this device for reference are shown below:

Figure 4:
AS5403A/D/E Block Diagram



3D Hall pixels:	The AS5403 contains two 3D Hall pixels, spaced 2.5mm apart.
MUX:	The multiplexer pre-selects depending on the AS5403 variant and chosen mode two/four magnetic components.
ADC:	The Sigma-Delta ADC samples the Hall sensors signals selected by the MUX. The sampling of the sensors is done sequentially.
Signal conditioning:	This block includes offset and temperature compensation as well as amplitude matching.
Bi/Bj:	Preparation of the input signal for the ATAN calculation. Inversion and offset adjustment functions.
ATAN:	Angle calculation.
Linearization:	A 33-point linearization of the ATAN output. In addition output settings for gain an clamping.
Temperature:	An on-chip temperature sensor is available. It can be read over the SPI interface. This sensor is also used for signal conditioning
PWM interface:	The linearized measurement data is available over a single pin in the form of a pulse width modulated (PWM) signal.
SPI interface:	A bi-directional SPI interface allows communication with the chip, including reading measurement data, E^2PROM contents or writing configuration data.
E^2PROM:	The on-chip E^2PROM contains the configuration data of the chip.
Diagnostics:	Monitor functions on different blocks to check the correctness of the internal signals.

Pin Assignments

Figure 5:
AS5403 Pin Configuration

AS5403 Pin Configuration, TSSOP-14 Package (Top View): X indicates the axis of lateral position measurement; z axis is perpendicular to the package surface

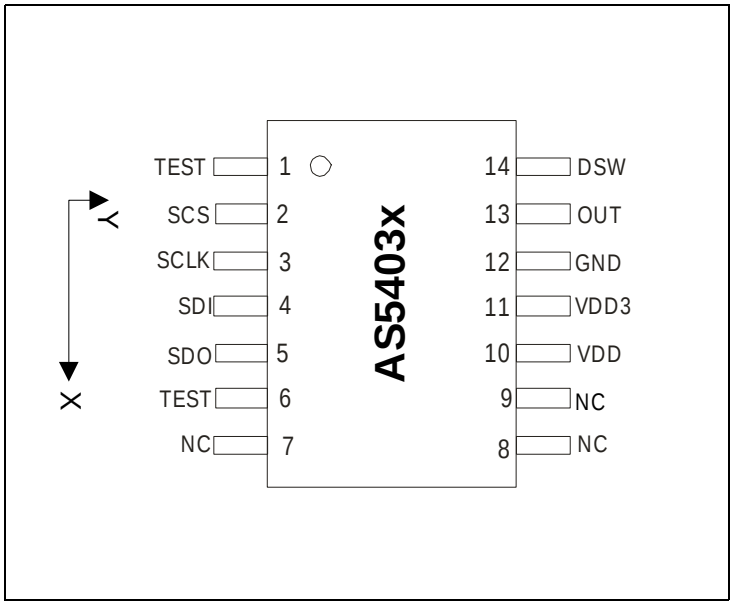


Figure 6:
Pin Description

Pin	Symbol	Type	Description
1	TEST	DI_PD	Test pin connect to GND on PCB
2	SCS	DI_PD	SPI chip select (active high), connect to GND if not used in application
3	SCLK	DI_PD	SPI clock, connect to GND if not used in application
4	SDI	DI_PD	SPI input data line, connect to GND if not used in application
5	SDO	DO	SPI output data line, leave open if not used in application
6	TEST	DO	leave open on PCB
7	NC		Not connected, Set to GND in application
8	NC		Not connected, Set to GND in application
9	NC		Not connected, Set to GND in application
10	VDD	S	Supply Voltage 5 V
11	VDD3	AIO	Regulator output
12	GND	S	Ground
13	OUT	AIO	Analog/PWM Output, programming option over output.
14	DSW	AIO	Programmable digital switch output

PIN Types:

S: Supply pad

AIO: Analog I/O

DI_PD: Digital input with internal pull down

DO: Digital output – push-pull

Electrical Characteristics

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Operating Conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 7:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Comments
VDD	DC supply voltage at pin VDD	-18	18	V	
OUT_OV	Voltage at pin OUT and DSW	-0.3	18	V	
VREG	DC voltage at VDD3 pin	-0.3	5	V	
VDIG	DC voltage at digital input and output pins	-0.3	5	V	
Iscr	Input current (latchup immunity)	-100	100	mA	AEC-Q100-004
ESD	Electrostatic discharge	± 2		kV	AEC-Q100-002
EEP_{cyc}	EEPROM endurance cycles		100	cycles	A part of EEPROM is reserved for factory settings. This part is pre-programmed and locked by **ams**. The customer area of EEPROM can be programmed up to 100 times at T_{amb}=27deg. EEPROM is intended to be programmed at 0h only in the customer production line and shall not be reprogrammed during operation in the field.
T_{strg}	Storage temperature	-55	150	°C	Min – 67°F; Max 302°F

Symbol	Parameter	Min	Max	Unit	Comments
T_{Body}	Body temperature		260	°C	The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices". The lead finish for Pb-free leaded packages is matte tin (100%Sn).
RH_{NC}	Relative humidity non-condensing	5	85	%	
MSL	Moisture Sensitivity Level	3			Represents a maximum floor life time of 168h

Operating Conditions

Operating Conditions: *Operating temperature = -40°C to 150°C, VDD = 4.5 - 5.5V unless otherwise noted.*

Figure 8:
Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comments
$T_{ambient}$	Operating temperature	-40		150	°C	
IDD	Supply current		20	25	mA	
VDD	Positive supply voltage	4.5	5	5.5	V	
T_{STUP}	Power up time			10	ms	

Magnetic Sensor Conditions

Operating Conditions: *Operating temperature = -40°C to 150°C, VDD = 4.5 - 5.5V unless otherwise noted.*

Figure 9:
Magnetic Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comments
B_{IR}	Magnetic Range X,Y,Z	±5(1)		±50	mT	AS5403A (Bx, Bz)
		±5(1)		±100	mT	AS5403D (Bx, Bz)
		±5(1)		±100	mT	AS5403E (Bx, By)
SRDxz_temp	Sensitivity ratio drift Bx/Bz	-3		3	%	Temperature only
SRDxy_temp	Sensitivity ratio drift Bx/By	-3		3	%	Temperature only
ODx	Offset drift Bx	-1(3)		1(3)	%FSR(2)	
ODy	Offset drift By	-1(3)		1(3)	%FSR(2)	
ODz	Offset drift Bz	-0.5		0.5	%FSR(2)	

Note(s) and/or Footnote(s):

1. Minimum condition is valid if both input components are above 5mT.
2. 50mT AS5403A, 100mT AS5403D and AS5403E.
3. Parameter is valid for version AS5403E and AS5403D. AS5403A ±1.5%FSR.

DC/AC Characteristics for Digital Pads

Figure 10:
DC/AC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comments
VIH	High level input voltage	70			%VDD3	
VIL	Low level input voltage			30	%VDD3	
IPD	Pull-Down input current	30		100	µA	
ILPD	Input leakage current PD	-5		5	µA	
VOH	High level output voltage	VDD3-0.5			V	IL=-4mA
VOL	Low level output voltage			0.4	V	IL=4mA
CL	Capacitive load			100	pF	

Output Driver Parameters

Figure 11:
Output Driver Characteristics OUT

Symbol	Parameter	Min	Typ	Max	Unit	Comments
GENERAL						
ILIMITLSD	Short circuit output current (LSD)	5	10	20	mA	VOUT=+18V
ILIMITHSD	Short circuit output current (HSD)	-20	-10	-5	mA	VOUT=0V
TSCDET	Short circuit detection time	20		600	µs	Output stage turned OFF
TSCREC	Short circuit recovery time	2		20	ms	Output stage turned ON
ILEAK	Output leakage	-20		20	µA	VOUT=5V; VDD=5V
BGNDPU	Output voltage broken GND with pull-up	96		100	%VDD	Guaranteed by design
BGNDPD	Output voltage broken GND with pull-down	0		4	%VDD	
BVDDPU	Output voltage broken VDD with pull-up	96		100	%VDD	
BVDDPD	Output voltage broken VDD with pull-down	0		4	%VDD	

Symbol	Parameter	Min	Typ	Max	Unit	Comments
ANALOG						
OUTVOH	Output level high	96			%VDD	IOUT=-3mA
OUTVOL	Output level low			4	%VDD	IOUT=3mA
OUTINL	Output integral non linearity			10	LSB	Between 4% and 96% of VDD
OUTDNL	Output differential non linearity	-10		10	LSB	Between 4% and 96% of VDD
OUTOFF	Output offset	-25			mV	Best fit line offset; evaluated between 4% and 96% of VDD
OUTUD	Update rate of the Output		1000		µs	
OUTSTPR	Output step response (rising)			150	µs	From step on DAC input to 90% of VDD on the OUT pin; RPUOUT=4.7KΩ; CLOUT=1nF; VDD=5V
OUTSTPF	Output step response (falling)			150	µs	From step on DAC input to 10% of VDD on the OUT pin; RPUOUT=4.7KΩ; CLOUT=1nF; VDD=5V
OUTDRIFT	Output Voltage Temperature drift	-0.5		0.5	%	of value at mid code
OUTRATE	Output ratiometricity error	-1.5		1.5	% VDD	Between 4% and 96% of VDD
OUTNOISE	Noise			25	mVpp	1KHz to 30kHz; at 2048 LSB level, lab characterization only

Symbol	Parameter	Min	Typ	Max	Unit	Comments
PWM						
PWMF	PWM frequency		1000		Hz	PWM frequency for version AS5403A and AS5403D and AS5403E 125 Hz in table selection 2. See Figure 44
T_{SYNCH}	PWM Sync time		0.1*1/PWMF		s	
PWMVOH	Output voltage high	4.6			V	VDD=5V; IOUT=-5mA
PWMVOL	Output voltage low	0		0.4	V	VDD=5V, IOUT=5mA
PWMSRR	PWM slew rate (rising edge)	1	2	4	V / µs	Between 25% and 75% RPUOUT=10kΩ; CLOUT=4.7nF VDD=5V
PWMSRF	PWM slew rate (falling edge)	1	2	4	V / µs	Between 75% and 25% RPUOUT=10kΩ; CLOUT=4.7nF VDD=5V
PROGRAMMING						
OUTVIH	High level input voltage at OUT	70			% VDD	VDD=5V
OUTVIL	Low level input voltage at OUT			30	% VDD	VDD=5V
BRATE	UART baud rate	2.4		9.6	kHz	VDD=5V

Figure 12:
Output Driver Characteristics DSW

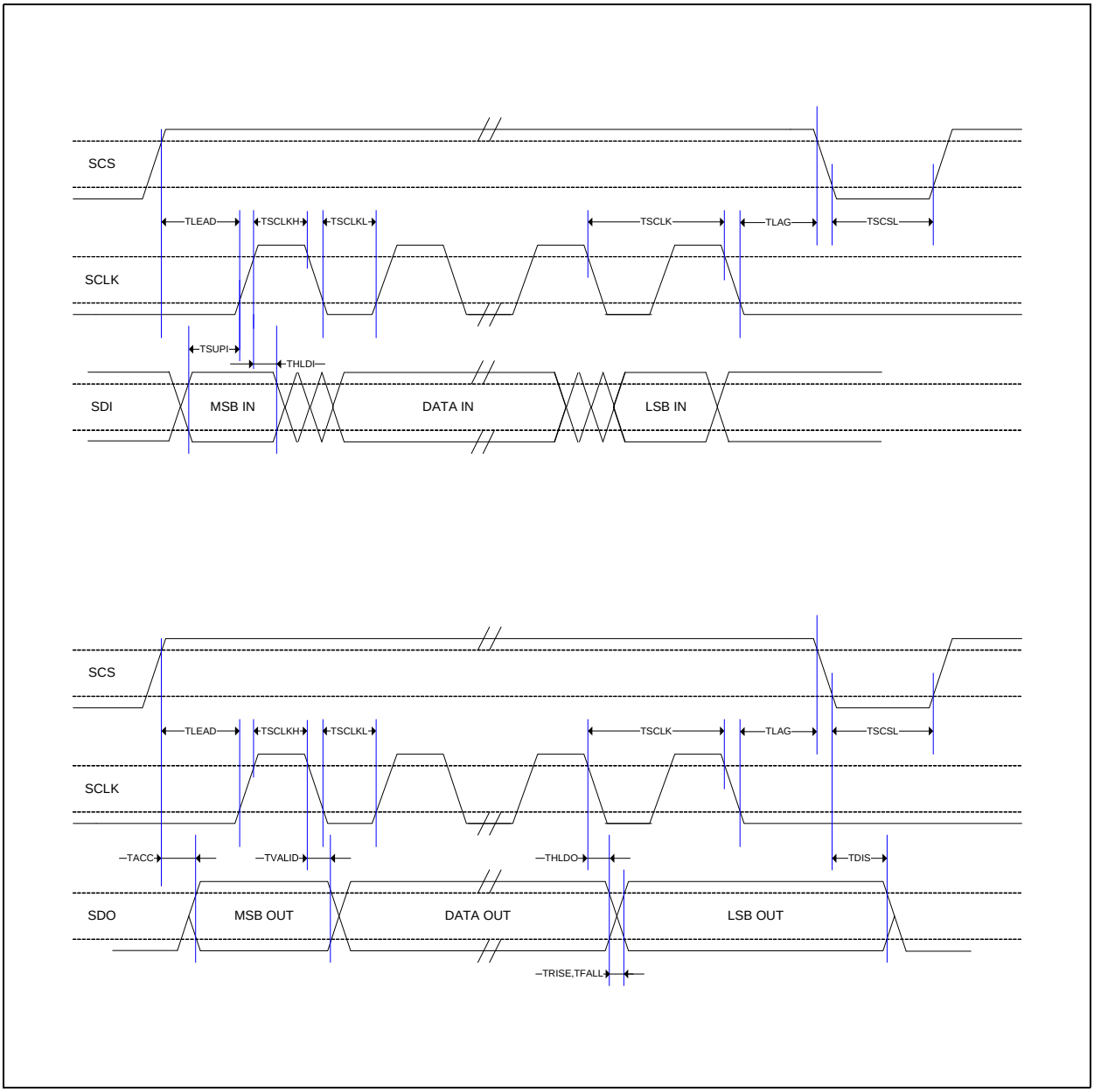
Symbol	Parameter	Min	Typ	Max	Unit	Comments
GENERAL						
DSWISCLS	Short circuit output current (LSD)	5	10	20	mA	VDSW=+18 V
DSWISCHS	Short circuit output current (LSD)	-20	-10	-5	mA	VDSW=0V
DSWTSCDET	Short circuit detection time			5	%PWM	
DSWTSCRC	Short circuit recovery time		16		PWM cycles	
DSWILEAK	Output leakage	-20		20	µA	
BGNDPU	Output voltage broken GND with pull-up	96		100	%VDD	
BGNDPD	Output voltage broken GND with pull-down	0		4	%VDD	
BVDDPU	Output voltage broken VDD with pull-up	96		100	%VDD	
BVDDPD	Output voltage broken VDD with pull-down	0		4	%VDD	
DSWVOH	Output voltage high	4.6			V	VDD=5V; IDSW=-5mA
DSWVOL	Output voltage low	0		0.4	V	VDD=5V; IDSW=5mA
DSWSRR	DSW slew rate (rising edge)	-4	-2	-1	V/µs	Between 25% and 75%; RPUDSW = 10kΩ; CLDSW=4.7nF; VDD=5V (PP with pullup)
DSWSRF	DSW slew rate (falling edge)	1	2	4	V/µs	Between 75% and 25%; RPUDSW = 10kΩ; CLDSW=4.7nF; VDD=5V (PP with pullup)

SPI Timing

Figure 13:
SPI Timing

Symbol	Parameter	Min	Typ	Max	Unit	Note
TSCLK	SCLK period	250			ns	
TSCLKH	SCLK high phase	125			ns	
TSCLKL	SCLK low phase	125			ns	
TLEAD	SCS lead time	100			ns	
TLAG	SCS lag time	100			ns	
TSCSL	SCS low phase	2500			ns	
TSUPI	SDI input setup time	50			ns	
THLDI	SDI input hold time	50			ns	
TVALID	SDO output valid time			50	ns	CL = 100pF
THLDO	SDO output hold time	0			ns	CL = 100pF
TACC	SDO output access time			100	ns	CL = 100pF
TDIS	SDO output disable time			50	ns	CL = 100pF
TRISE	SDO output rise time			60	ns	CL = 100pF
TFALL	SDO output fall time			60	ns	CL = 100pF

Figure 14:
SPI Timing Diagram



UART Timing

Figure 15:
UART Timing

Symbol	Parameter	Min	Typ	Max	Unit
UARTF	UART baud rate	2.4		9.6	kHz

Functional Description

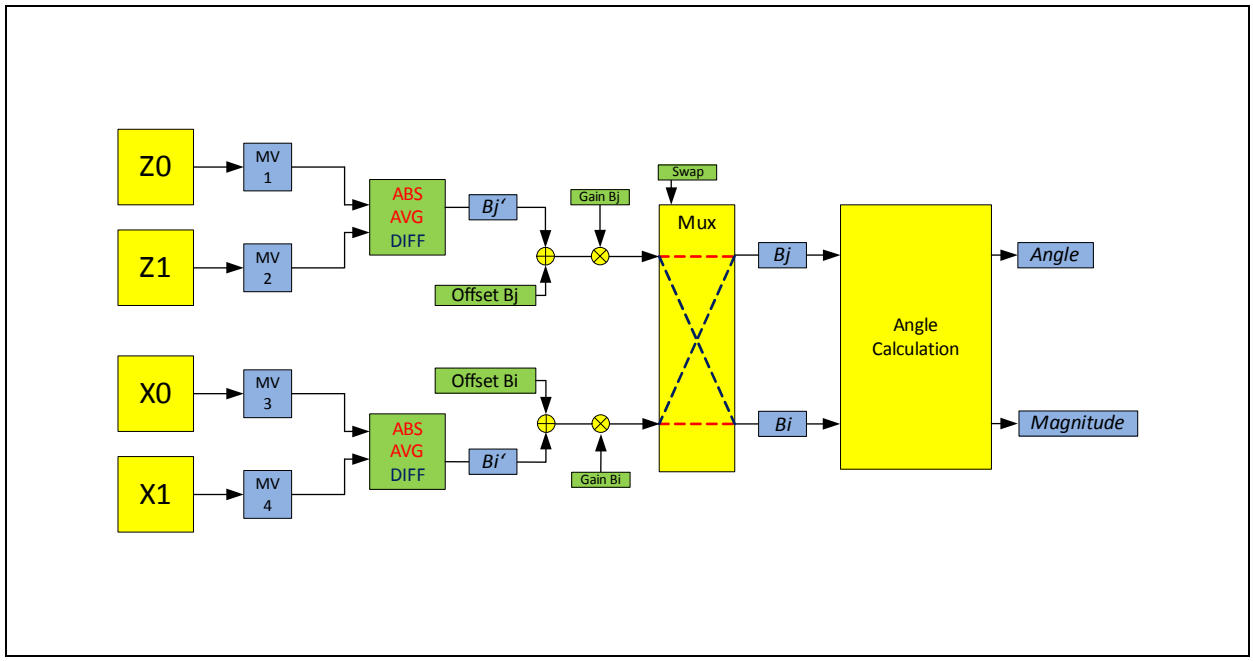
The AS5403 is manufactured in a CMOS process and uses lateral and vertical Hall sensor technology for sensing the magnetic field distribution in all 3D directions. The integrated 3D-Hall pixels are placed with a pixel pitch of 2.5 mm and deliver a voltage representation of the magnetic field at the surface of the IC.

Through Sigma-Delta Analog / Digital Conversion and Digital Signal-Processing (DSP) algorithms, the AS5403 provides accurate high-resolution absolute angular position information. For this purpose a Coordinate Rotation Digital Computer (CORDIC) calculates the angle and the magnitude.

Signal Processing Path Front

The AS5403 can be configured in different operation modes. These are absolute (ABS), average (AVG) and differential (DIFF). The internal calculation scene is changed automatically with the selected mode.

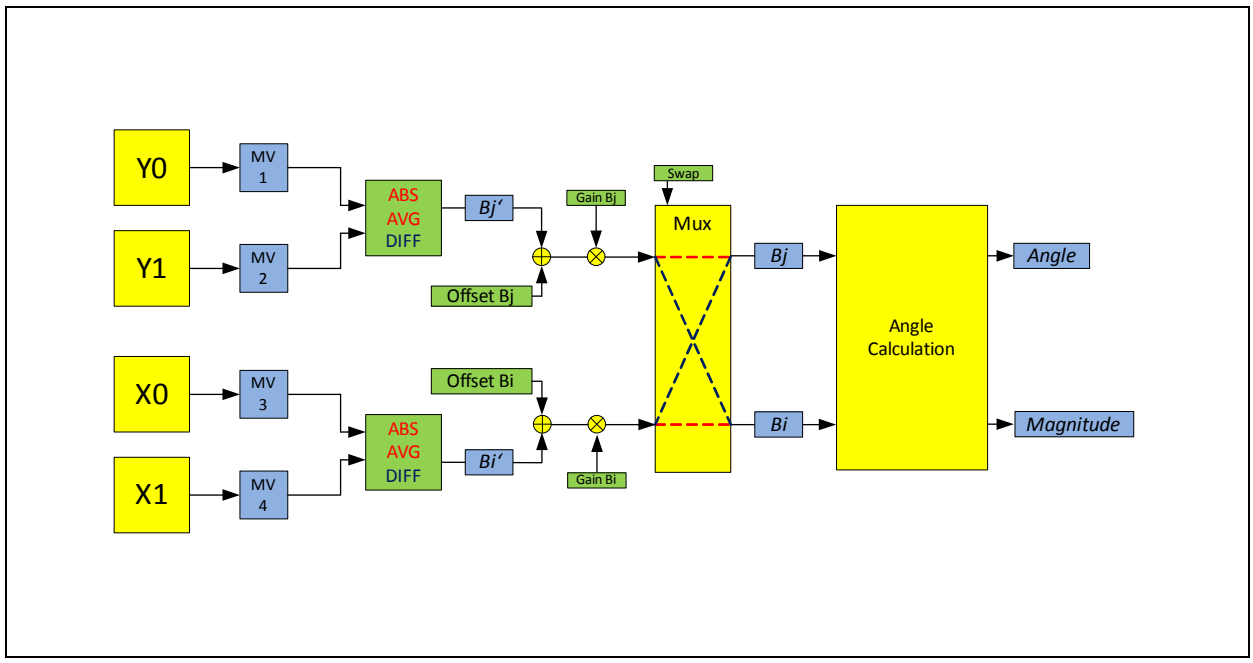
Figure 16:
Signal Processing Path AS5403A and AS5403D (Bx and Bz)



Note(s) and/or Footnote(s):

1. Yellow → Functional block
2. Blue → Readable register
3. Green → Write/Readable EEPROM parameter

Figure 17:
Signal Processing Path AS5403E (Bx and By)



Note(s) and/or Footnote(s):

1. Yellow → Functional block
2. Blue → Readable register
3. Green → Write/Readable EEPROM parameter

The individual component from 3D Hall pixel 0 and 3D Hall pixel 1 are measured sequentially. Refer to Figure 4. This sequence is predefined and depends also on the mode selection (absolute, average or differential). The digital values after conversation are stored in the measurement value registers MV1 to MV4. These values represent the raw data. The pre-calculation leads to internal result values of Bi' and Bj'. The final Bi and Bj values are available after further manipulation possibilities like offset or gain manipulation. In addition is an exchange of Bi and Bj possible over the swap function. The calculated angle and magnitude can be read out too.

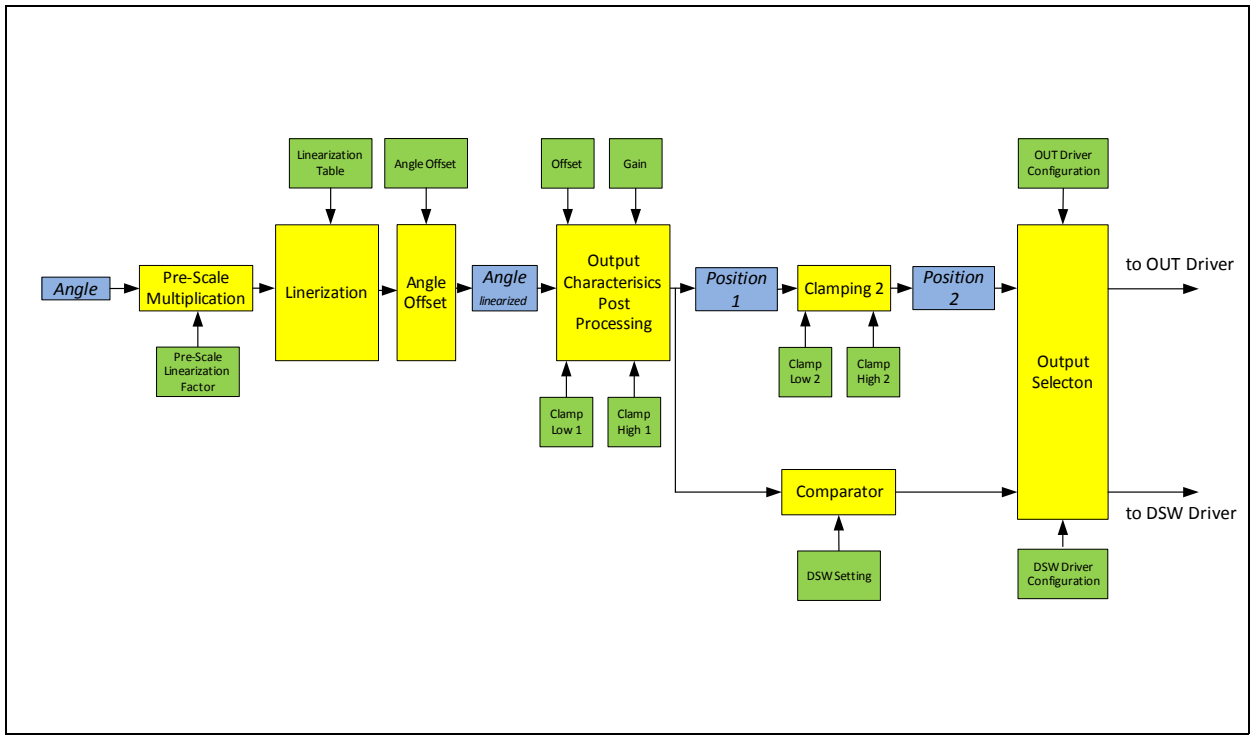
Internal Calculation Formulas

Figure 18:
Formulas for Calculation

Absolute Mode (ABS)	Average Mode (AVG)	Differential Mode (DIFF)
$Bj' = MV1$	$Bj' = (MV1 + MV2)/2$	$Bj' = -(MV1 - MV2)/2$
$Bi' = MV3$	$Bi' = (MV3 + MV4)/2$	$Bi' = (MV3 - MV4)/2$
$Bj = Gain\ Bj * (Bj' + Offset\ Bj)$	$Bj = Gain\ Bj * (Bj' + Offset\ Bj)$	$Bj = Gain\ Bi * (Bi' + Offset\ Bi)$
$Bi = Gain\ Bi * (Bi' + Offset\ Bi)$	$Bi = Gain\ Bi * (Bi' + Offset\ Bi)$	$Bi = Gain\ Bj * (Bj' + Offset\ Bj)$
$ATAN2(-B_i; B_j)$	$ATAN2(-B_i; B_j)$	$ATAN2(-B_i; B_j)$

Signal Processing Path Backend

Figure 19:
Signal Processing Path Backend



Note(s) and/or Footnote(s):

1. Yellow → functional block
2. Blue → Readable register
3. Green → Write/readable EEPROM parameter

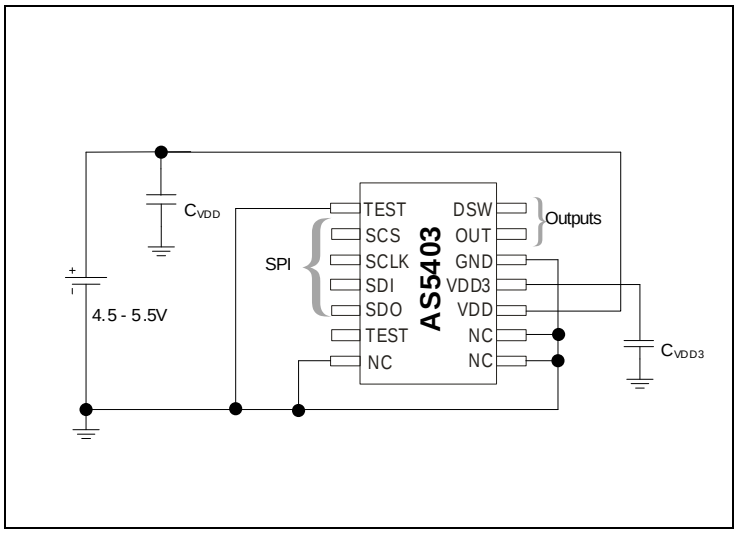
A pre-scale function can be used to extend the angle range. This is in particular needed in sector applications (off-axis) or small linear strokes. This function optimizes the usage of the linearization function in the following step. The linearization takes maximum 33 supporting point. These points are equally spread over the angular range. The post-processing function is able to manipulate the output characteristic in gain, offset and clamping. The digital output switch function uses a comparator. The switching value and hysteresis can be defined.

Finally the configuration of the output defines the operation of the output drivers.

Operation

The AS5403 operates at 5V ±10%, using one internal Low-Dropout (LDO) voltage regulator. For operation, the 5V supply is connected to pin VDD. While VDD3 (LDO output) must be buffered by 1µF capacitor, the VDD requires a 1µF capacitor. All capacitors (low ESR ceramic) are supposed to be placed close to the supply pins (see Figure 20).The VDD3 output is intended for internal use only. It must not be loaded with an external load.

Figure 20:
Connections for 5V Supply Voltages



Note(s) and/or Footnote(s):

1. The pin VDD3 must always be buffered by a capacitor. It must not be left floating, as this may cause instable internal supply voltages which may lead to larger output jitter of the measured angle.
   The supply pin is over voltage protected up to 18V. In addition the device has a reverse polarity protection.

External Components

Figure 21:
External Components in the System

Symbol	Parameter	Min	Typ	Max	Unit	Note
C_{VDD}	VDD Buffer capacitance	0.8	1	1.2	µF	
ESRCBVDD	ESR of VDD capacitance			0.3	Ω	
C_{VDD3}	VDD3 Buffer capacitor	0.8	1	1.2	µF	
ESRREG3	ESR of VDD3 capacitance			0.3	Ω	
C_{LOUT}	OUT Load Capacitance	0		20	nF	
R_{PUOUT}	OUT Pull-Up Resistance	4.7		10	kΩ	
R_{PDOUT}	OUT Pull-Down Resistance	4.7		10	kΩ	
C_{LDSW}	DSW Load Capacitance	0		20	nF	
R_{PUDSW}	DSW Pull-Up Resistance	4.7		10	kΩ	
R_{PDDSW}	DSW Pull-Down Resistance	4.7		10	kΩ	

Built-In Safety

Figure 22:
Diagnostic Functions of the AS5403

Monitoring	Error Type	Source	Comments
VDD undervoltage	Hardware-Error (1)	Power management	Recoverable
VDD overvoltage	Hardware-Error (1)	Power management	Recoverable
VREG undervoltage	Hardware-Error (1)	Power management	Recoverable
Oscillator failure	Hardware-Error (1)	CLK management	Not recoverable
Loss of GND	Hardware-Error (1)	Output driver	
Loss of VDD	Hardware-Error (1)	Output driver	
Output short circuit	Hardware-Error (1)	Output driver	Recoverable after 16 PWM period
PWM/Digital switch readout failure	Hardware-Error (1)	Output driver	Recoverable after 16 PWM period
Signature failure	Hardware-Error (1)	EEPROM	Not recoverable
Linearization Overflow	Algorithm Error (2)	Digital DSP	
Range Warning	Algorithm Error (2)	Digital DSP	
Sensitivity Correction Overflow	Algorithm Error (2)	Digital DSP	
Normalization Overflow	Algorithm Error (2)	Digital DSP	
Magnet Lost	Algorithm Error (2)	Digital DSP	
Self Monitoring Error	Hardware-Error (1)	Digital DSP	Not recoverable
PWM synchronization Error	Hardware-Error (1)	PWM Engine	Not recoverable

Note(s) and/or Footnote(s):

1. Hardware Error output to high impedance (HZ).
2. Algorithm Error PWM at 5%DC and /PWM at 95%DC depending on Diag_High, digital switches in high impedance (HZ), analog output insight upper or lower failure band depending on Diag_High. All algorithm errors are recoverable.

Output Drivers

AS5403 has two output stages, with different characteristics. The output driver on pin OUT can be programmed as analog output or low side driver PWM (/PWM), and includes a receiver for the bidirectional communication used to configure the device at module level. The driver on pin DSW is a low side only and can be configured as /PWM (PWM) or digital switch but doesn't have the receiver and in communication behaves as programmed in the EEPROM. Possible configurations for OUT selectable from EEPROM bits are:

Figure 23:
Possible Configurations of OUT Pin

Mode	OUT CFG <2>	OUT CFG <1>	OUT CFG <0>	Note
Analog Output Mode	0	0	0	Push-Pull analog output driver external pull up or pull down required
PWM push/pull	0	1	0	Pulse width modulated output with push/pull driver external pull up required
PWM open drain	0	1	1	Pulse width modulated output with low side driver external pull up required
PWMn push/pull	1	0	0	Inverted pulse width modulated output with push/pull driver external pull up required
PWMn push/pull	1	0	1	Inverted pulse width modulated output with low side driver external pull up required
PWM open drain reduced slew rate	1	1	0	Pulse width modulated output with low side driver external pull up required reduced falling edge

Note(s) and/or Footnote(s):

1. All other not specified combinations are reserved and not allowed. To avoid floating situation in diagnostic case a pull up resistor is recommended also in push/pull mode.

PWM Output

When the PWM mode is selected the measured position is proportional to the duty cycle. A range of 10% to 90% of the PWM period is used to carry the information and the remaining ranges are used as a fail signal (a 5% PWM means Algorithm Error, no change over a whole period means a Hard Error). The 80% of the PWM period contains the position information. Depending on the AS5403 version (A/D/E) and mode selection the PWM frequency can change between 1.0 kHz and 0.125 kHz. The PWM resolution can also change between 10 bit (1024 positions) for 1.0 kHz and 12 bit (4096 positions) for 0.125 kHz. The behavior of PWM and /PWM is shown in the following figures.

Figure 24:
PWM Output

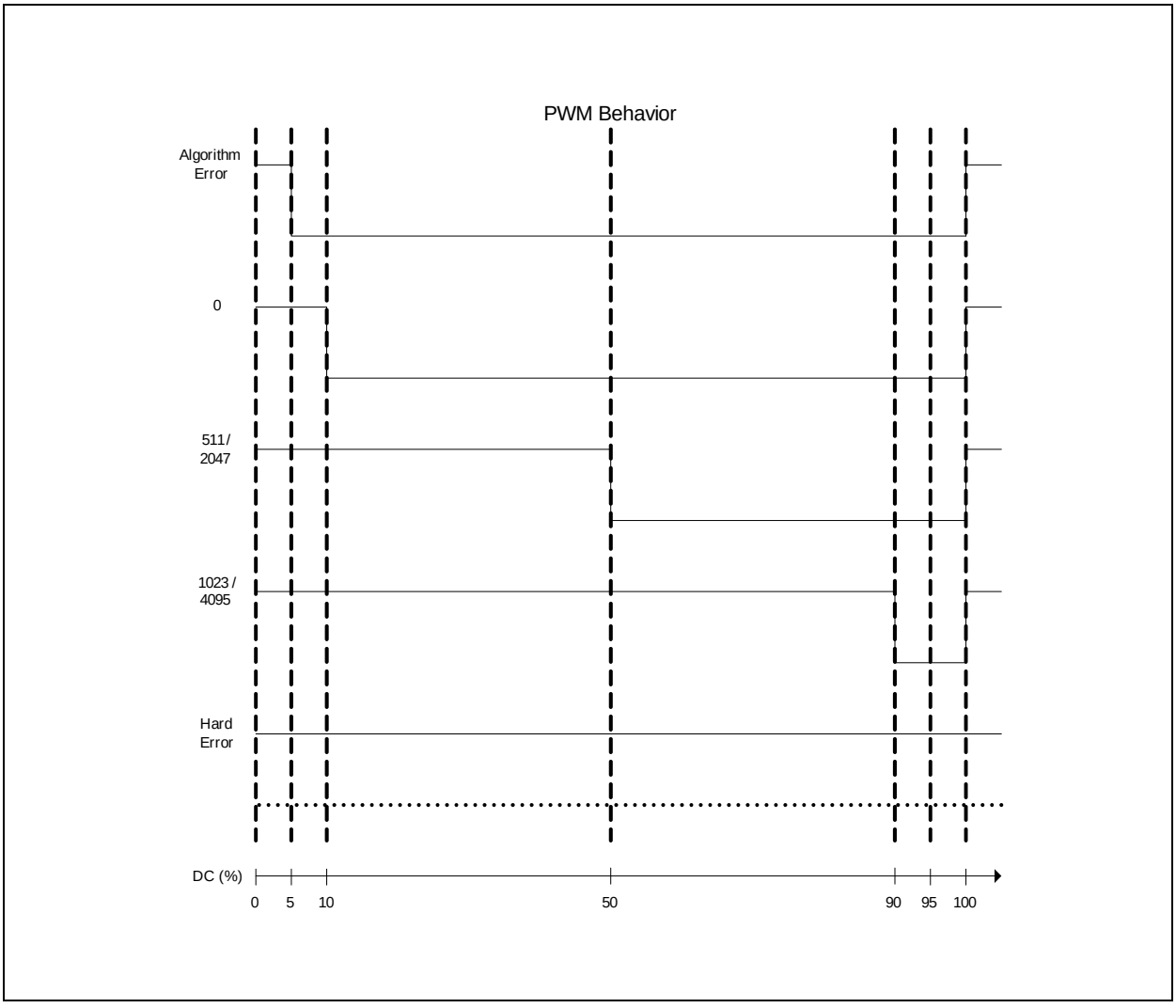
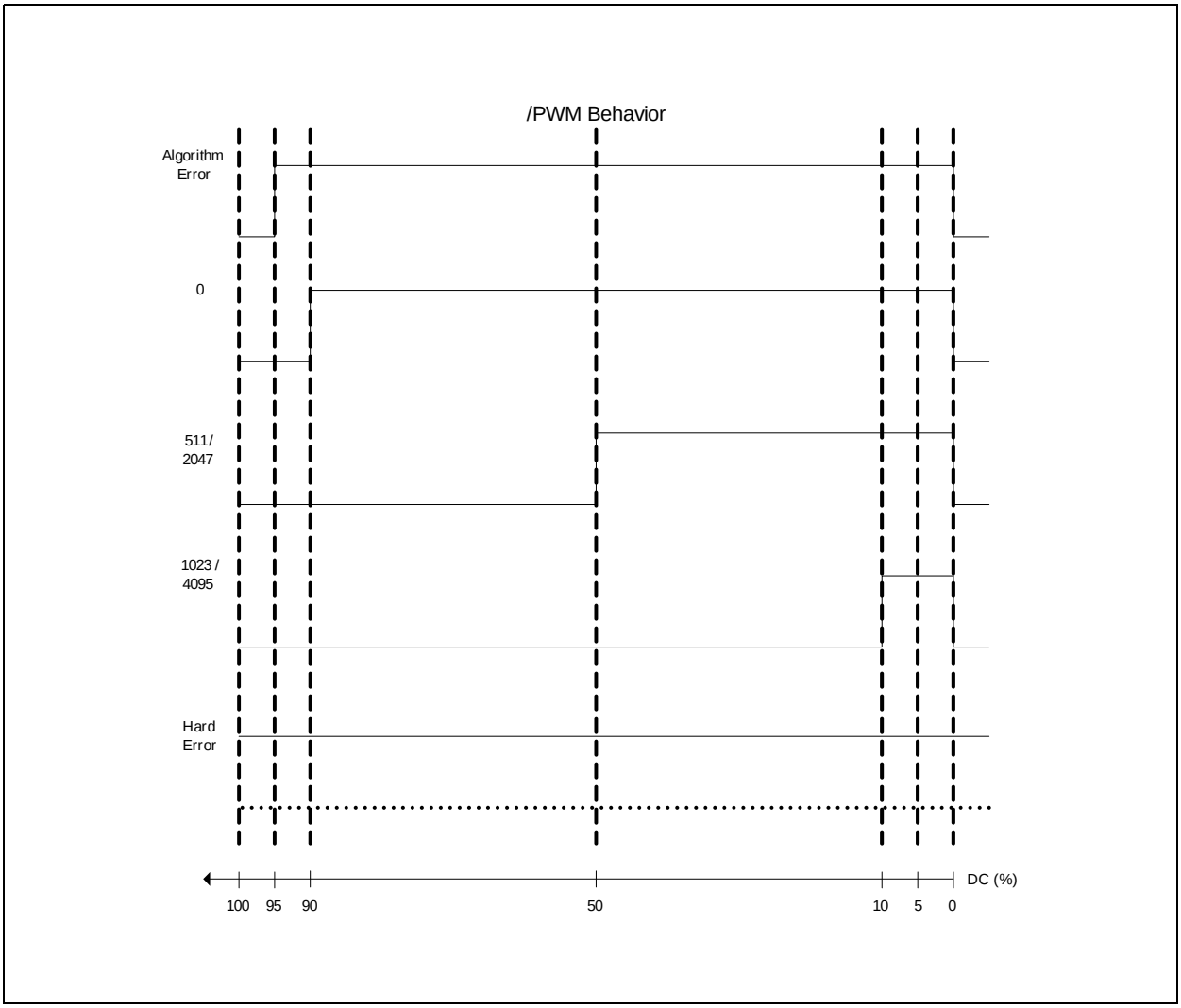
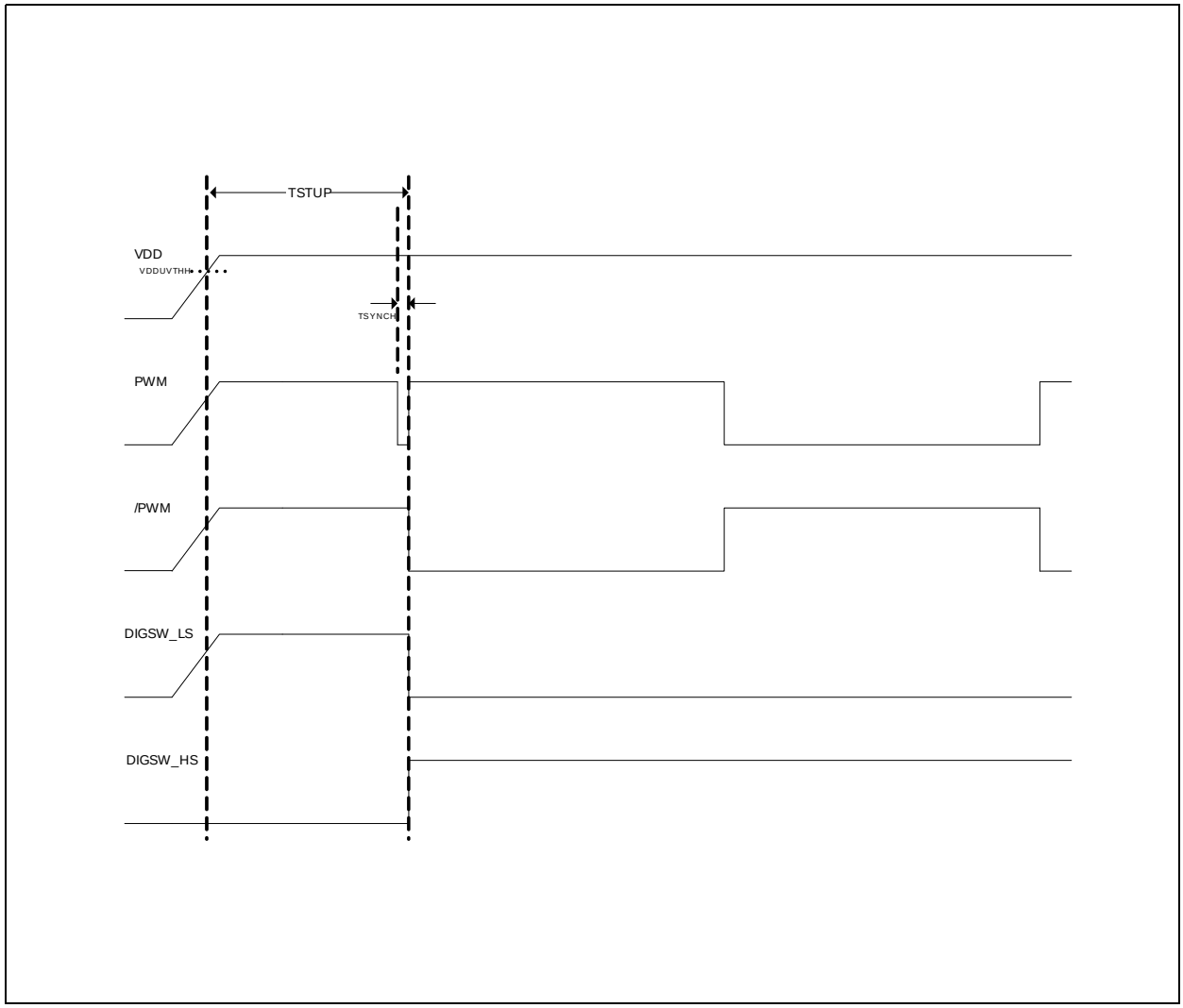


Figure 25:
/PWM Output Signal



At the end of the power up phase, after an under voltage recovery and after the transition from sleep to normal mode a synch pulse with duration T_{SYNCH} precedes the PWM wave as shown in the following picture. Only after the pulse the digital switches leave the HZ state.

Figure 26:
Sync Pulse at PWM After Power-Up



Digital Switch

The AS5403 provides a digital output switch function. This signal can be defined by settings in the EEPROM. The switching point DSW SW POINT <11:0> are compared to the calculated linearized sensor position. The polarity is selectable and the hysteresis is configurable. Possible configurations for DSW selectable from EEPROM bits are:

Figure 27:
Possible Configurations of DSW Pin

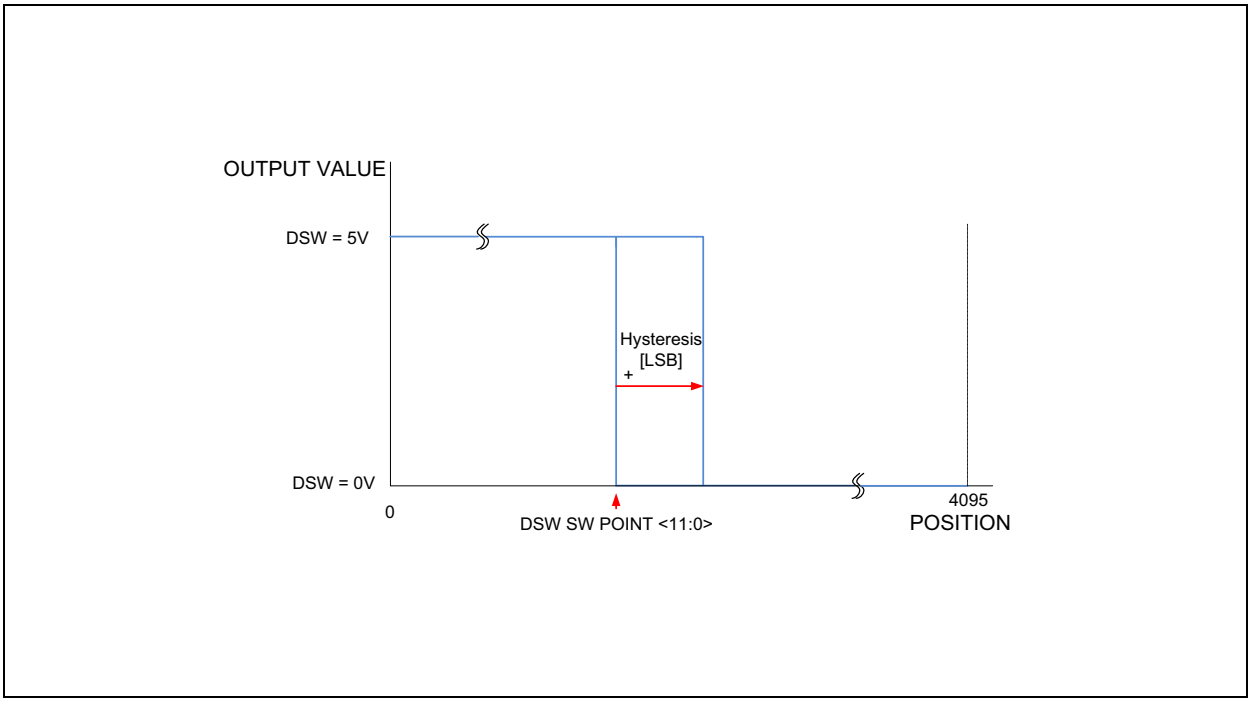
Mode	DSW CFG<2>	DSW CFG <1>	DSW CFG <0>	Comments
Digital switch push/pull	0	0	0	Push-Pull digital output driver external pull up required
Digital switch open source	0	0	1	High side digital driver external pull down required
Digital switch open drain	0	1	0	Low side digital driver external pull up required
PWMn push/pull	0	1	1	Inverted pulse width modulated output with push/pull driver external pull up required
PWMn open drain	1	0	0	Inverted pulse width modulated output with low side driver external pull up required
PWM push/pull	1	0	1	Pulse width modulated output with low side driver external pull up required
PWM open drain	1	1	0	Pulse width modulated output with low side driver external pull up required

Note(s) and/or Footnote(s):

1. All other not specified combinations are reserved and not allowed.

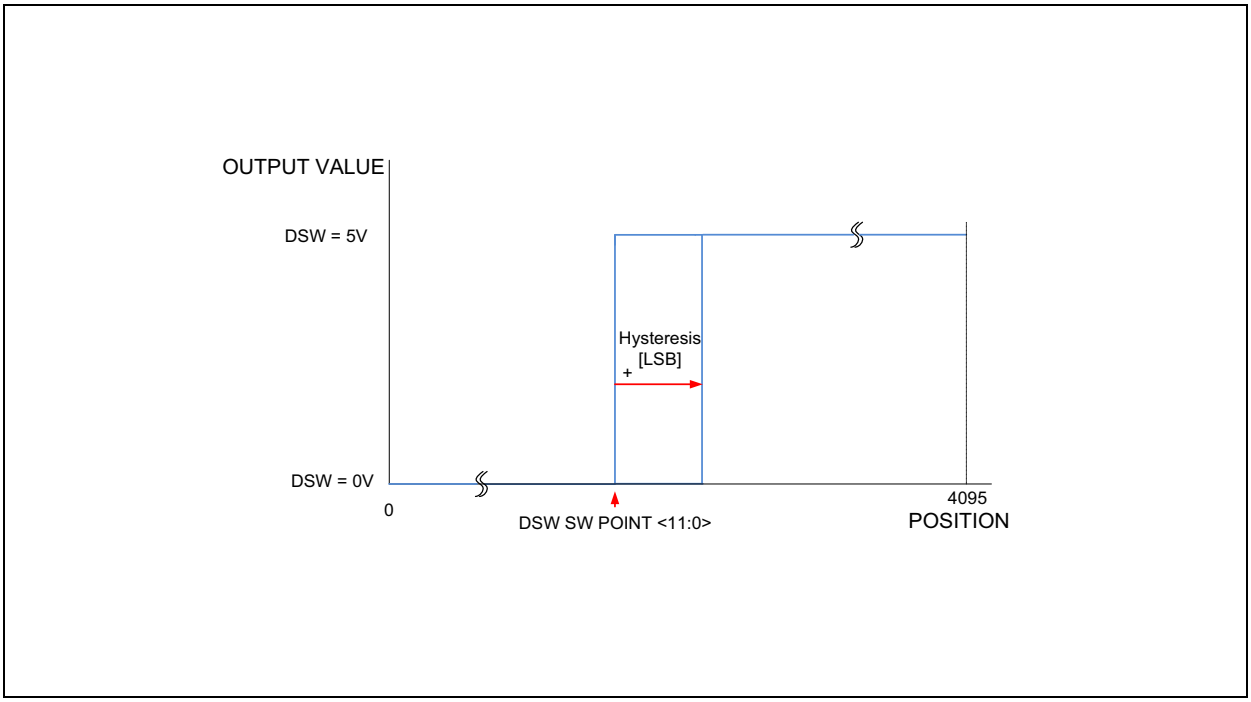
DSW_POL= 1:

Figure 28:
DSW Characteristic With Positive Polarity



DSW_POL=0:

Figure 29:
DSW Characteristic With Negative Polarity



4-Wire Serial Peripheral Interface (SPI)

AS5403 is equipped with a 4wire serial peripheral interface (SPI) to access the EEPROM memory and the read /write registers. SCS input pin (active high) selects the device for serial transfers. Register data is shifted in from the external master on the SDI pin or shifted out from the device on the SDO pin on each subsequent SCLK, in both the cases MSB first. Data are captured on the rising edge and shifted on the falling edge of SCLK for receiving command and transmitting command. An even parity bit is used to check the consistency of the frame. SPI protocol is built by frames; each frame is composed by 4 bytes and it is detected only when SCS pin is high. If a frame contains a number of bits different from the expected the command is not executed.

Valid commands for the SPI interface are the following:

Figure 30:
Commands SPI

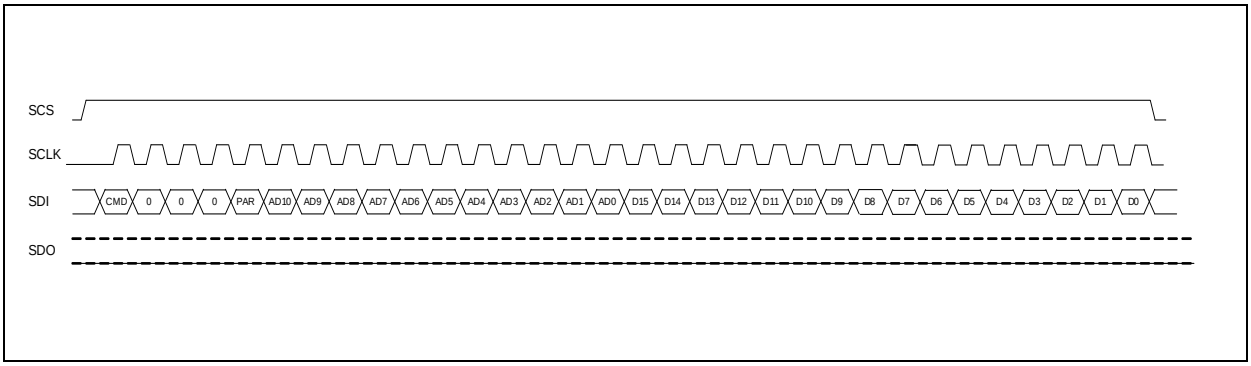
CMD Name	CMD Value	Note	AS5403 Communication Mode
Write	0	Write data in the memory area	SLAVE
Read	1	Read data from the memory area	SLAVE/MASTER

Write (0)

The first byte of the write command is composed by the command identifier (CMD) the even parity bit (PAR) and the MSBs of the address AD<10:8>.

The second byte of the command is the remaining part of the address AD<7:0>, the third and the fourth byte contains the data word we want to write (D<15:0>) on address AD<10:0>. The device forces the SDO pin low. With this command it is possible to access the EEPROM locations and the read/write registers area.

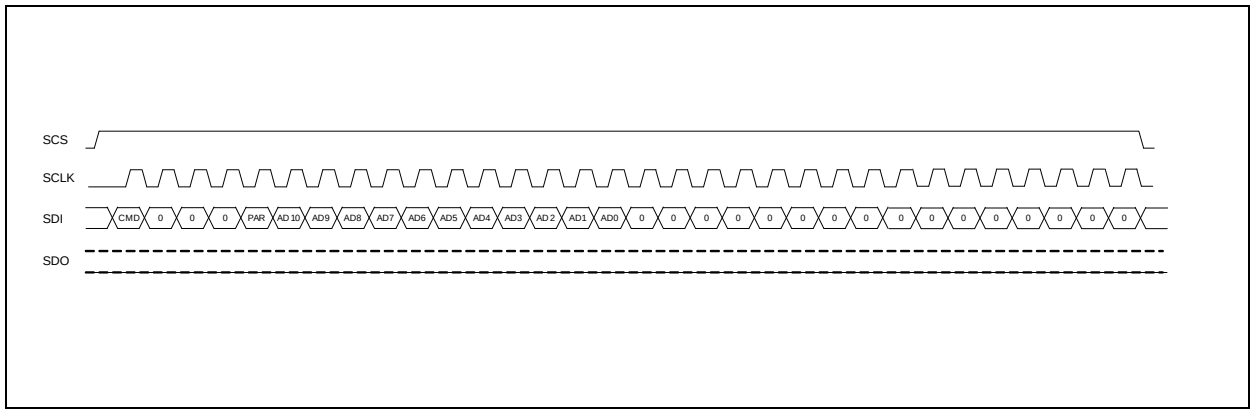
Figure 31:
SPI Write



Read (1)

The read command is composed by 2 frames, in the first one the external master sends the command, the even parity and the address to be read on the SDO line (the last 16 bits are ignored). The device forces the SDO pin low.

Figure 32:
SPI Read



After the switching time (TSCSL) the device drives the SDO line and when the SCS pin goes high starts to send out the answer. The first byte of the second frame is composed by the command the device is executing, the even parity and the MSBs of the address required in the previous frame (AD<10:8>). The second byte of the command is the remaining part of the address AD<7:0>, the third and the fourth bytes are the data word at the required address (AD<10:0>). With this command it is possible to access the EEPROM locations and the read/write registers area.

Programming the AS5403

A standard half duplex UART protocol is used to exchange data with the device in the communication mode.

UART Interface for Programming

The AS5403 uses a standard UART interface with two bytes for address and two bytes for the data content. The read or write mode is selected in the first byte. An even parity for every byte is included. The timing (baud-rate) is selected by the AS5403 over an initial command from the master. The baud rate register can be read and overwritten. The keep synchronization it AS5403 synchronizes art every Start bit. This happens during a standard write access 3 times. A time out function detects not complete commands and resets the AS5403 UART after the timeout period.

Figure 33:
Valid Commands

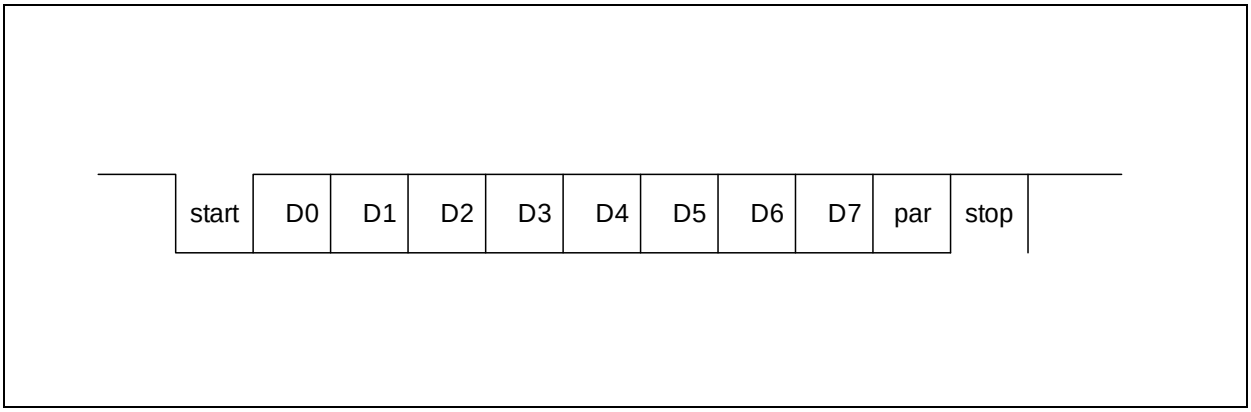
CMD Name	Description	AS5403 Communication Mode
Write	Write data in the EEPROM/ SFR memory	SLAVE
Read	Read data from the EEPROM/ SFR memory	SLAVE/MASTER

In case of Write command the request is followed by the frames containing the data to write.In case of Read command the communication direction will change and the device will answer with the frames containing the data requested.

Frame Organization

The UART frame consists of 1 start bit (low level), 8 data bit, 1 even-parity bit and 1 stop bit (high level). Data are transferred from LSB to MSB.

Figure 34:
General UART Frame



In case of read command the idle phase between the command and the answer is TSW.

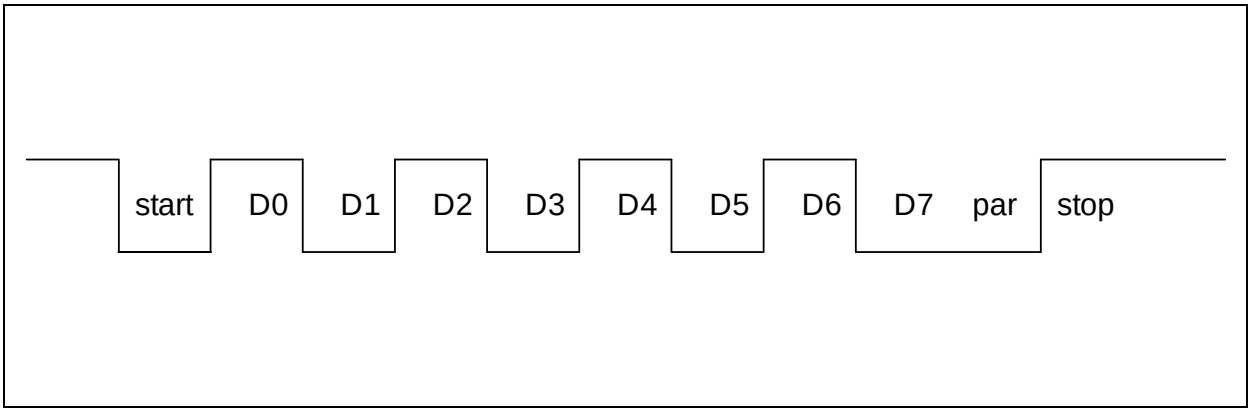
Figure 35:
Bit Assignment in Frame

Symbol	Parameter	Min	Typ	Max	Unit
START	Start bit		1		TBIT
Dx	Data bit		1		TBIT
PAR	Parity bit		1		TBIT
STOP	Stop bit	1			TBIT
TSW	Slave/Master Switch Time		7		TBIT

Each communication starts with the reception of a request from the external controller. The request consists of 3 frames: one synchronization byte and 1 word for the command.

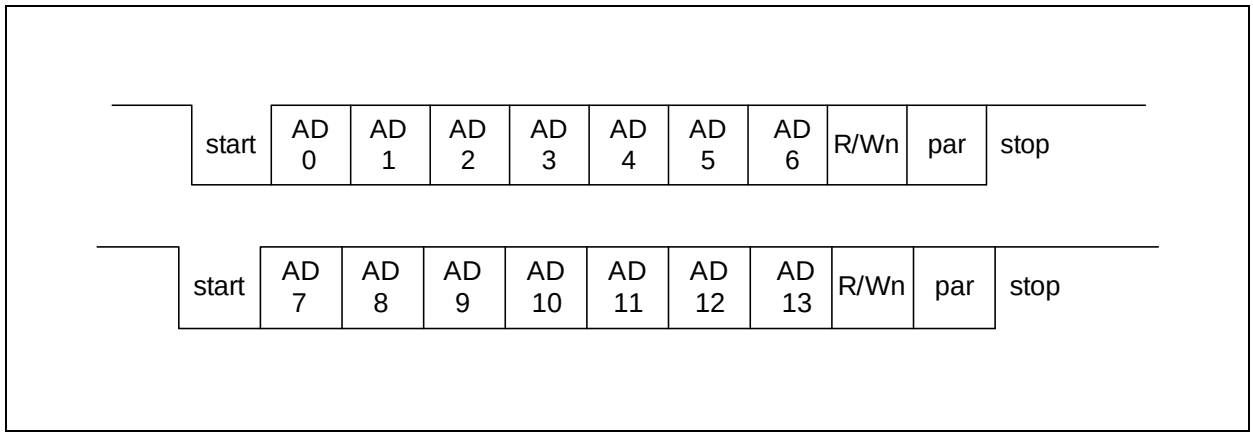
The synchronization frame contains the data 0x55 and allows the UART to measure the external controller baud-rate.

Figure 36:
Synchronization Frame 0x55 Hex



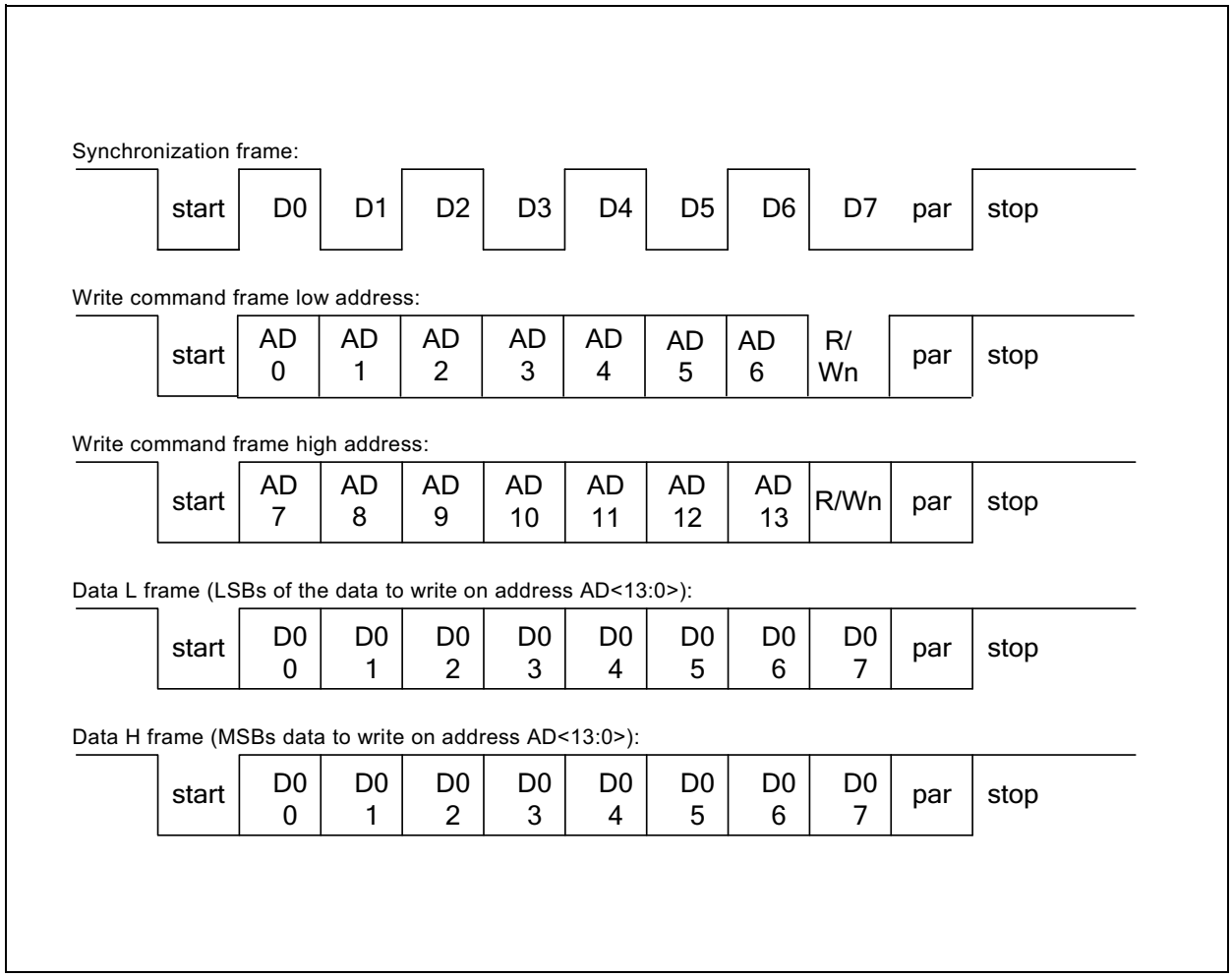
The 2nd and 3rd frames contain the command Read/ Write (1 bit) and the address (7+7 bits):

Figure 37:
2nd and 3rd Frame Addressing



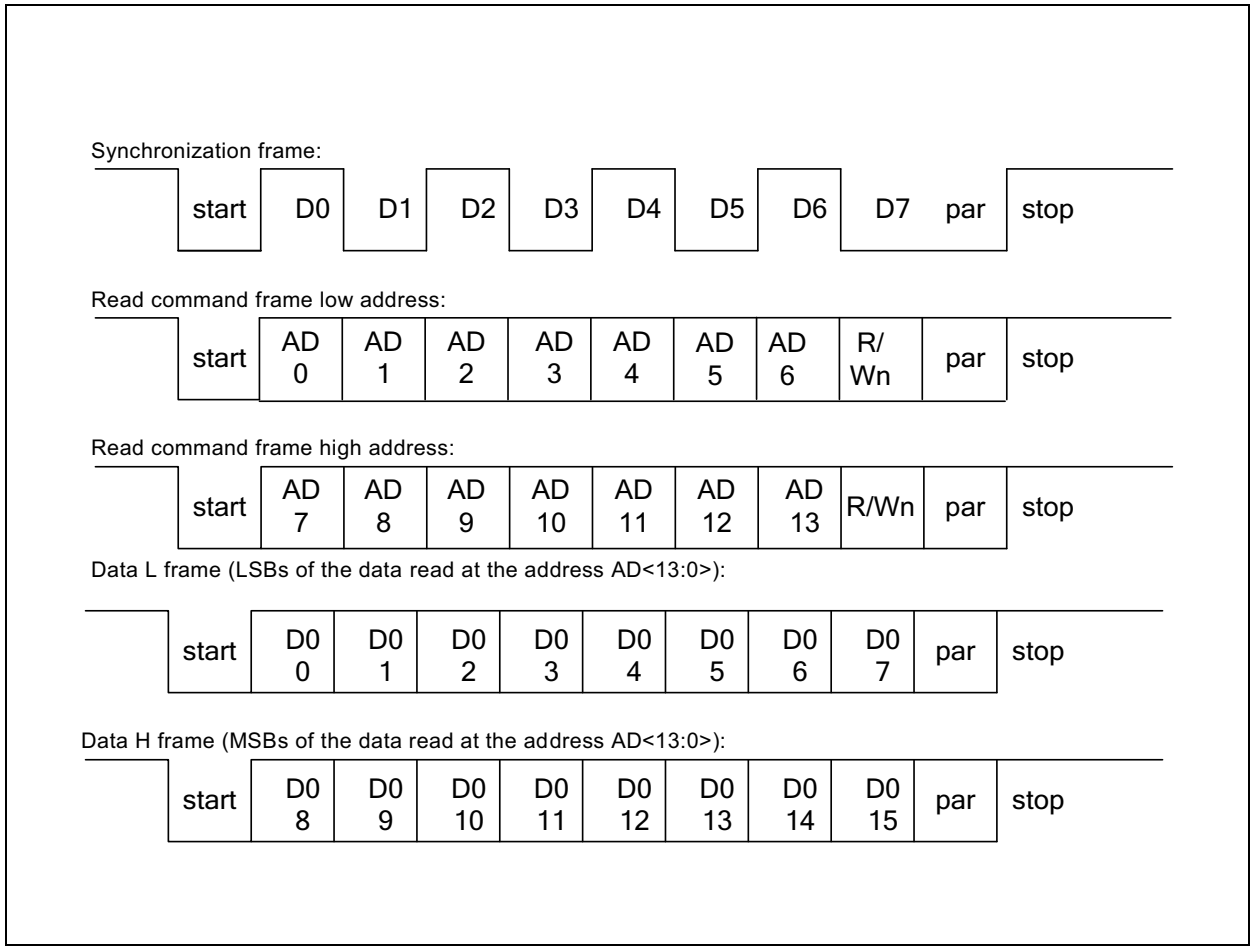
Write Command

Figure 38:
Write Command Frames



Read Command

Figure 39:
Read Command Frames



BAUD RATE Automatic Detection

The UART includes a built-in baud-rate monitor that uses the synchronization frame to detect the external controller baud rate. This baud-rate is used after the synchronization byte to decode the following frame and to transmit the answer and it is stored in the BAUDREG register.

Programming Procedure

The EEPROM programming is possible over the SPI or UART interface. A page write/read mode with 64 pages 8 words each is implemented.

Figure 40:
Page Mode Address

Address	Page
0x000 - 0x007	1
0x008 - 0x00F	2
:	:
0x1F8 - 0x1FF	64

Page Write mode procedure:

1. Write 0x00 on address 0x2FF (START DSP = 0)
2. Write the EEPROM words (SPI/UART) inside a page (min 1 max 8 words)
3. Write 0x0003 on address 0x2FF (CFG_EPP=11)
4. Wait for 10 ms
5. Repeat from 2. for further programming.

It is important that the write access to the selected EEPROM page are consecutive: a write command in a different page or a read command before writing CFG_EPP will delete the data. A writing to factory reserved area will be ignored.

After programming it is mandatory to read back the EEPROM content and to download again the EEPROM to avoid misalignment with the mirror registers. This can be done with a power up or writing 0x0004 on address 0x2FF (EE_DWNL SFR).

The programming procedure is not allowed in case Customer Lock word is 0x55AA after EEPROM download (mask_fuse=1).

Lock Procedure and Signature Calculation

The AS5403 contains a signature diagnostic function for the EEPROM. This signature is calculated in the AS5403 during power up and is compared to the calculated signature directly after the end of line calibration by the customer. A deviation leads to an error indication in the diagnostic flag or into the failure band mode at the output. The signature check is enabled in case of a locked device by the user.

Device Configuration

AS5403 is equipped with a 1kx8 EEPROM memory to store the factory settings and the customer configuration data. The device can be configured using the UART or 4wire Serial Peripheral Interface (SPI).

EEPROM Memory Map

Note(s): Write 0x0000 hex to register address 0x2FF (START DSP = 0) before a read or write access to EEPROM.

Figure 41:
EEPROM Memory Map

ADDRESS (HEX)	EEPROM Location Name
0x00B	Sequencer Control
0x00F	Magnet Lost threshold and hysteresis
0x019	Offset Bj
0x01A	Gain Bj
0x01E	Gain Bi
0x01F	Offset Bi
0x05F	Linearization table entry 16
0x060	Linearization table entry 0
0x061	Linearization table entry 1
0x062	Linearization table entry 2
0x063	Linearization table entry 3
0x064	Linearization table entry 4
0x065	Linearization table entry 5
0x066	Linearization table entry 6
0x067	Linearization table entry 7
0x068	Linearization Table entry 8
0x069	Linearization table entry 9
0x06A	Linearization table entry 10
0x06B	Linearization table entry 11
0x06C	Linearization table entry 12
0x06D	Linearization table entry 13
0x06E	Linearization table entry 14
0x06F	Linearization table entry 15
0x070	Linearization table entry -16

ADDRESS (HEX)	EEPROM Location Name
0x071	Linearization table entry -15
0x072	Linearization table entry -14
0x073	Linearization table entry -13
0x074	Linearization table entry -12
0x075	Linearization table entry -11
0x076	Linearization table entry -10
0x077	Linearization table entry -9
0x078	Linearization table entry -8
0x079	Linearization table entry -7
0x07A	Linearization table entry -6
0x07B	Linearization table entry -5
0x07C	Linearization table entry -4
0x07D	Linearization table entry -3
0x07E	Linearization table entry -2
0x07F	Linearization table entry -1
0x1CF	Pre-Scale linearization
0x1D0	Post-Processing offset
0x1D1	Post-Processing gain
0x1D2	Clamp Low 1
0x1D3	Clamp High 1
0x1F5	Clamp high 2 (MSBs), clamp low 2
0x1F6	Clamp high 2 (LSBs)
0x1F7	Angle offset
0x1F8	Customer LOCK
0x1F9	Output configuration and PWM frequency
0x1FA	DSW driver configuration
0x1FB	DSW settings
0x1FC	Customer ID
0x1FD	Customer ID
0x1FE	Customer ID
0x1FF	EEPROM signature + customer ID

Figure 42:
EEPROM Sequencer Control 0x00B

Register Hex	Access	Bit	Function	Default	Note
0x00B	R/W	D15 (MSB)	Reserved	0	
		D14			
		D13			
		D12	ExtRng	0	Extended Range (for differential mode): 0 = disabled 1 = enabled
		D11	Reserved	0	
		D10	Swap	0	Swap Bi and Bj before angle calculation
		D9	Reserved	0	
		D8	Reserved	0	
		D7	Table Select <1>	0	These bits allow the selection of 3 different operating modes, stored in 3 individual sequencer tables. Don't use 11 --> no operation
		D6	Table Select <0>	1	
		D5	Reserved	0	
		D4	DIFF	0	Differential mode: 0 = absolute measurement of one pixel 1 = differential measurement of both pixels
		D3	Reserved	0	
		D2	SeqEn	1	1 = Sequencer enabled 0 = Sequencer disabled
		D1	AVG	1	Average mode: 0 = absolute measurement of one pixel, 1 = average measurement of both pixels
		D0 (LSB)	Reserved	0	

Figure 43:
Possible Table Selection AS5403A and AS5403D

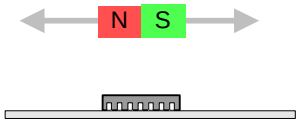
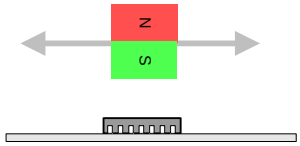
	Table 0 Table Select 00	Table 1 Table Select 01	Table 2 Table Select 10
Sensor arrangement	X/Z	X/Z	X/Z
EEPROM 0x00B settings	Absolute Mode Pixel1 1 kHz Sampling Rate	Differential/Average Mode 1 kHz Sampling Rate	Differential/Average Mode 1 kHz Sampling Rate
Magnet orientation			

Figure 44:
Possible Table Selection AS5403E

	Table 0 Table Select 00	Table 1 Table Select 01	Table 2 Table Select 10
Sensor arrangement	X/Y	X/Y	X/Y
EEPROM 0x00B settings	Differential/Average Mode 1 kHz Sampling Rate	Absolute Mode 1 kHz Sampling Rate	Absolute Mode 0.125 kHz Sampling Rate
Magnet orientation	Off-axis (ring magnet or sector magnet)		

Figure 45:
EEPROM Magnet Lost 0x00F

Register Hex	Access	Bit	Function	Default	Note
0x00F	R/W	D15 (MSB)	Reserved	0	
		:		:	
		D11		0	
		D10	MgnLostHyst<2>	1	Magnet lost hysteresis
		:	:	:	
		D8	MgnLostHyst<0>	0	
		D7	MgnLostLmt<7>	0	Magnet lost threshold value compared to register 0x520
		:	:	:	
		D0 (LSB)	MgnLostLmt<0>	0	

The magnitude information is compared with the magnet lost threshold value calculated with following formula:

$$MagnetLostLimit = MgnLostLmt\ <7:0> * 64$$

The hysteresis is calculated using following formula:

$$Hysteresis = MagnetLost\ Limit * \frac{1}{2^{MgnLostHyst\ <2:0>}}$$

MgnLostHyst<2:0>=0 disables the hysteresis

Figure 46:
EEPROM Offset Bj 0x019

Register Hex	Access	Bit	Function	Default	Note
0x019	R/W	D15 (MSB)	Offset Bj	0	Offset to the Bj value to improve performance Signed integer, range [-32768;32767]
		:			
		D0 (LSB)			

Figure 47:
EEPROM Offset Bi 0x01F

Register Hex	Access	Bit	Function	Default	Note
0x01F	R/W	D15 (MSB) : D0 (LSB)	Offset Bi	0	Offset to the Bi value to improve performance Signed integer, range [-32768;32767]

Figure 48:
EEPROM Gain Bj 0x01A

Register Hex	Access	Bit	Function	Default	Note
0x01A	R/W	D15 (MSB) : D0 (LSB)	Gain Bj	+1 decimal	Gain to the Bj value Signed integer, range [-1;1]

Figure 49:
EEPROM Gain Bi 0x01E

Register Hex	Access	Bit	Function	Default	Note
0x01E	R/W	D15 (MSB) : D0 (LSB)	Gain Bi	+1 decimal	Gain to the Bj value Signed integer, range [-1;1]

Figure 50:
EEPROM Linearization Table 0x05F to 0x07F

Register Hex	Access	Bit	Content	Default	Note
0x05F	R/W	D15 to D0	Angle linearization table, value 16	0000	Signed integer [-1;1]
0x060			Angle linearization table, value 0		
0x061			Angle linearization table, value 1		
:			…		
0x06F			Angle linearization table, value 15		
0x070			Angle linearization table, value -16		
0x071			Angle linearization table, value -15		
:			…		
0x07E			Angle linearization table, value -2		
0x07F			Angle linearization table, value -1		

Figure 51:
EEPROM Pre-Scale Linearization 0x1CF

Register Hex	Access	Bit	Function	Default	Note
0x1CF	R/W	D15 (MSB)	Pre-Scale linearization Factor	+1 decimal	Signed integer [-8;8]
		:			
		D0 (LSB)			

Figure 52:
EEPROM Post-Processing Offset 0x1D0

Register Hex	Access	Bit	Function	Default	Note
0x1D0	R/W	D15 (MSB)	Post processing offset	0	Signed integer [-32768;32767]
		:			
		D0 (LSB)			

Figure 53:
EEPROM Post-Processing Gain 0x1D1

Register Hex	Access	Bit	Function	Default	Note
0x1D1	R/W	D15 (MSB)	Post processing gain	+1 decimal	Signed integer [-4;4]
		:			
		D0 (LSB)			

Figure 54:
EEPROM Clamp Low 1 0x1D2

Register Hex	Access	Bit	Function	Default	Note
0x1D2	R/W	D15 (MSB)	Clamp Low 1	-32768 decimal	Signed integer [-32768;32767]
		:			
		D0 (LSB)			

Figure 55:
EEPROM Clamp High 1 0x1D3

Register Hex	Access	Bit	Function	Default	Note
0x1D3	R/W	D15 (MSB)	Clamp High 1	32767 decimal	Signed integer [-32768;32767]
		:			
		D0 (LSB)			

Figure 56:
EEPROM Clamp Low 2 and Clamp High 2 (LSBs) 0x1F5

Register Hex	Access	Bit	Function	Default	Note
0x1F5	R/W	D15 (MSB)	Clamp High 2 (LSBs)	0	Clamp High 2 (LSBs) value for PWM and analog output. DSW not effected. 4 lower LSBs [0;16]
		:		:	
		D12		0	
		D11	Clamp Low 2	0	Clamp Low 2 value for PWM and analog output. DSW not effected. 12 bit unsigned value [0;4096]
		:		:	
		D0 (LSB)		0	

Figure 57:
EEPROM Clamp High 2 (MSBs) 0x1F6

Register Hex	Access	Bit	Function	Default	Note
0x1F6	R/W	D15 (MSB)	Reserved	0	
		:		:	
		D8		0	
		D7	Clamp High 2 (MSBs)	0	Clamp High 2 (MSBs) value for PWM and analog output. DSW not effected. 8 higher MSBs [0;256]
		:		:	
		D0 (LSB)		0	

Figure 58:
EEPROM Angle Offset 0x1F7

Register Hex	Access	Bit	Function	Default	Note
0x1F7	R/W	D15 (MSB)	Angle Offset	0	Signed integer [-32768;32767]
		:			
		D0 (LSB)			

Figure 59:
EEPROM Customer Lock 0x1F8

Register Hex	Access	Bit	Function	Default	Note
0x1F8	R/W	D15 (MSB)	Customer Lock	0	EEPROM lock key region. When key 0x55AA is programmed --> no more write access to complete EEPROM
		:			
		D0 (LSB)			

Figure 60:
EEPROM OUT Pin Configuration and PWM Frequency 0x1F9

Register Hex	Access	Bit	Function	Default	Note
0x1F9	R/W	D15 (MSB)	OUT FALL <1>	0	Threshold for the fall time check. 00 = no check 01 = 24 to 28 µs 10 = 56 to 60 µs 11 = 120 to 124 µs
		D14	OUT FALL <0>	0	
		D13	OUT RISE <1>	0	Threshold for the rise time check. 00 = no check 01 = 24 to 28 µs 10 = 56 to 60 µs 11 = 120 to 124 µs
		D12	OUT RISE <0>	0	
		D11	Reserved	0	
		D10	OUT CFG <2>	0	Output driver configuration OUT pin
		:	:	:	
		D8	OUT CFG <0>	0	
		D7	Reserved	0	
		:		:	
		D3		0	
		D2	DIAG_HIGH	0	Failure band selection internal errors 0=Failure band low 1= Failure band high
		D1	PWMF <1>	0	PWM frequency selection 00 = 1 kHz. Don't use other settings except AS5403E 11=0.125kHz in case of Table Select = 10
		D0 (LSB)	PWMF <0>	0	

Figure 61:
EEPROM DSW Pin Configuration 0x1FA

Register Hex	Access	Bit	Function	Default	Note
0x1FA	R/W	D15 (MSB)	DSW SW POINT <7:0>	0	Low byte of the switching point
		:		:	
		D8		0	
		D7	DSW FALL <1>	0	Threshold for the fall time check. 00 = no check 01 = 24 to 28 µs 10 = 56 to 60 µs 11 = 120 to 124 µs
		D6	DSW FALL <0>	0	
		D5	DSW RISE <1>	0	Threshold for the rise time check. 00 = no check 01 = 24 to 28 µs 10 = 56 to 60 µs 11 = 120 to 124 µs
		D4	DSW RISE <0>	0	
		D3	Reserved	0	
		D2	DSW CFG <2>	0	Output driver configuration DSW pin. See Figure 23
		D1	:	0	
		D0 (LSB)	DSW CFG <0>	0	

Figure 62:
EEPROM DSW Settings 0x1FB

Register Hex	Access	Bit	Function	Default	Note
0x1FB	R/W	D15 (MSB)	Reserved	0	
		D14	Reserved	0	
		:		0	
		D10		0	
		D9	Reserved	0	
		D8	Reserved	0	
		D7	DSW_POL	0	Polarity: 0 = low level 1 = high level
		D6	DSW HYST <2>	0	DSW Hysteresis: 000 = 4 LSB; 001 = 8 LSB; 010 = 16 LSB; 011 = 32 LSB; 100 = 48 LSB; 101 = 64 LSB; 110 = 96 LSB; 111 =128 LSB; LSB are on 12 bits
		:	:	0	
		D4	DSW HYST <0>	0	
		D3	DSW SW POINT <11>	0	Upper 4 bits of the switching point
		:	:	:	
		D0 (LSB)	DSW SW POINT <8>	0	

Figure 63:
EEPROM Customer ID 0x1FC

Register Hex	Access	Bit	Function	Default	Note
0x1FC	R/W	D15 (MSB)	CUST ID	0	Customer ID number 7 to 0
		:		:	
		D8		0	
		D7	CUST ID	0	Extended Byte
		:		:	
		D0 (LSB)		0	

Figure 64:
EEPROM Customer ID 0x1FD

Register Hex	Access	Bit	Function	Default	Note
0x1FD	R/W	D15 (MSB)	CUST ID	0	Customer ID number 23 to 8
		:		:	
		D0 (LSB)		0	

Figure 65:
EEPROM Customer ID 0x1FE

Register Hex	Access	Bit	Function	Default	Note
0x1FE	R/W	D15 (MSB)	CUST ID	0	Customer ID number 39 to 24
		:		:	
		D0 (LSB)		0	

Figure 66:
EEPROM Customer ID and Signature 0x1FF

Register Hex	Access	Bit	Function	Default	Note
0x1FF	R/W	D15 (MSB)	EESIGN	0	EEPROM Signature
		:		:	
		D8		0	
		D7	CUST ID	0	Customer ID number 47 to 40
		:		:	
		D0 (LSB)		0	

Register Memory Map

Note(s): Register Memory Map Write 0x0100 hex to register address 0x2FF (START DSP = 1) before a read of following registers.

Figure 67:
Register Map

Address (Hex)	Register Location Name
0x2FF	Control DSP
0x300	Error Register 1
0x301	Position 2
0x302	Error Register 2
0x510	Temperature
0x511	Measurement Value 1 (MV 1)
0x512	Measurement Value 2 (MV 2)
0x513	Measurement Value 3 (MV 3)
0x514	Measurement Value 4 (MV 4)
0x520	Magnitude
0x521	Angle (not linearized)
0x522	Angle linearized
0x547	Position 1
0x548	Bi component
0x549	Bj component
0x54B	Bi' component
0x54C	Bj' component
0x54D	Bk (unused)

Figure 68:
Control DSP 0x2FF

Register Hex	Access	Bit	Function	Note
0x2FF	R/W	D15 (MSB)	Reserved	
		:		
		D12		
		D11	PASS2FUNC	Activation for functional mode of the output.
		D10	FREEZE	When CAL_EN=1 it enables the 3D Hall Core for 1 only measurement (automatically cleared at the end of the measurement). Used For SPI calibration in communication mode. When CAL_EN=0 it freezes the read SFR content
		D9	CAL_EN	Enable the calibration procedure. Used in communication mode.
		D8	START_DSP	Start the 3D Hall Core. Used in communication mode to start the DSP measurements.
		D7	Reserved	
		:		
		D4		
		D3	EE_RESET	Force EEPROM reset. Used in communication mode.
		D2	EE_DWNL	Force EEPROM download. Used in communication mode.
		D1	CFG_EPP <1>	EEPROM programming mode: 00: no EEPROM permanent write; 11: permanent write of the current EEPROM page (bits CFG_EPP are automatically cleared); 01: permanent write after each EEPROM write command.
		D0 (LSB)	CFG_EPP <0>	

Figure 69:
Error Register 1 0x300

Register Hex	Access	Bit	Function	Note
0x300	R	D15 (MSB)	Reserved	
		D14	MgnLost	Magnet Lost: it indicates that Magnitude is below the configured threshold (magnet is too far away) (EEPROM 0x00F)
		D13	DiPaSeMo	Digital Part Self-Monitoring fail: it indicates that the digital part self-monitoring detected an error.
		D12	NrmOvfl	Normalization Overflow: it indicates the multiplier overflow during normalization.
		D11	SensOvfl	Sensitivity Correction Overflow: it indicates the Multiplier overflow during sensitivity correction over temperature
		D10	RngWarn	Range Warning: it indicates that the ADC input signal exceeds the input range.
		D9	Reserved	
		D8	CalcError	Calculation Error: it indicates that an overflow in post-processing calculations occurred.
		D7	Reserved	
		D6	SLOvfl	Linearization Overflow: it indicates that the multiplication in front of the linearization saturated.
		D5	GainSat	Gain Multiplication Saturation: it indicates that the result of the gain multiplication saturated.
		D4	ClampStatus 1	Clamp Status 1: it indicates that the post-processing used the clamping values to limit the output value.
		D3	ClampStatus 2	Clamp Status 2: it indicates that the unsigned post-processing used the clamping values to limit the PWM/Analog value.
		D2	Reserved	
		:		
		D0 (LSB)		

Figure 70:
Error Register 2 0x302

Register Hex	Access	Bit	Function	Note
0x302	R	D15 (MSB)	Reserved	
		:		
		D11		
		D10	WD_ERR	Watchdog error
		D9	DWL_BIST_ER	EEPROM signature error is generated during the download into SFR mirror
		D8	TST_ERR	Signature error on TEST SFR (they should be at 0 during functional mode
		D7	SYNCH_ERR	Synchronization error between 3D Hall Core data rate and PWM frequency
		D6	Reserved	
		D5	RD_BACK_ERR2	Read back error on DSW pin
		D4	RD_BACK_ERR1	Read back error on OUT pin
		D3	Reserved	
		D2	DSW_SHORT	Short circuit error on DSW pin
		D1	PWM_SHORT	Short circuit error on OUT pin
		D0 (LSB)	BIST_ERR	EEPROM signature error

Figure 71:
Register Temperature 0x510

Register Hex	Access	Bit	Function	Note
0x510	R	D15 (MSB)	Temperature	Temperature [°C] = (17325 + value [LSB])/ 315
		:		
		D0 (LSB)		

Figure 72:
Register Measurement Value 1to 4 MV1 to MV4 0x511, 0x512, 0x513, 0x514

Register Hex	Access	Bit	Function	Note
0x511 0x512 0x513 0x514	R	D15 (MSB) : D0 (LSB)	MV1 MV2 MV3 MV4	Measurement values of 3D Hall Pixels

Figure 73:
Register Magnitude 0x520

Register Hex	Access	Bit	Function	Note
0x520	R	D15 (MSB) : D0 (LSB)	Magnitude	Magnitude information after ATAN calculation

Figure 74:
Register Angle not Linearized 0x521

Register Hex	Access	Bit	Function	Note
0x521	R	D15 (MSB) : D0 (LSB)	Angle	Angle information after CORDIC calculation

Figure 75:
Register Angle Linearized 0x522

Register Hex	Access	Bit	Function	Note
0x522	R	D15 (MSB) : D0 (LSB)	Angle linearized	Angle information after linearization. 16 bit linearized output

Figure 76:
Register Position 1 0x547

Register Hex	Access	Bit	Function	Note
0x547	R	D15 (MSB) : D0 (LSB)	Position 1	Position 1 value signed output

Figure 77:
Register Position 2 0x301

Register Hex	Access	Bit	Function	Note
0x301	R	D15 (MSB) : D0 (LSB)	Position 2	Position 2 value unsigned output 12 bit number MSBs = zero

Figure 78:
Register Bi Component 0x548

Register Hex	Access	Bit	Function	Note
0x548	R	D15 (MSB) : D0 (LSB)	Bi	Magnetic field component Bi. Content dependant on sequencer control settings and table selection

Figure 79:
Register Bj Component 0x549

Register Hex	Access	Bit	Function	Note
0x549	R	D15 (MSB) : D0 (LSB)	Bj	Magnetic field component Bj. Content dependant on sequencer control settings and table selection

Figure 80:
Register Bi' Component 0x54B

Register Hex	Access	Bit	Function	Note
0x54B	R	D15 (MSB) : D0 (LSB)	Bi'	Magnetic field component Bi'. Content dependant on sequencer control settings and table selection

Figure 81:
Register Bj' Component 0x54C

Register Hex	Access	Bit	Function	Note
0x54C	R	D15 (MSB) : D0 (LSB)	Bj'	Magnetic field component Bj'. Content dependant on sequencer control settings and table selection

Temperature Sensor

The on chip temperature sensor can be used to gain rough information about the ambient temperature. The SPI interface is mandatory when this information shall be used.

Figure 82:
Temperature Sensor

Parameter	Conditions	Min	Typ	Max	Unit
Temperature Signal	@ 0°C		-17325		LSB
Temperature Sensor Resolution			315		LSB/K

Protections

When the voltage applied to the VDD pin falls below the undervoltage lower threshold (VDDUVTL) for longer than the TVDDUVDET time the device stops the clock of the digital part, it resets the EEPROM signature calculation and the 3D Hall core and the output drivers are turned off to reduce the power consumption. When the voltage applied to the VDD pin exceeds the VDD undervoltage upper threshold (VDDUVTH) for longer than the TVDDUVREC time the clock, the signature calculation and the 3D Hall core are restarted and the output drivers are turned ON.

Figure 83:
Single Wire Bit Timing

Symbol	Parameter	Min	Typ	Max	Unit
VDDUVTH	VDD Undervoltage Upper Threshold	3.7	4.1	4.5	V
VDDUVTL	VDD Undervoltage Lower Threshold	3.3	3.7	4.1	V
TVDDUVDET	VDD Undervoltage Detection Time	10		250	µs
TVDDUVREC	VDD Undervoltage Recovery Time	10		250	µs

Sensor Placement

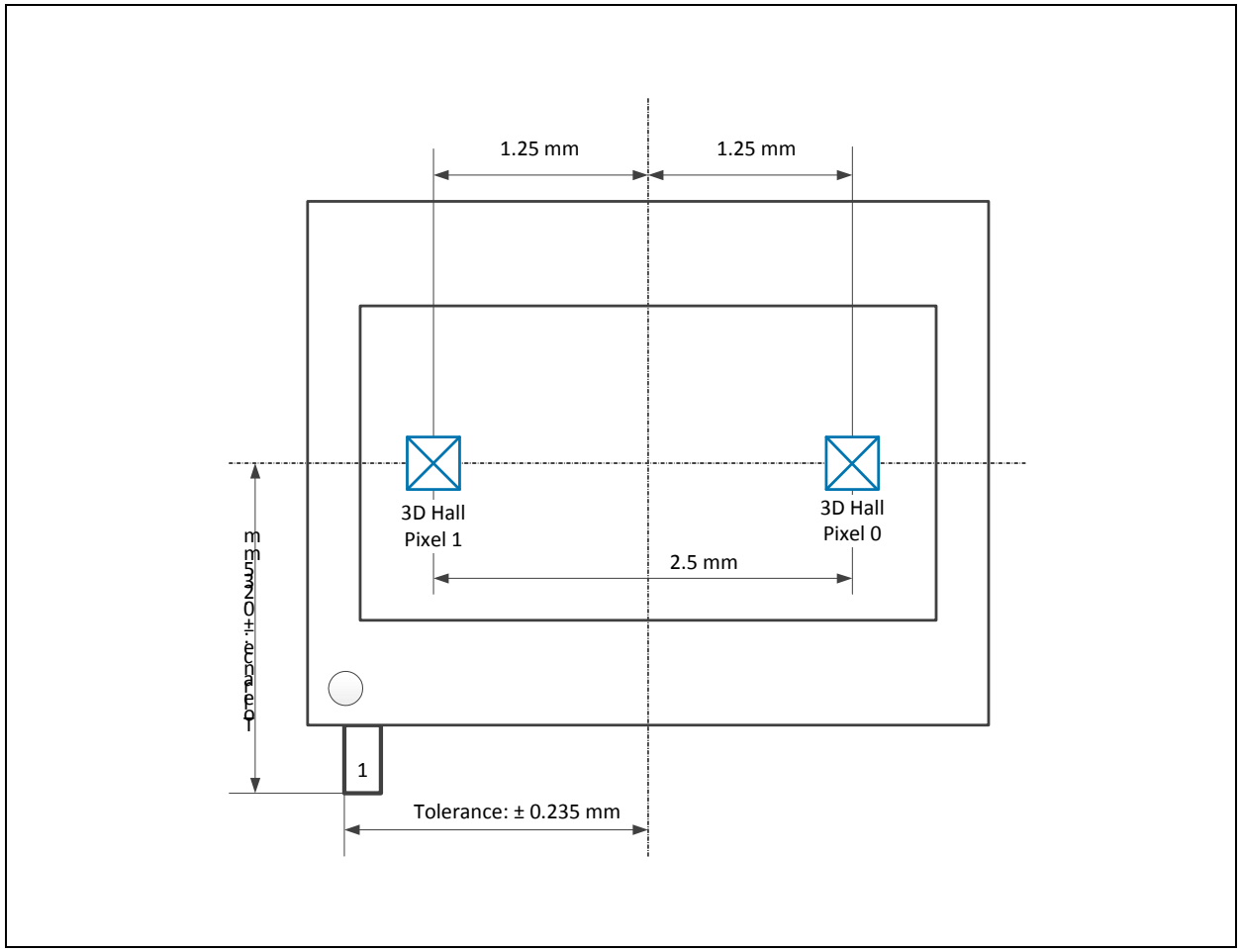
Two 3D Hall pixels each with an X-/Y-/Z-sensor are arranged in a line on the X-axis parallel to the chip edge, 2.5mm distant from each other.

3D Hall pixel positions relative to chip centre are:

Pixel 1: -1250 µm

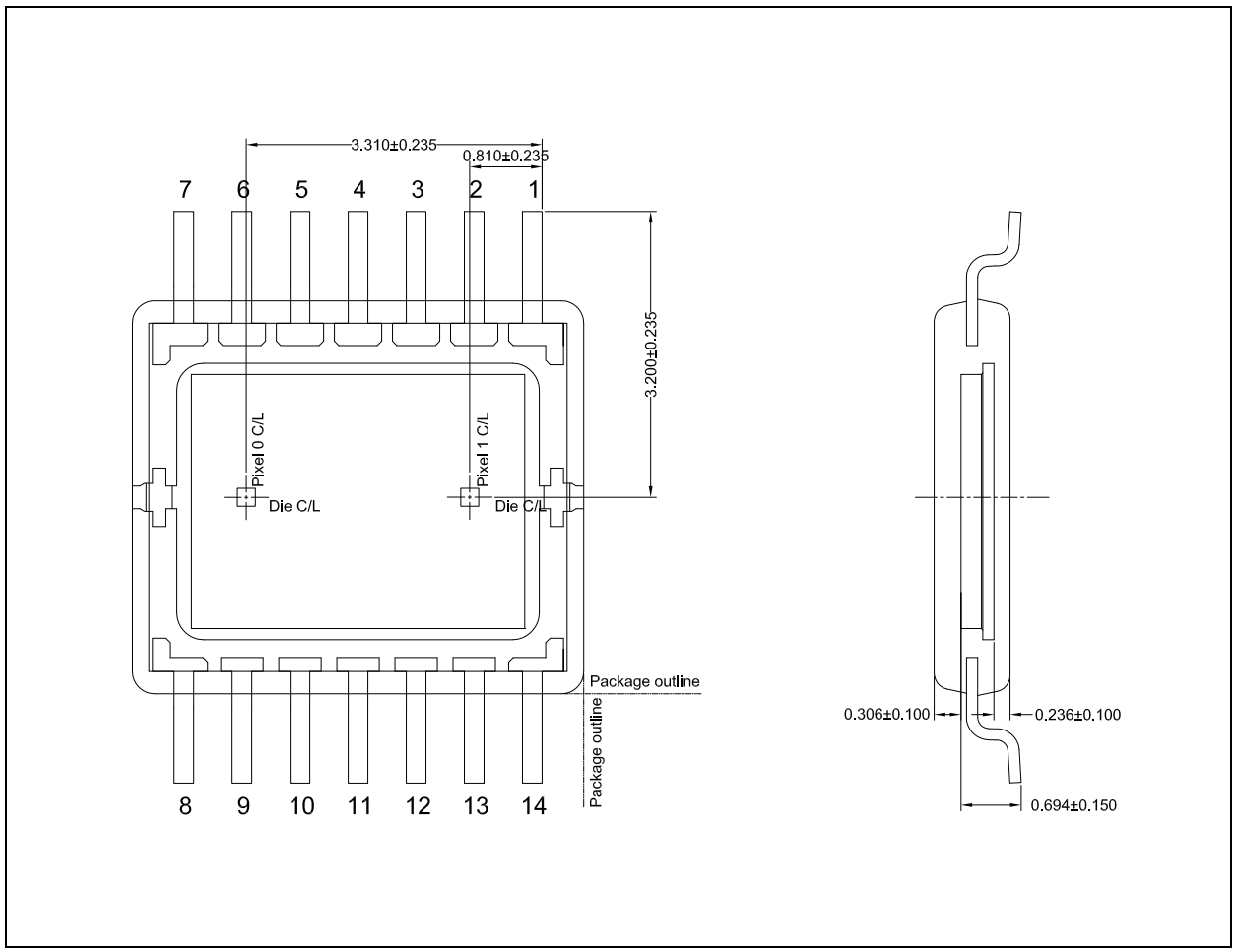
Pixel 0: 1250 µm

Figure 84:
3D Hall Pixel Arrangement



Package Drawings & Markings

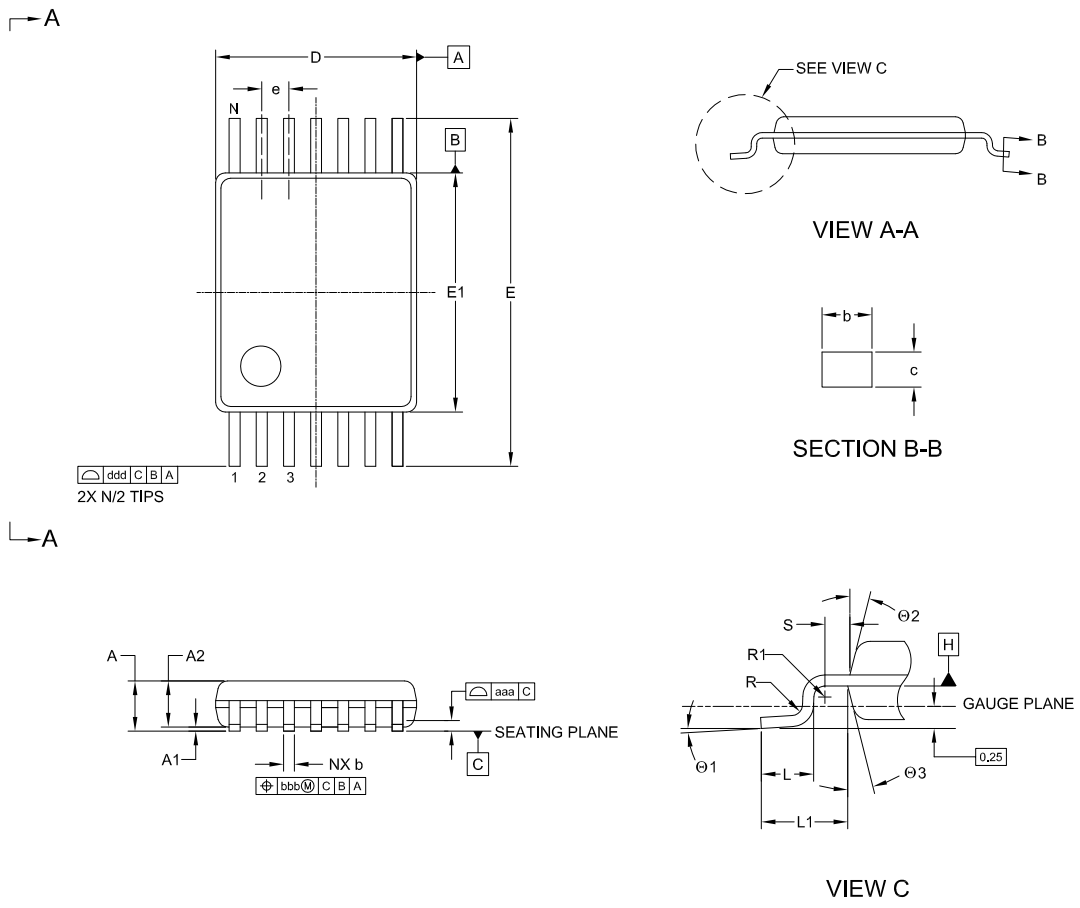
Figure 85:
Pixel Cell Placement



Note(s) and/or Footnote(s):

1. All dimensions in mm.
2. Die thickness 203µm nom.
3. Adhesive thickness 30 ± 15µm.
4. Leadframe downest 152 ± 25µm.
5. Leadframe thickness 125 ± 8µm.

Figure 86:
14-Lead Thin Shrink Small Outline Package TSSOP-14



Symbol	Min	Nom	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	5.00	5.10
E	-	6.40 BSC	-
E1	4.30	4.40	4.50
e	-	0.65 BSC	-
L	0.45	0.60	0.75
L1	-	1.00 REF	-

Symbol	Min	Nom	Max
R	0.09	-	-
R1	0.09	-	-
S	0.20	-	-
Θ1	0°	-	8°
Θ2	-	12REF	-
Θ3	-	12 REF	-
aaa	-	0.10	-
bbb	-	0.10	-
ccc	-	0.05	-
ddd	-	0.20	-
N		14	

Note(s) and/or Footnote(s):

1. Dimensions & toleranceing confirm to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. N is the total number of terminals.

Figure 87:
TSSOP-14 Marking

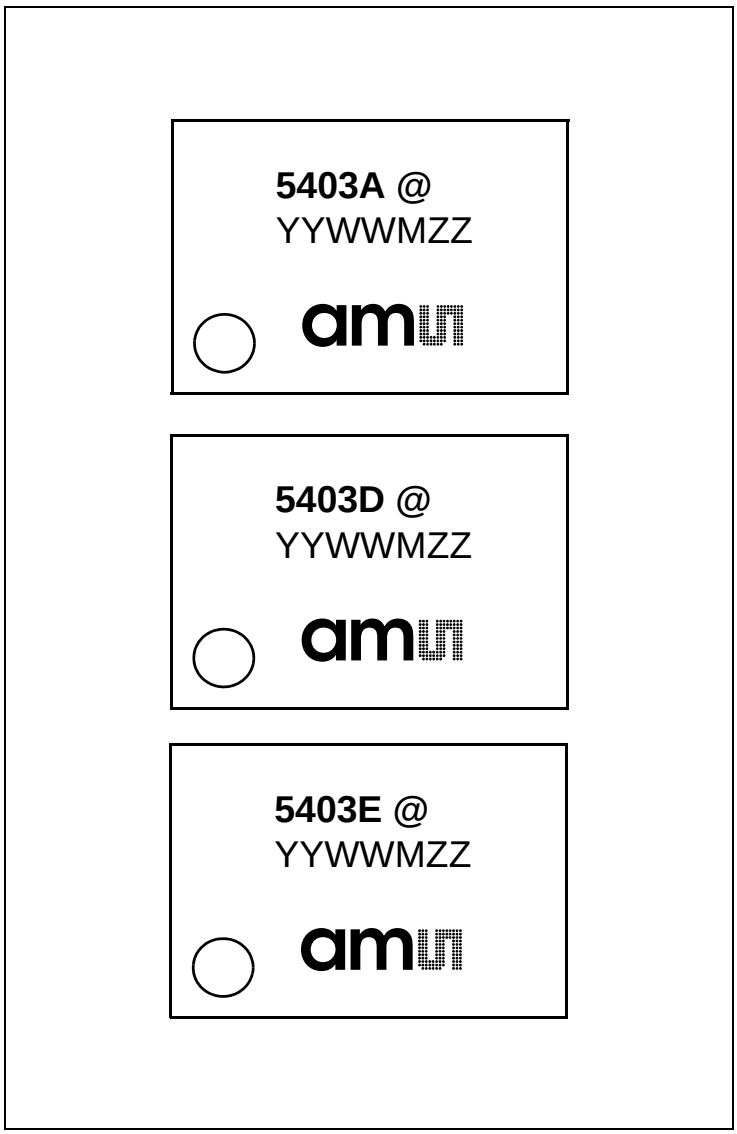


Figure 88:
Packaging Code: @YYWWMZZ

@	YY	WW	M	ZZ
Sublot identifier	Year	Manufacturing Week	Assembly plant identifier	Assembly traceability code

Ordering & Contact Information

The device is available as the standard products shown in Figure 89.

Figure 89:
Ordering Information

Ordering Code	Package	Description	Delivery Form	Delivery Quantity
AS5403**A**-HTST	TSSOP-14	Absolute Linear Position Sensor with ±50 mT magnetic input range Bx/Bz	13" Tape & Reel in dry pack	4500
AS5403**A**-HTSM			7" Tape & Reel in dry pack	500
AS5403**D**-HTST		Absolute Linear Position Sensor with ±100 mT magnetic input range Bx/Bz	13" Tape & Reel in dry pack	4500
AS5403**D**-HTSM			7" Tape & Reel in dry pack	500
AS5403**E**-HTST		Off-Axis Position Sensor with ±100 mT magnetic input range Bx/By ±100 mT magnetic input range Bx/Bz	13" Tape & Reel in dry pack	4500
AS5403**E**-HTSM			7" Tape & Reel in dry pack	500

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Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
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Revision Information

Changes from 1-04 (2015-Apr-07) to current revision 1-06 (2015-Aug-27)	Page
1-04 (2015-Apr-07) to 1-05(2015-Aug-04)	
Removed content related to AS5403B	
1-05 (2015-Aug-04) to 1-06(2015-Aug-27)	
Updated Figure 7	7
Updated Figure 14	15
Updated Sensor Placement section	56
Added Figure 85	57
Updated Figure 86	58

Note(s) and/or Footnote(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

Content Guide