Features

- **Full-Frame Image Sensor 4096 x 4096 Pixels**
- **11 µm x 11 µm Photo-MOS Pixel with 100% Aperture**
- **Image Zone: 45 x 45 mm**
- **Frame Readout Through One, Two or Four Outputs**
- **Data Rates Up to 4 x 40 MHz (Compatibility with 7, 4 Frames/Second)**
- **True 12-bit High Dynamic Range**
- **Very Low Readout Noise**
- **Very Low Dark Current (MPP Mode)**
- **Optimized Resolution and Responsivity in the 400 - 1100 nm Spectrum**
- **On-chip Thermometer for Each Quarter**
- **Additional Full-Frame Operating Modes:**
  - **4/3 Aspect Ratio: 4096 x 3072**
  - **2/1 Aspect Ratio: 4096 x 2048**
  - **Binning 2 x 2 Pixels (Format 2048 x 2048 Pixels of 22 x 22 µm)**
  - **Binning 4 x 4 Pixels (Format 1024x 1024 Pixels of 44 x 44 µm)**
- **On-request Frame Transfer Architecture:**
  - **2048 Active Lines, One Memory Zone with Frame Readout Through One or Two Outputs**
  - **2048 Active Lines, Two Memories Zones with Frame Readout Through Two or Four Outputs**

Applications

Flexibility and performance makes this device suitable for digital photography, graphic arts, medical or industrial applications and scientific analysis.

Description

Atmel's AT71201M is a full-frame sensor based on charge-coupled device (CCD) technology. It can be used in a wide range of applications thanks to operating mode flexibility, very high definition and high dynamic range.

The nominal photosensitive area is made up of 4096 x 4096 useful pixels and is split into four independent zones that are driven separately by four independent four-phase clock sets. Thus the sensor can be used in up to 12 main modes.

The large format and high definition make the device suitable for any application requiring precision.

The high sensitivity of the 11 x 11 µm pixels with 100% fill factor provides a large bandwidth of response with up to 1100 nm wavelength.

Two serial registers and four independent output amplifiers offer a high-frequency functionality at 40 MSPS and up to 7.4 frames per second with a high signal to noise ratio.

16 M-Pixels Sensor

AT71201M

Preliminary

Rev. 5328A–IMAGE–05/03

Pinout

Figure 1. AT71201M Pinout, Top View of the Sensor

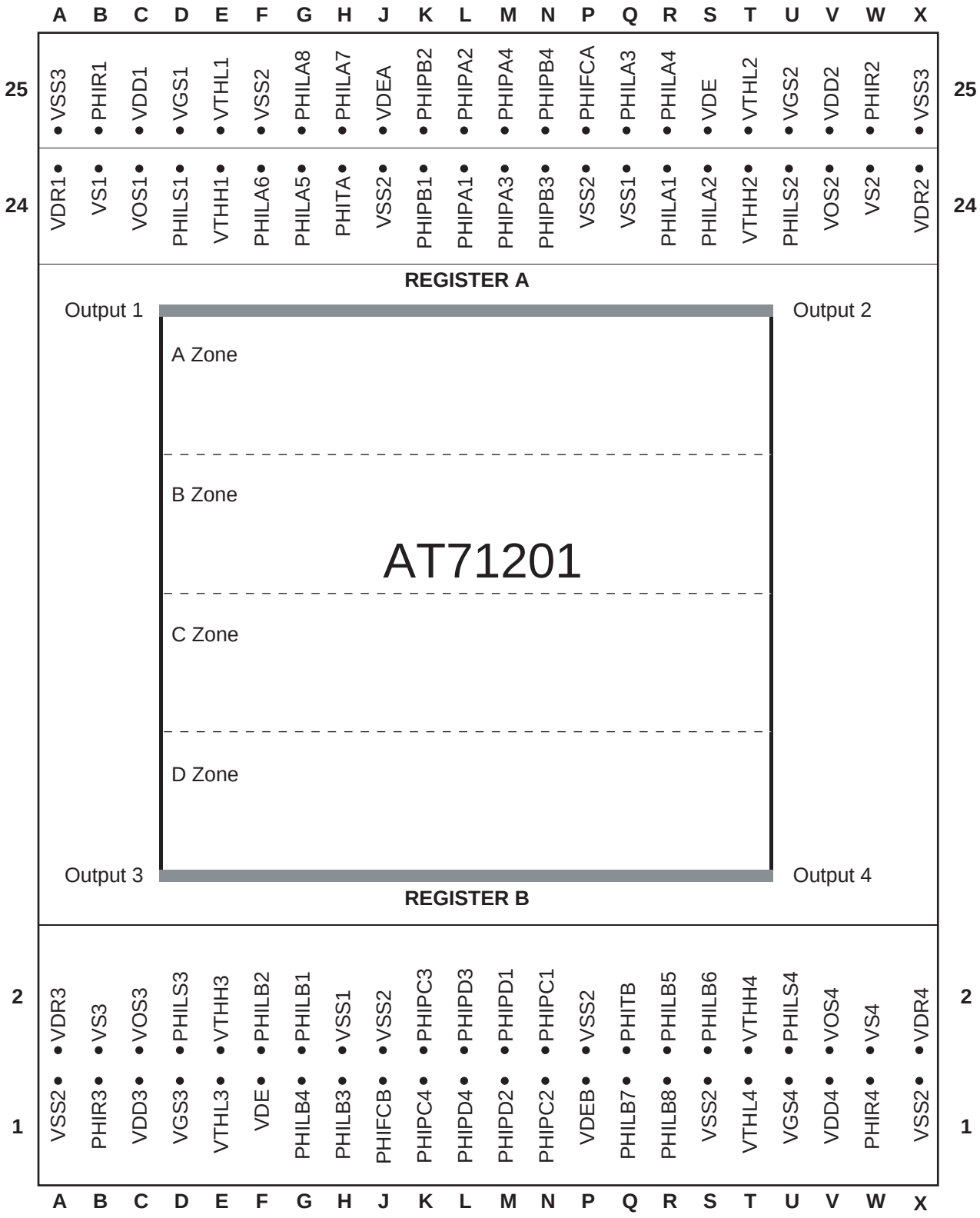

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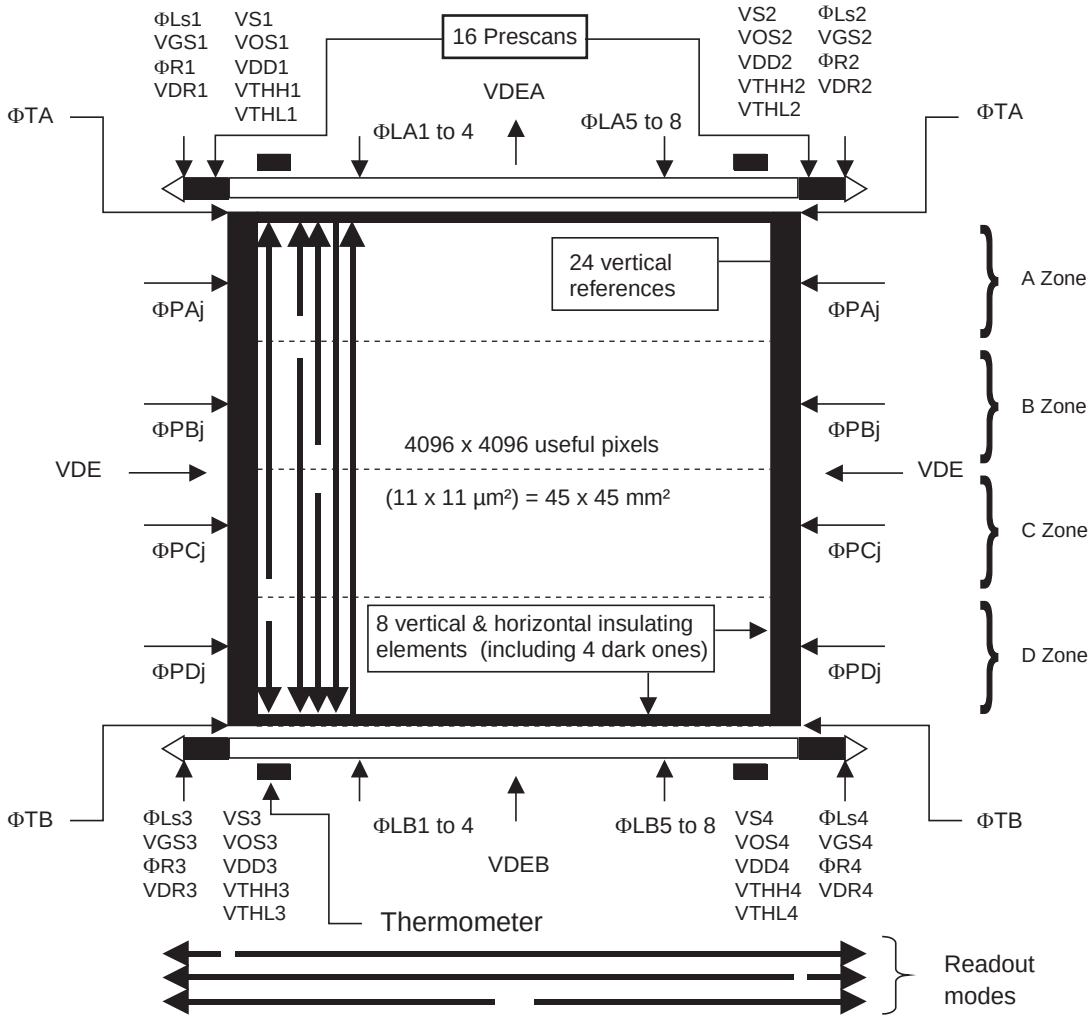
Table 1. AT71201M Pinout

Signal Name	Parameter
PHILA [1;8]	Registers A clocks
PHILB [1;8]	Registers B clocks
PHILS [1;4]	Summing clocks
PHIR [1;4]	Reset gates
PHIPA [1;4]	Image zone A clocks
PHIPB [1;4]	Image zone B clocks
PHIPC [1;4]	Image zone C clocks
PHIPD [1;4]	Image zone D clocks
PHITA	Image zone to register A transfer clock
VGS [1;4]	Register output gate biases
VOS [1;4]	Video outputs
VDD [1;4]	Amplifier drains
VS [1;4]	Amplifier sources
VDR [1;4]	Reset drains
VDE (2)	Peripheral vertical drain
VDEA	Peripheral drain along register A
VDEB	Peripheral drain along register B
VTHL [1;4]	Thermometer low 1 to 4
VTHH [1;4]	Thermometer high 1 to 4
VSS (12)	Ground connection

Block Diagram

Figure 2. AT71201M Block Diagram - Top View



Architectural Overview

General Parameters

Table 2. General Parameters

Parameter	Value
Pixel size	11 x 11 µm²
Number of useful pixels per line	4096
Number of useful lines	4096
Number of extra lines	8 per register
Number of readout registers	2
Number of prescan CCD stages (per output)	16
Number of dark references (cells per line)	24
Number of outputs (2 per register)	4(1)
MPP mode/low dark current mode	Yes (image zone)
Anti-blooming functionality	no
Binning (summation) mode	Yes(2)
Pixel clocking mode	4-phase
Readout Register clocking mode	2-phase
Specific functions	Thermometer

Notes: 1. The full-frame version can be read through one, two or four outputs
2. The lines summation into the register is made by a specific timing diagram. The integration time should be adapted to prevent charge overflow.

A specific clock allows column summation.

The pixel size is 11 x 11µm^2 with 100% fill factor (photo-MOS technology).

The sensor is compatible with a 180° rotation.

The image zone commands are split in 4 horizontal areas. The combination of the

ΦPij clocks allows various transfer configurations.

The serial registers are driven by 8 ΦLi clocks. An adapted combination of them allows transfers of 100% of stages to the right side or the left side or 50% in each direction.

Organization

Top to Bottom

The AT71201M is made up of four zones (A, B, C and D) that are separately driven.

Table 3. Vertical Characteristics

Zone	Configuration
A	8 dummy lines (4 photosensitive ones)
	2048 active lines, 100% photosensitive
B	2048 active lines, 100% photosensitive
C	2048 active lines, 100% photosensitive
D	2048 active lines, 100% photosensitive
	8 dummy lines (4 photosensitive ones)

Corner to Center

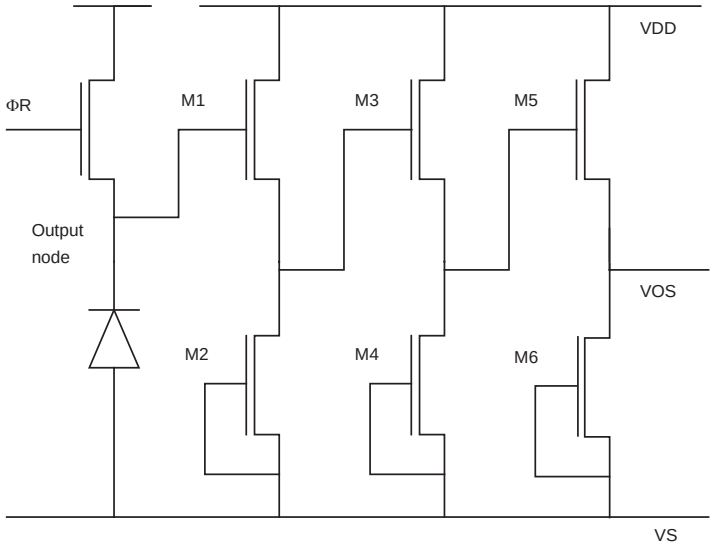
Table 4. Horizontal Characteristics for Different Modes

	Readout Mode	
Characteristic	**One Output**	**Two Outputs on Same Register**
Prescan stages	16	16
Dark references	24	24
Insulating elements	8	8
Useful pixels	4096	2048

Output Amplifiers

The charge packets are clocked towards the output nodes and are converted to voltages. The potential at the output node is read through a source follower amplifier.

Figure 3. On-Chip Output Amplifiers



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Absolute Maximum Ratings[1]

Table 5. Maximum Applied Voltages with Respect to VSS

Signal Name	Parameter	Min	Max
PHILA [1;8]	Registers A clocks	-0.3V	+15V
PHILB [1;8]	Registers B clocks	-0.3V	+15V
PHILS [1;4]	Summing clocks	-0.3V	+15V
PHIR [1;4]	Reset gates	-0.3V	+15V
PHIPA [1;4]	Image zone A clocks	-15V & PHIPA [others] -15V	+15V & PHIPA [others] +15V
PHIPB [1;4]	Image zone B clocks	-15V & PHIPB [others] -15V	+15V & PHIPB [others] +15V
PHIPC [1;4]	Image zone C clocks	-15V & PHIPC [others] -15V	+15V & PHIPC [others] +15V
PHIPD [1;4]	Image zone D clocks	-15V & PHIPD [others] -15V	+15V & PHIPD [others] +15V
PHITA	Image zone to register A transfer clock	-15V & PHIPA [4] -15V	+15V & PHIPA [4] +15V
PHITB	Image zone to register B transfer clock	-15V & PHIPB [4] -15V	+15V & PHIPB [4] +15V
VGS [1;4]	Ouput gates	-0.3V	+15V
VOS [1;4]	Video outputs	-0.3V	+15V
VDD [1;4]	Amplifier drains	-0.3V	+15V
VS [1;4]	Amplifier sources	-0.3V	+15V
VDR [1;4]	Reset drains	-0.3V	+15V
VDE	Peripheral drain	-0.3V	+15V
VDEA	Peripheral drain along register A	-0.3V	+15V
VDEB	Peripheral drain along register B	-0.3V	+15V
VTHL [1;4]	Thermometer low 1 to 4	-0.3V	+15V
VTHH [1;4]	Thermometer high 1 to 4	-0.3V	+15V
VSS	Ground		

Note: 1. Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Shorting VOS to any other pin, even temporally, can permanently damage the output amplifier.

Device exposure to ESD stress could result in current leakage or performance degradation; reliability can also be affected.

To avoid degradation, sensors (including pins and package) have to be handled carefully using a grounded bracelet. When unplugged, they have to be stored in the original case (or box).

In any case, pins of the devices must not be discharged straight to ground..

Storage Temperature Range	-40°C to +70°C
Operating Temperature Range	0°C to +70°C
Thermal Cycling	3°C/mn

DC Characteristics

Table 6. DC Characteristics

Parameters	Symbol	Typical Value	Adjusting Range	Current
Source bias	Vsi	0V	[0;1] Volts	4 x -25 mA
Amplifier drain supply	VDDi(1)	15V	[14.5;15.5] Volts	4 x 25 mA
Substrate bias	Vss	0V		
Reset diode	VDRi(2)	14V	[13.5;14.5] Volts	< 5 µA
Output gate	VGSi	3.5V	[3;4] Volts	< 5 µA
Vertical drain	VDE	8V	[6;9] Volts (15 V max respect to ΦTi)	< 50 µA
Horizontal drain	VDEi	12V	[6;15] Volts	< 50 µA

Notes: 1. If the associated output i is not used, VDDi should be stated to 0 Volts in order to reduce global power consumption
2. VDRi voltage should always be kept lower than VDDi voltage, especially during power on

Recommendation: All DC voltages should be bypassed by adding capacitors as closed as possible to the pin connection.

Drive Clock Characteristics

Table 7. Drive Clock Characteristics

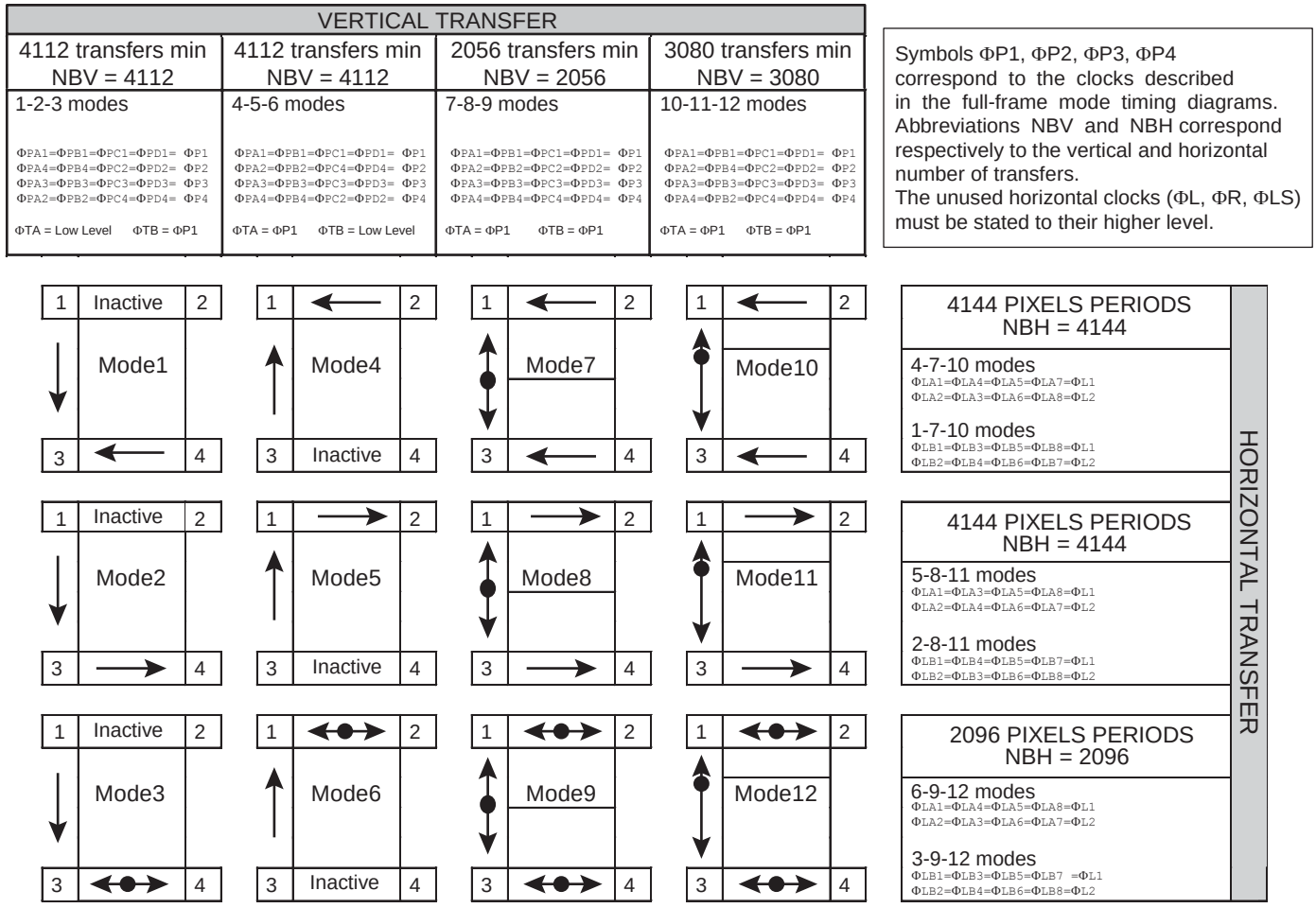
Parameter	Symbol	State	Minimum	Typical	Maximum	Typical Capacitance
Image clocks	PHIPij(1)	Low	-9V	-8V	-7.5V	37 nF
		High	+2.5V	+3V	+3.5V	
Transfer clocks	PHITk(2)	Low	-6V	-5V	-4V	200 pF
		High	+2.5V	+3V	+3.5V	
Register clocks	PHILkm(2)	Low	0V	0V	0.5V	180 pF
		High	+7V	+7.5V	+8V	
Summing clocks	PHILSj(1)	Low	0V	0V	0.5V	15 pF
		High	+7V	+7.5V	+8V	
Reset gate clocks	PHIRj(1)	Low	0V	+2V	+3V	15 pF
		High	+11V	+12V	+13V	

Notes: 1. i = A to D, j = 1 to 4
2. k = A to B, m = 1 to 8

Operating Modes

For the required readout mode, the vertical and horizontal clocks must be tied together, as following:

Figure 4. Operating Modes



Timing Diagrams

Figure 5. Full-Frame Mode Timing Diagram

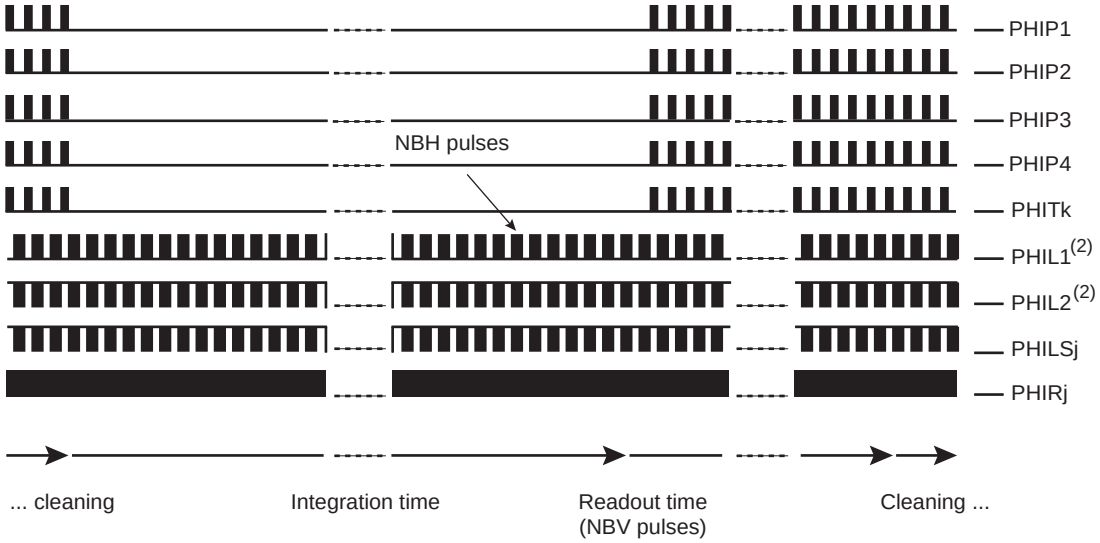
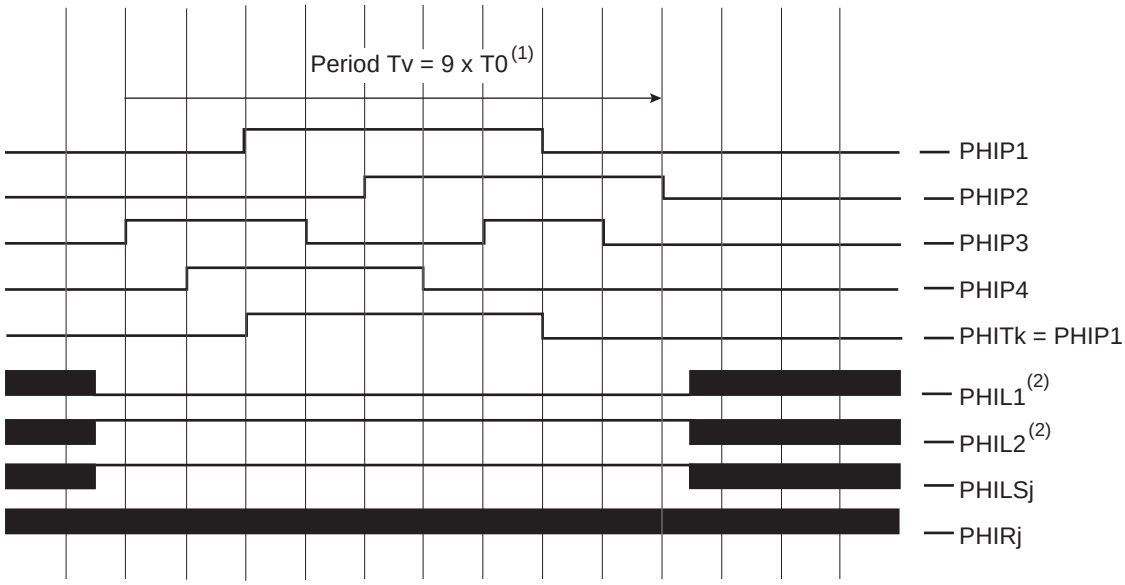


Figure 6. Line Timing Diagram



Notes: 1. T0 = Master clock period (vertical transfer)
2. See Figure 4

Figure 7. Summation Timing Diagram of 2 Lines

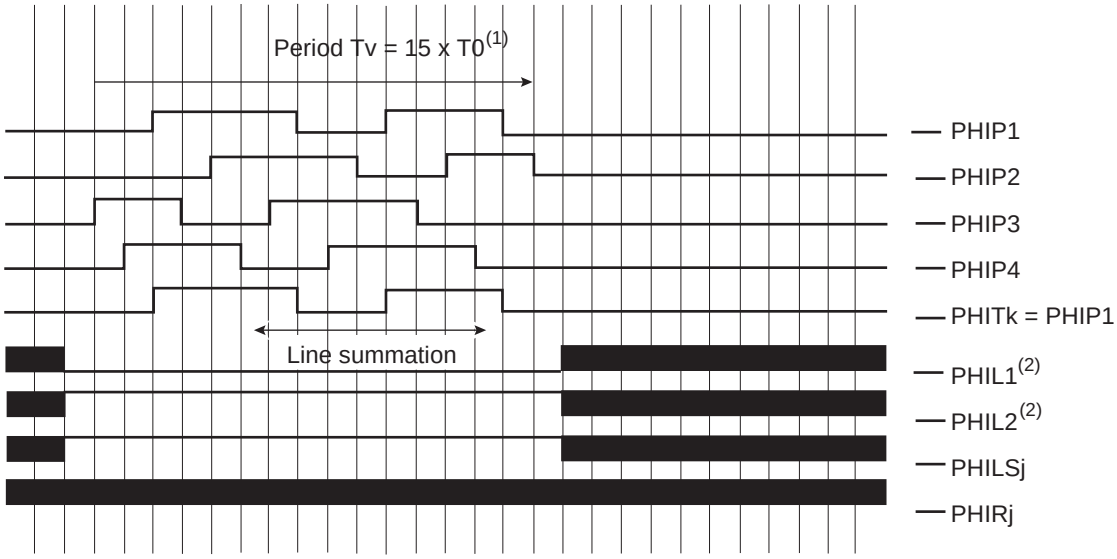
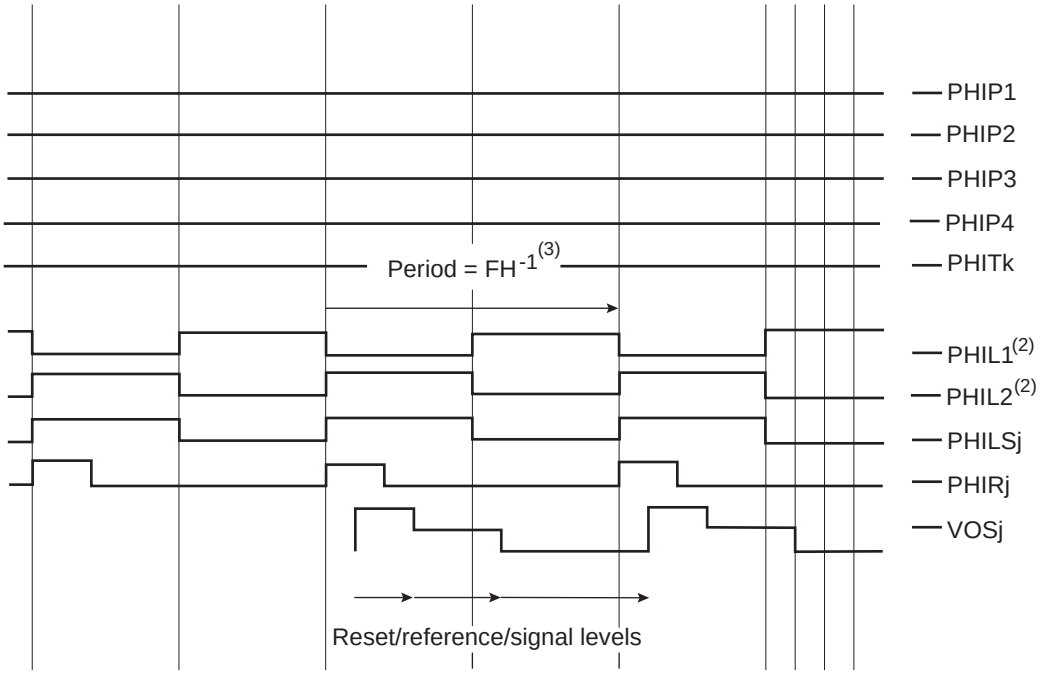
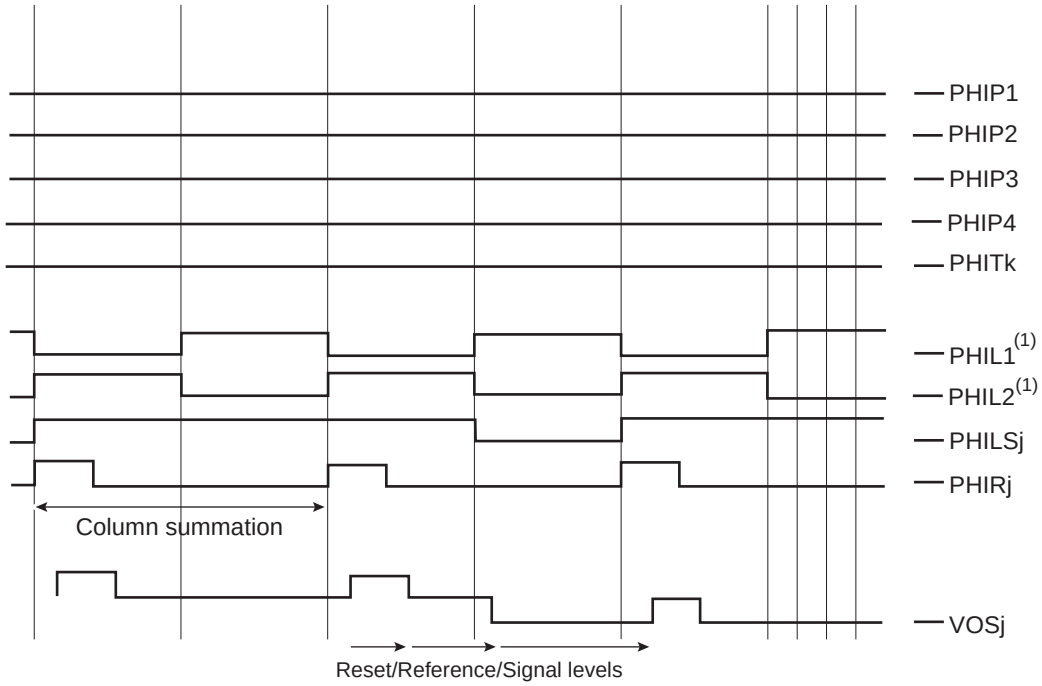


Figure 8. Readout Signal



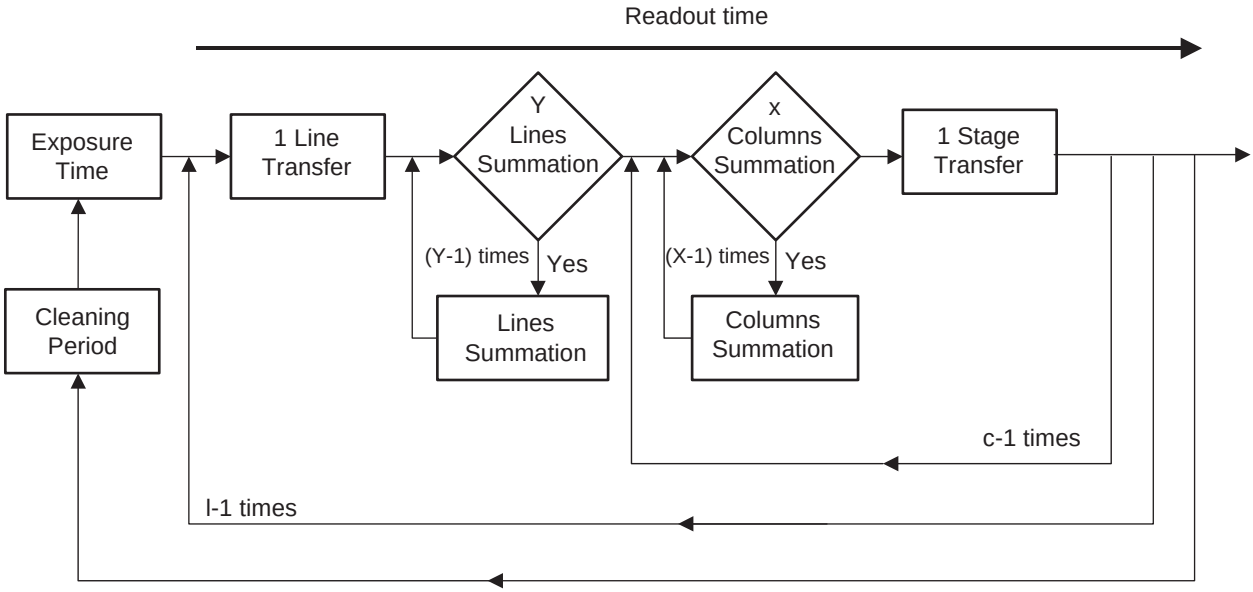
Notes: 1. T0 = Master clock period (vertical transfer)
2. See Figure 4
3. FH = Readout Register Frequency

Figure 9. Summation Timing Diagram



Note: 1. See Figure 4

Figure 10. Frame Transfer Sequence



The readout sequence corresponding to an image made of C x l pixels

- XC = 2048 in modes 3, 6, 9, 12
- XC = 4096 in other modes
- Yl = 2048 in modes 1 to 6
- Yl = 4096 in modes 7 to 9

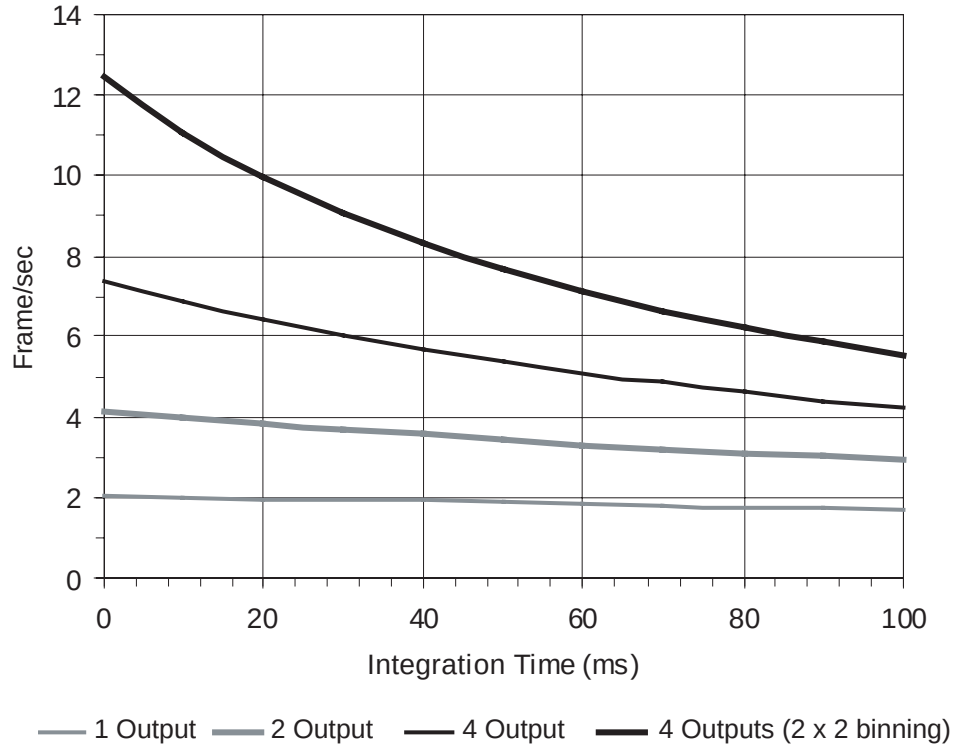
Table 8. Time Constants of Different Phases

Time	Symbol	Minimum	Typical	Maximum
Buffer time = Waiting time between ΦPij and ΦLkm acting	Tb	100 ns	-	-
Rise Time and Fall Time of ΦPij, ΦTk	Ts	250 ns	0.5 x T0	0.5 x T0
Rise Time and Fall Time of ΦLkm, ΦLSj	Tq	3 ns	6 ns	-
Rise Time and Fall Time of ΦRj	Tr	1.5 ns	3 ns	-

T0 = master clock period (vertical transfer)

Frame Rate Characteristics

Figure 11. Frame Rate Characteristics



Frame rate is given for maximum readout frequency(1).

Note: 1. Horizontal pixel frequency, FH = 40 MHz
Vertical transfer time, To = 1.5 µs
Buffer time, Tb = 100 ns

Output Buffer

Table 9. Output Buffer[2]

Parameter	Symbol	Minimum	Typical	Maximum	Unit
DC output	Vref	8.0	8.6	9.2	V
Output impedance	Zout	–	88	–	Ω
Output amplifier supply current[1]	IDD	19	25	31	mA
Amplifier bandwidth (-3 dB)	BW	–	200	–	MHz
Charge to Voltage Conversion factor	CVF	–	6.0	–	µV/ electron
Temperature conversion	VTH	–	7.5	–	mV/°C
Vertical transfer time	T0	1.5	2	–	µs
Readout register frequency	FH	–	–	40	MHz

Note: 1. Per output
2. All characteristics given for temperature = 25°C

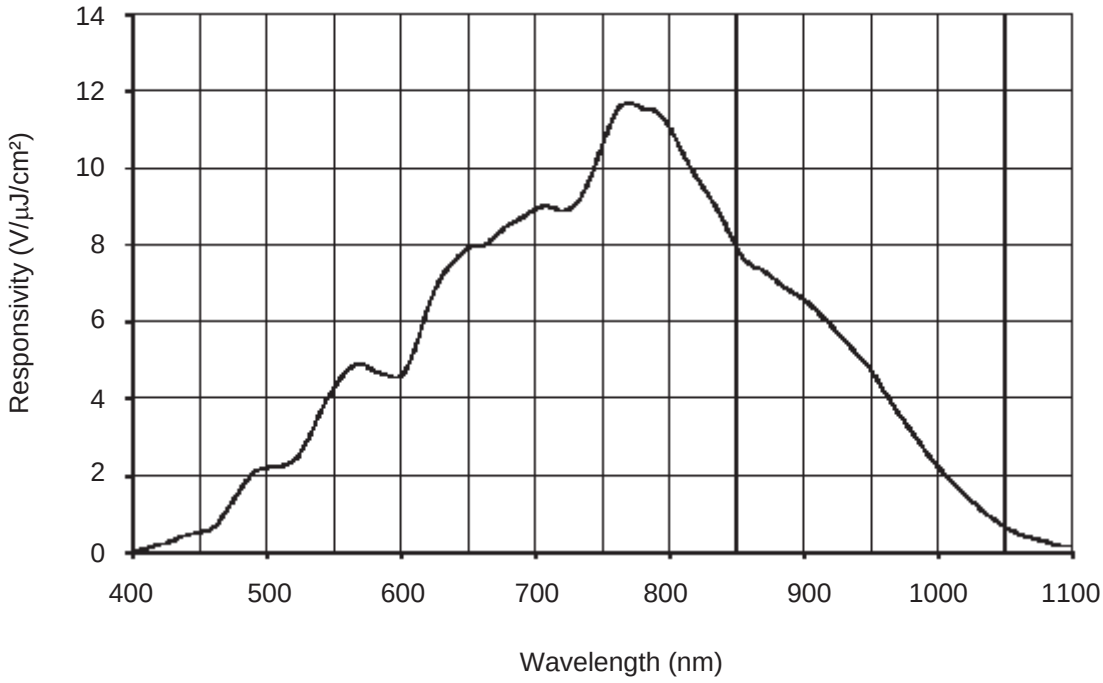
Electro-Optical Performances

Table 10. Electro-Optical Performances[3]

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Pixel saturation voltage	VSAT	600	750	900	mV
Readout saturation charge in binning mode	RSAT	–	1800	–	mV
Dynamic range	DR	72	74	76	dB
Readout noise	RN	–	25	–	electron
Responsivity	R	3.8	4.2	–	V/(µJ/cm²)
Resolution (MTF) at 45 cycles/mm – H axis Resolution (MTF) at 45 cycles/mm – V axis	MTFX[1] MTFY[1]	– –	45 50	– –	% %
Pixel response non-uniformity	PRNU[1][2]	–	0.5	3	%
Image zone dark signal, MPP Image zone dark signal, non-MPP Register dark signal, non-MPP	DS1 DS2 DSR	0.05 10 30	0.2 20 60	2 40 100	mV/s mV/s mV/s
Image zone dark signal non-uniformity, MPP integration	DSNU[2]	–	0.5	1.5	mV/s
Horizontal charge transfer efficiency per CCD stage	HCTE	0.99993	0.99998	–	–
Vertical charge transfer efficiency per CCD stage	VCTE	0.99995	0.99998	–	–

Notes: 1. Combined with 2 mm "BG38" IR filter type
2. Standard deviation
3. All values given at 25°C, typical voltages

Figure 12. Spectral Responsivity



Temperature Measurement

A current of 100 µA is forced between VTHLi and VTHHi, in the range of 0 to 70°C, the corresponding measured voltage, is proportional to temperature:

$$Temperature(°C) = \frac{VTHHi(mV) - VTHLi(mV)}{7.5(mV/°C)} - 613(°C)$$

Relative thermometer accuracy is 0.13°C/mV ±10%

Absolute thermometer precision is ±10°C.

Figure 13. On Chip Thermometer

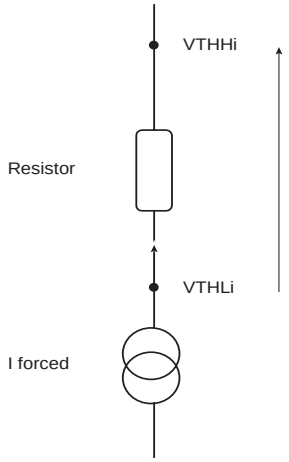


Image grade

Table 11. Image Grade[2]

Grade	Blemishes		Cluster 1		Cluster 2		Column	
	Total	**D-min**[1]	**Total**	**D-min**[1]	**Total**	**D-min**[1]	**Total**	**D-min**[1]
E	≤ 1500	3	≤ 100	50	≤ 20	100	≤ 10	150

Notes: 1. D-min: distance of pixels defects in any direction. All occurrences are non-contiguous.
2. Testing has been carried out under the following conditions:
Operating temperature = 25 °C
Illumination conditions: 3200K Halogen lamp with BG38 Infrared filter and f/3.5 aperture
Integration time in darkness = 10 seconds, test under illumination at 50% of VSAT
Standard mode, To = 1.5 µs, FH = 40 MHz

Definitions

Table 12. Defect Sizes

Type	Description
Blemish	1 x 1 pixel defect
Cluster	Blemish groupings of less than a given number of adjacent defects: 1 x 1 pixel < cluster 1 size ≤ 2 x 2 pixels 2 x 2 pixels < cluster 2 size ≤ 5 x 5 pixels
Column	One-pixel-wide column with more than seven contiguous defective pixels

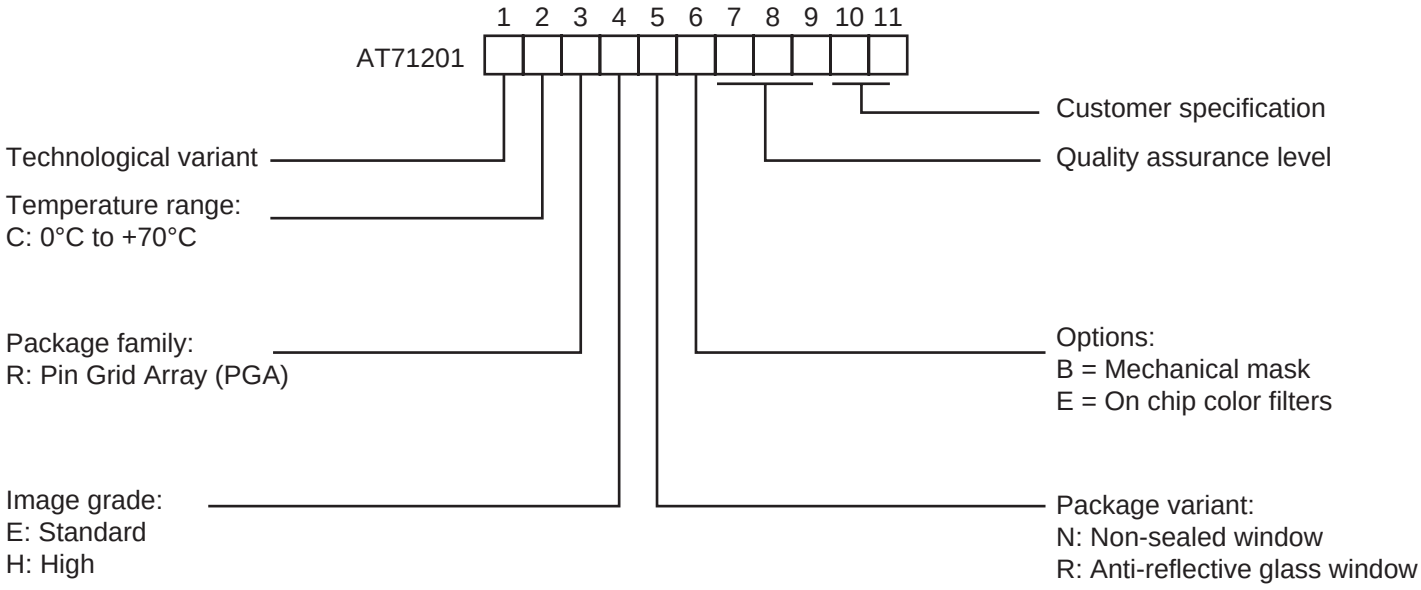
Table 13. Defects in Darkness

Type	Description
Blemish/Clusters	Pixel signal deviation of more than 200 mV from the average output signal
Column	Column signal deviation of more than 50 mV from the average output signal

Table 14. Defects Under Illumination

Type	Description
Blemish/Clusters	Pixel signal deviation of more than ± 30% from the average output signal
Column	Column signal deviation of more than ± 20% from the average output signal

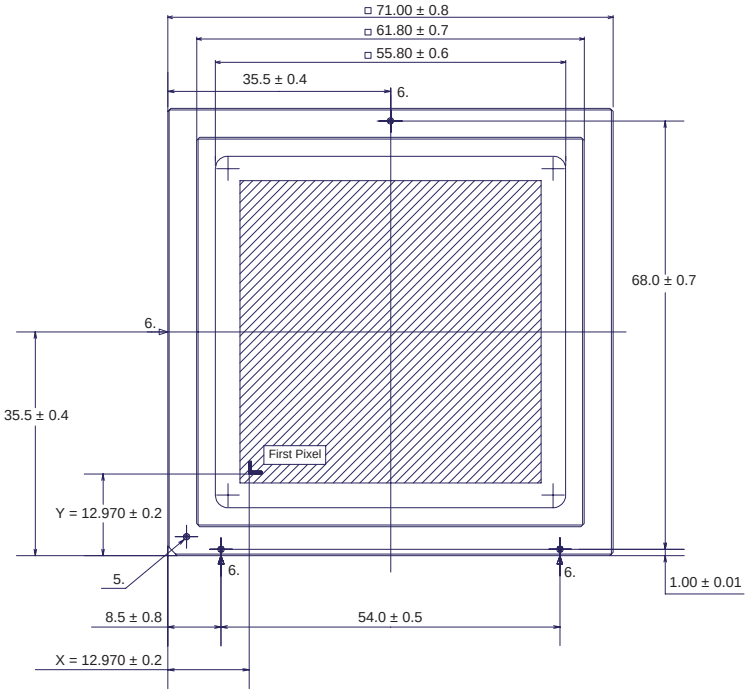
Ordering Information

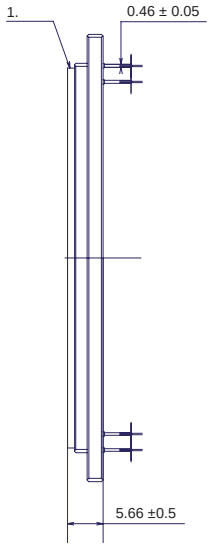


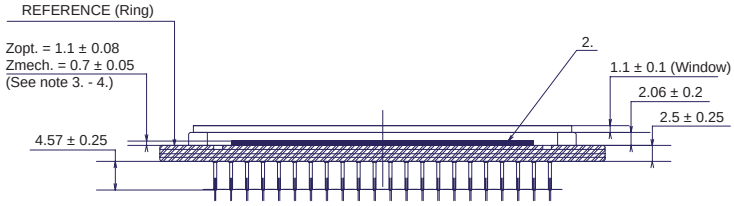
The following part numbers are available:

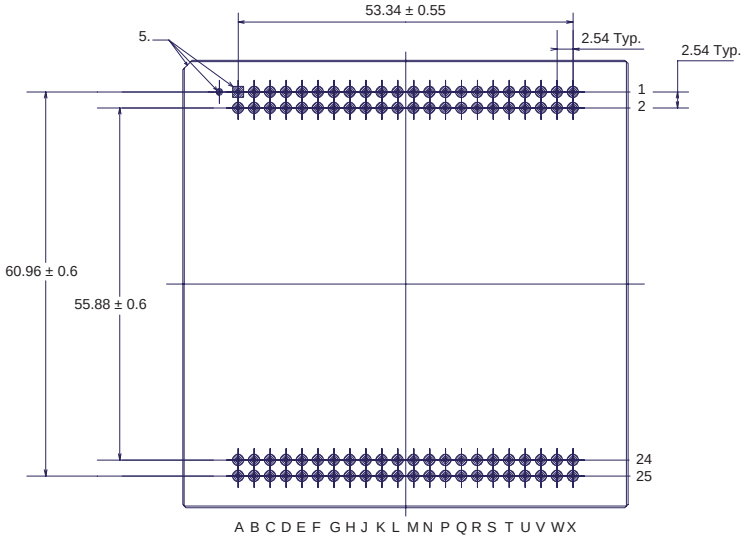
- AT71201MCRER
- AT71201MCREN

Package Drawing









Notes:
1. Anti-reflective window 400 - 700 nm
2. Photosensitive area
3. Zopt = Optical distance between REFERENCE surface and 2
4. Zmech = Mechanical distance between REFERENCE surface and 2
5. Pin A1 index mark
6. Mechanical references/die positionning (first pixel)

REFERENCE: Z
REFERENCE: XY
All Dimensions In Millimeter

Die Flatness ≤ 50 µm
Die Axis Angle ≤ 0.2°

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