



Atmel 8-bit Microcontroller with 16K Bytes In-System Programmable Flash

AT90PWM216 /AT90PWM316 Summary

Features

- High Performance, Low Power AVR[®] 8-bit Microcontroller
- Advanced RISC Architecture
 - 129 Powerful Instructions - Most Single Clock Cycle Execution
 - 32 x 8 General Purpose Working Registers
 - Fully Static Operation
 - Up to 1 MIPS throughput per MHz
 - On-chip 2-cycle Multiplier
- Data and Non-Volatile Program Memory
 - 16K Bytes Flash of In-System Programmable Program Memory
 - Endurance: 10,000 Write/Erase Cycles
 - Optional Boot Code Section with Independent Lock Bits
- In-System Programming by On-chip Boot Program
- True Read-While-Write Operation
 - 512 Bytes of In-System Programmable EEPROM
- Endurance: 100,000 Write/Erase Cycles
 - 1024 Bytes Internal SRAM
 - Programming Lock for Flash Program and EEPROM Data Security
- On Chip Debug Interface (debugWIRE)
- Peripheral Features
 - Two or three 12-bit High Speed PSC (Power Stage Controllers) with 4-bit Resolution Enhancement
 - Non Overlapping Inverted PWM Output Pins With Flexible Dead-Time
 - Variable PWM duty Cycle and Frequency
 - Synchronous Update of all PWM Registers
 - Auto Stop Function for Event Driven PFC Implementation
 - Less than 25Hz Step Width at 150kHz Output Frequency
 - PSC2 with four Output Pins and Output Matrix
 - One 8-bit General purpose Timer/Counter with Separate Prescaler and Capture Mode
 - One 16-bit General purpose Timer/Counter with Separate Prescaler, Compare Mode and Capture Mode
 - Programmable Serial USART
 - Standard UART mode
 - 16/17 bit Biphase Mode for DALI Communications
 - Master/Slave SPI Serial Interface
 - 10-bit ADC
 - Up To 11 Single Ended Channels and 2 Fully Differential ADC Channel Pairs
 - Programmable Gain (5x, 10x, 20x, 40x on Differential Channels)
 - Internal Reference Voltage
 - 10-bit DAC
 - Two or three Analog Comparator with Resistor-Array to Adjust Comparison Voltage
 - 4 External Interrupts
 - Programmable Watchdog Timer with Separate On-Chip Oscillator
- Special Microcontroller Features
 - Low Power Idle, Noise Reduction, and Power Down Modes
 - Power On Reset and Programmable Brown Out Detection
 - Flag Array in Bit-programmable I/O Space (4 bytes)
 - In-System Programmable via SPI Port
 - Internal Calibrated RC Oscillator (8 MHz)
 - On-chip PLL for fast PWM (32 MHz, 64 MHz) and CPU (16 MHz)
- Operating Voltage: 2.7V - 5.5V
- Extended Operating Temperature:
 - -40°C to +105°C

Atmel®

| Product | Package | 12 bit PWM with deadtime | ADC Input | ADC Diff | Analog Comparator | Application |
|------------|----------------|--------------------------|-----------|----------|-------------------|--|
| AT90PWM216 | SO24 | 2 x 2 | 8 | 1 | 2 | One fluorescent ballast |
| AT90PWM316 | SO32, QFN32 | 3 x 2 | 11 | 2 | 3 | HID ballast, fluorescent ballast, Motor control |

1. Disclaimer

Typical values contained in this datasheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device is characterized.

2. Pin Configurations

Figure 2-1. SOIC 24-pin Package

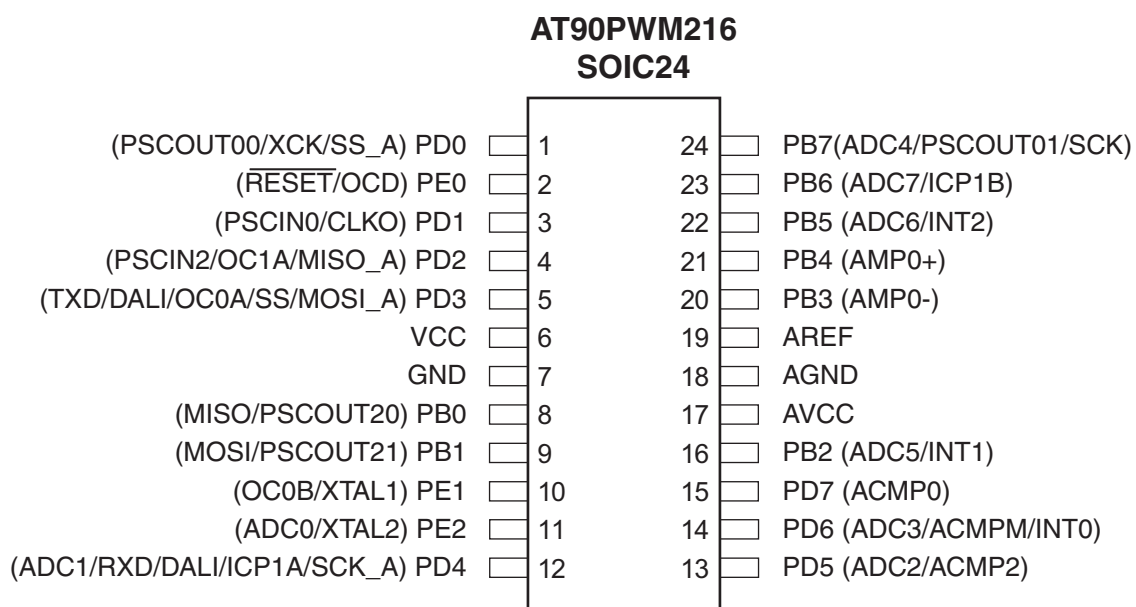


Figure 2-2. SOIC 32-pin Package

AT90PWM316
SOIC 32

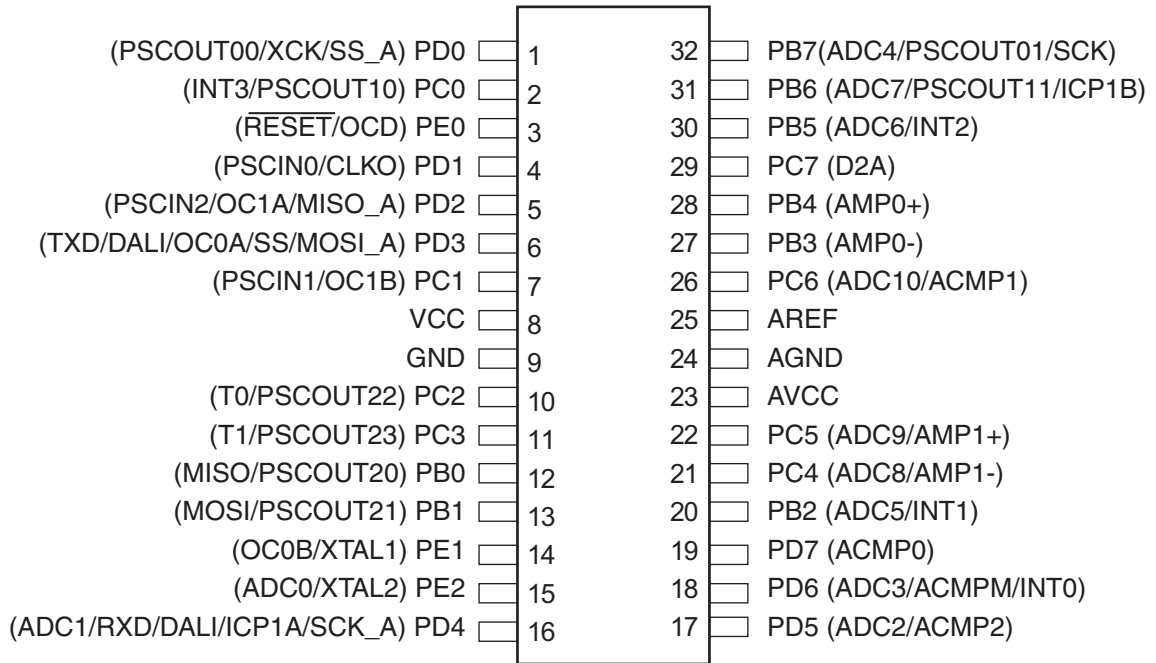
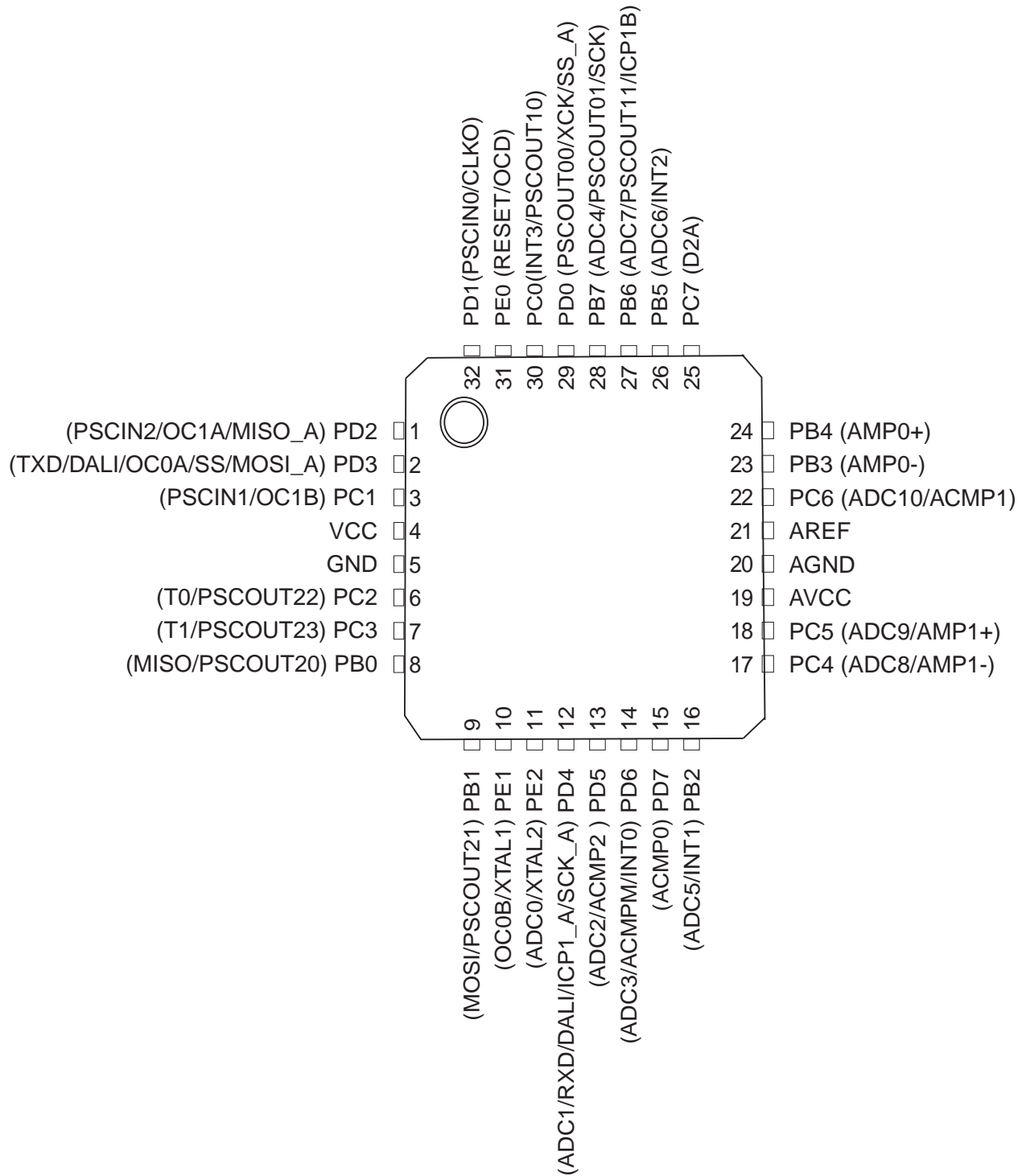


Figure 2-3. QFN32 (7*7 mm) Package.



Note: The Center GND PADDLE has to be connected to GND.

2.1 Pin Descriptions

Table 2-1. Pin out description

| S024 Pin Number | SO32 Pin Number | QFN32 Pin Number | Mnemonic | Type | Name, Function & Alternate Function |
|-----------------|-----------------|------------------|----------|---------------------------------|--|
| 7 | 9 | 5 | GND | Power | Ground: 0V reference |
| 18 | 24 | 20 | AGND | Power | Analog Ground: 0V reference for analog part |
| 6 | 8 | 4 | VCC | power | Power Supply: |
| 17 | 23 | 19 | AVCC | Power | Analog Power Supply: This is the power supply voltage for analog part For a normal use this pin must be connected. |
| 19 | 25 | 21 | AREF | Power | Analog Reference: reference for analog converter. This is the reference voltage of the A/D converter. As output, can be used by external analog |
| 8 | 12 | 8 | PBO | I/O | MISO (SPI Master In Slave Out) PSCOUT20 output |
| 9 | 13 | 9 | PB1 | I/O | MOSI (SPI Master Out Slave In) PSCOUT21 output |
| 16 | 20 | 16 | PB2 | I/O | ADC5 (Analog Input Channel5) INT1 |
| 20 | 27 | 23 | PB3 | I/O | AMP0- (Analog Differential Amplifier 0 Input Channel) |
| 21 | 28 | 24 | PB4 | I/O | AMP0+ (Analog Differential Amplifier 0 Input Channel) |
| 22 | 30 | 26 | PB5 | I/O | ADC6 (Analog Input Channel 6) INT 2 |
| 23 | 31 | 27 | PB6 | I/O | ADC7 (Analog Input Channel 7) ICP1B (Timer 1 input capture alternate input) PSCOUT11 output (see note 1) |
| 24 | 32 | 28 | PB7 | I/O | PSCOUT01 output ADC4 (Analog Input Channel 4) SCK (SPI Clock) |
| NA | 2 | 30 | PC0 | I/O | PSCOUT10 output (see note 1) INT3 |
| | 7 | 3 | PC1 | I/O | PSCIN1 (PSC 1 Digital Input) OC1B (Timer 1 Output Compare B) |
| | 10 | 6 | PC2 | I/O | T0 (Timer 0 clock input) PSCOUT22 output |
| | 11 | 7 | PC3 | I/O | T1 (Timer 1 clock input) PSCOUT23 output |
| | 21 | 17 | PC4 | I/O | ADC8 (Analog Input Channel 8) AMP1- (Analog Differential Amplifier 1 Input Channel) |
| | 22 | 18 | PC5 | I/O | ADC9 (Analog Input Channel 9) AMP1+ (Analog Differential Amplifier 1 Input Channel) |
| | 26 | 22 | PC6 | I/O | ADC10 (Analog Input Channel 10) ACMP1 (Analog Comparator 1 Positive Input) |
| 29 | 25 | PC7 | I/O | D2A : DAC output ⁽²⁾ | |

Table 2-1. Pin out description (Continued)

| S024 Pin Number | SO32 Pin Number | QFN32 Pin Number | Mnemonic | Type | Name, Function & Alternate Function |
|-----------------|-----------------|------------------|----------|----------|---|
| 1 | 1 | 29 | PD0 | I/O | PSCOUT00 output ⁽¹⁾ XCK (UART Transfer Clock) SS_A (Alternate SPI Slave Select) |
| 3 | 4 | 32 | PD1 | I/O | PSCIN0 (PSC 0 Digital Input) CLKO (System Clock Output) |
| 4 | 5 | 1 | PD2 | I/O | PSCIN2 (PSC 2 Digital Input) OC1A (Timer 1 Output Compare A) MISO_A (Programming & alternate SPI Master In Slave Out) |
| 5 | 6 | 2 | PD3 | I/O | TXD (Dali/UART Tx data) OC0A (Timer 0 Output Compare A) SS (SPI Slave Select) MOSI_A (Programming & alternate Master Out SPI Slave In) |
| 12 | 16 | 12 | PD4 | I/O | ADC1 (Analog Input Channel 1) RXD (Dali/UART Rx data) ICP1A (Timer 1 input capture) SCK_A (Programming & alternate SPI Clock) |
| 13 | 17 | 13 | PD5 | I/O | ADC2 (Analog Input Channel 2) ACMP2 (Analog Comparator 2 Positive Input) |
| 14 | 18 | 14 | PD6 | I/O | ADC3 (Analog Input Channel 3) ACMPM reference for analog comparators INT0 |
| 15 | 19 | 15 | PD7 | I/O | ACMP0 (Analog Comparator 0 Positive Input) |
| 2 | 3 | 31 | PE0 | I/O or I | RESET (Reset Input) OCD (On Chip Debug I/O) |
| 10 | 14 | 10 | PE1 | I/O | XTAL1: XTAL Input OC0B (Timer 0 Output Compare B) |
| 11 | 15 | 11 | PE2 | I/O | XTAL2: XTAL OuTput ADC0 (Analog Input Channel 0) |

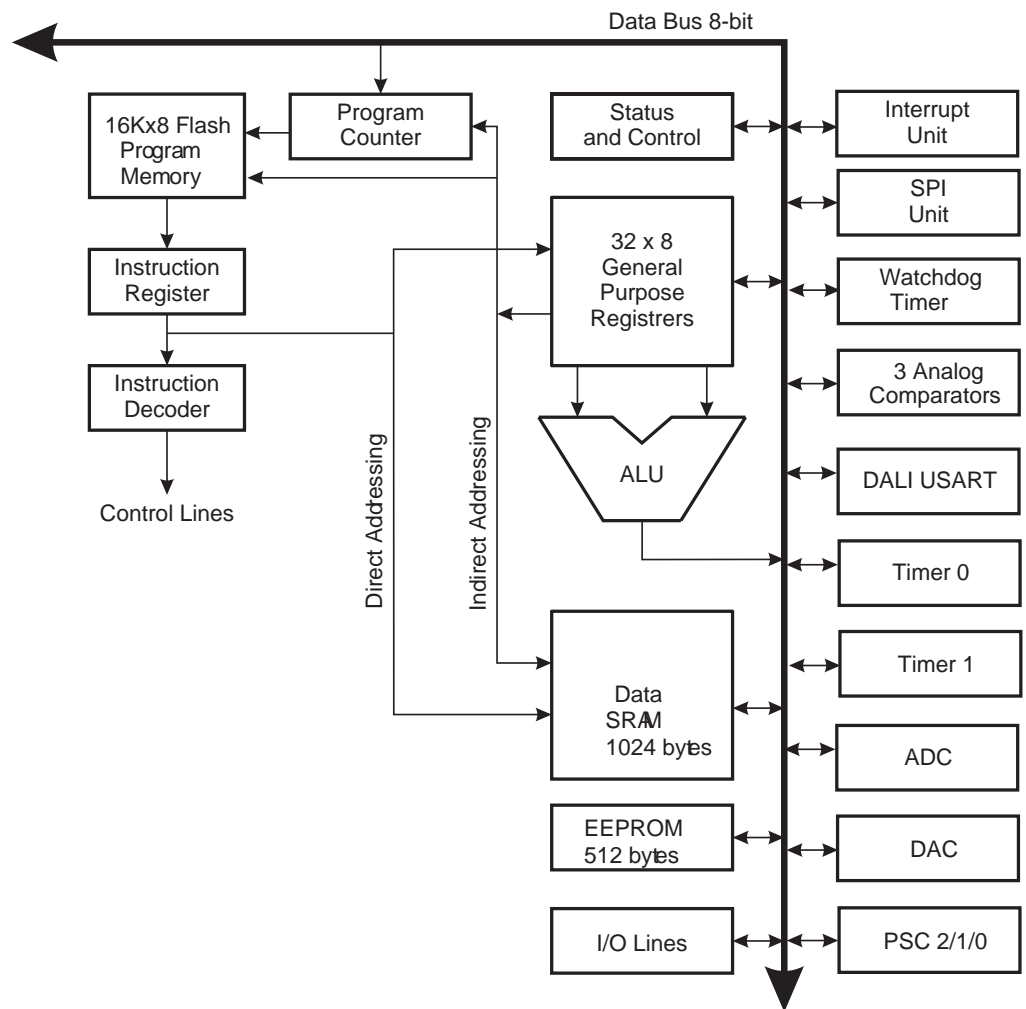
- Notes: 1. PSCOUT10 & PSCOUT11 are not present on 24 pins package
2. D2A (DAC Output) not available on AT90PWM261 (SOIC 24-pins)

3. Overview

The AT90PWM216/316 are low-power CMOS 8-bit microcontrollers based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the AT90PWM216/316 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

3.1 Block Diagram

Figure 3-1. Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The AT90PWM216/316 provides the following features: 16K bytes of In-System Programmable Flash with Read-While-Write capabilities, 512 bytes EEPROM, 1024 bytes SRAM, 53 general purpose I/O lines, 32 general purpose working registers, three Power Stage Controllers, two flexible Timer/Counters with compare modes and PWM, one USART with DALI mode, an 11-channel 10-bit ADC with two differential input stage with programmable gain, a 10-bit DAC, a programmable Watchdog Timer with Internal Oscillator, an SPI serial port, an On-chip Debug system and four software selectable power saving modes.

The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI ports and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or Hardware Reset. The ADC Noise Reduction mode stops the CPU and all I/O modules except ADC, to minimize switching noise during ADC conversions. In Standby mode, the Crystal/Res-

onator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low power consumption.

The device is manufactured using the Atmel high-density nonvolatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed in-system through an SPI serial interface, by a conventional non-volatile memory programmer, or by an On-chip Boot program running on the AVR core. The boot program can use any interface to download the application program in the application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel AT90PWM216/316 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The AT90PWM216/316 AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

Note: AT90PWM216 device is available in SOIC 24-pin Package and does not have the D2A (DAC Output) brought out to I/O pins.

3.2 Pin Descriptions

3.2.1 VCC

Digital supply voltage.

3.2.2 GND

Ground.

3.2.3 Port B (PB7..PB0)

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the AT90PWM216/316 as listed on [page 63](#).

3.2.4 Port C (PC7..PC0)

Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port C is not available on 24 pins package.

Port C also serves the functions of special features of the AT90PWM316 as listed on [page 65](#).

3.2.5 Port D (PD7..PD0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the AT90PWM216/316 as listed on [page 68](#).

3.2.6 **Port E (PE2..0) RESET/ XTAL1/ XTAL2**

Port E is an 3-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port E output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port E pins that are externally pulled low will source current if the pull-up resistors are activated. The Port E pins are tri-stated when a reset condition becomes active, even if the clock is not running.

If the RSTDISBL Fuse is programmed, PE0 is used as an I/O pin. Note that the electrical characteristics of PE0 differ from those of the other pins of Port C.

If the RSTDISBL Fuse is unprogrammed, PE0 is used as a Reset input. A low level on this pin for longer than the minimum pulse length will generate a Reset, even if the clock is not running. The minimum pulse length is given in [Table 8-1 on page 41](#). Shorter pulses are not guaranteed to generate a Reset.

Depending on the clock selection fuse settings, PE1 can be used as input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

Depending on the clock selection fuse settings, PE2 can be used as output from the inverting Oscillator amplifier.

The various special features of Port E are elaborated in [“Alternate Functions of Port E” on page 71](#) and [“Clock Systems and their Distribution” on page 25](#).

3.2.7 **AVCC**

AVCC is the supply voltage pin for the A/D Converter. It should be externally connected to V_{CC} , even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter.

3.2.8 **AREF**

This is the analog reference pin for the A/D Converter.

3.3 **About Code Examples**

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

4. Register Summary

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Page |
|---------|----------|---------|----------|---------|---------|----------|----------|----------|---------|---------------------|
| (0xFF) | PICR2H | | | | | | | | | page 161 |
| (0xFE) | PICR2L | | | | | | | | | page 161 |
| (0xFD) | PFRC2B | PCAE2B | PISEL2B | PELEV2B | PFLTE2B | PRFM2B3 | PRFM2B2 | PRFM2B1 | PRFM2B0 | page 160 |
| (0xFC) | PFRC2A | PCAE2A | PISEL2A | PELEV2A | PFLTE2A | PRFM2A3 | PRFM2A2 | PRFM2A1 | PRFM2A0 | page 159 |
| (0xFB) | PCTL2 | PPRE21 | PPRE20 | PBFM2 | PAOC2B | PAOC2A | PARUN2 | PCCYC2 | PRUN2 | page 159 |
| (0xFA) | PCNF2 | PFIFTY2 | PALOCK2 | PLOCK2 | PMODE21 | PMODE20 | POP2 | PCLKSEL2 | POME2 | page 156 |
| (0xF9) | OCR2RBH | | | | | | | | | page 155 |
| (0xF8) | OCR2RBL | | | | | | | | | page 155 |
| (0xF7) | OCR2SBH | | | | | | | | | page 155 |
| (0xF6) | OCR2SBL | | | | | | | | | page 155 |
| (0xF5) | OCR2RAH | | | | | | | | | page 155 |
| (0xF4) | OCR2RAL | | | | | | | | | page 155 |
| (0xF3) | OCR2SAH | | | | | | | | | page 155 |
| (0xF2) | OCR2SAL | | | | | | | | | page 155 |
| (0xF1) | POM2 | POMV2B3 | POMV2B2 | POMV2B1 | POMV2B0 | POMV2A3 | POMV2A2 | POMV2A1 | POMV2A0 | page 162 |
| (0xF0) | PSOC2 | POS23 | POS22 | PSYNC21 | PSYNC20 | POEN2D | POEN2B | POEN2C | POEN2A | page 154 |
| (0xEF) | PICR1H | | | | | | | | | page 161 |
| (0xEE) | PICR1L | | | | | | | | | page 161 |
| (0xED) | PFRC1B | PCAE1B | PISEL1B | PELEV1B | PFLTE1B | PRFM1B3 | PRFM1B2 | PRFM1B1 | PRFM1B0 | page 160 |
| (0xEC) | PFRC1A | PCAE1A | PISEL1A | PELEV1A | PFLTE1A | PRFM1A3 | PRFM1A2 | PRFM1A1 | PRFM1A0 | page 159 |
| (0xEB) | PCTL1 | PPRE11 | PPRE10 | PBFM1 | PAOC1B | PAOC1A | PARUN1 | PCCYC1 | PRUN1 | page 158 |
| (0xEA) | PCNF1 | PFIFTY1 | PALOCK1 | PLOCK1 | PMODE11 | PMODE10 | POP1 | PCLKSEL1 | - | page 156 |
| (0xE9) | OCR1RBH | | | | | | | | | page 155 |
| (0xE8) | OCR1RBL | | | | | | | | | page 155 |
| (0xE7) | OCR1SBH | | | | | | | | | page 155 |
| (0xE6) | OCR1SBL | | | | | | | | | page 155 |
| (0xE5) | OCR1RAH | | | | | | | | | page 155 |
| (0xE4) | OCR1RAL | | | | | | | | | page 155 |
| (0xE3) | OCR1SAH | | | | | | | | | page 155 |
| (0xE2) | OCR1SAL | | | | | | | | | page 155 |
| (0xE1) | Reserved | - | - | - | - | - | - | - | - | |
| (0xE0) | PSOC1 | - | - | PSYNC11 | PSYNC10 | - | POEN1B | - | POEN1A | page 153 |
| (0xDF) | PICR0H | | | | | | | | | page 161 |
| (0xDE) | PICR0L | | | | | | | | | page 161 |
| (0xDD) | PFRC0B | PCAE0B | PISEL0B | PELEV0B | PFLTE0B | PRFM0B3 | PRFM0B2 | PRFM0B1 | PRFM0B0 | page 160 |
| (0xDC) | PFRC0A | PCAE0A | PISEL0A | PELEV0A | PFLTE0A | PRFM0A3 | PRFM0A2 | PRFM0A1 | PRFM0A0 | page 159 |
| (0xDB) | PCTL0 | PPRE01 | PPRE00 | PBFM0 | PAOC0B | PAOC0A | PARUN0 | PCCYC0 | PRUN0 | page 157 |
| (0xDA) | PCNF0 | PFIFTY0 | PALOCK0 | PLOCK0 | PMODE01 | PMODE00 | POP0 | PCLKSEL0 | - | page 155 |
| (0xD9) | OCR0RBH | | | | | | | | | page 155 |
| (0xD8) | OCR0RBL | | | | | | | | | page 155 |
| (0xD7) | OCR0SBH | | | | | | | | | page 155 |
| (0xD6) | OCR0SBL | | | | | | | | | page 155 |
| (0xD5) | OCR0RAH | | | | | | | | | page 155 |
| (0xD4) | OCR0RAL | | | | | | | | | page 155 |
| (0xD3) | OCR0SAH | | | | | | | | | page 155 |
| (0xD2) | OCR0SAL | | | | | | | | | page 155 |
| (0xD1) | Reserved | - | - | - | - | - | - | - | - | |
| (0xD0) | PSOC0 | - | - | PSYNC01 | PSYNC00 | - | POEN0B | - | POEN0A | page 153 |
| (0xCF) | Reserved | - | - | - | - | - | - | - | - | |
| (0xCE) | EUDR | EUDR7 | EUDR6 | EUDR5 | EUDR4 | EUDR3 | EUDR2 | EUDR1 | EUDR0 | page 209 |
| (0xCD) | MUBRRH | MUBRR15 | MUBRR014 | MUBRR13 | MUBRR12 | MUBRR011 | MUBRR010 | MUBRR9 | MUBRR8 | page 214 |
| (0xCC) | MUBRRL | MUBRR7 | MUBRR6 | MUBRR5 | MUBRR4 | MUBRR3 | MUBRR2 | MUBRR1 | MUBRR0 | page 214 |
| (0xCB) | Reserved | - | - | - | - | - | - | - | - | |
| (0xCA) | EUCSRC | - | - | - | - | FEM | F1617 | STP1 | STP0 | page 213 |
| (0xC9) | EUCSRB | - | - | - | EUSART | EUSBS | - | EMCH | BODR | page 212 |
| (0xC8) | EUCSRA | UTxS3 | UTxS2 | UTxS1 | UTxS0 | URxS3 | URxS2 | URxS1 | URxS0 | page 211 |
| (0xC7) | Reserved | - | - | - | - | - | - | - | - | |
| (0xC6) | UDR | UDR07 | UDR06 | UDR05 | UDR04 | UDR03 | UDR02 | UDR01 | UDR00 | page 209 & page 191 |
| (0xC5) | UBRRH | - | - | - | - | UBRR011 | UBRR010 | UBRR09 | UBRR08 | page 195 |
| (0xC4) | UBRRL | UBRR07 | UBRR06 | UBRR05 | UBRR04 | UBRR03 | UBRR02 | UBRR01 | UBRR00 | page 195 |
| (0xC3) | Reserved | - | - | - | - | - | - | - | - | |
| (0xC2) | UCSRC | - | UMSEL0 | UPM01 | UPM00 | USBS0 | UCSZ01 | UCSZ00 | UCPOL0 | page 194 |
| (0xC1) | UCSRB | RXCIE0 | TXCIE0 | UDRIE0 | RXEN0 | TXEN0 | UCSZ02 | RXB80 | TXB80 | page 193 |
| (0xC0) | UCSRA | RXC0 | TXC0 | UDRE0 | FE0 | DOR0 | UPE0 | U2X0 | MPCM0 | page 191 |
| (0xBF) | Reserved | - | - | - | - | - | - | - | - | |
| (0xBE) | Reserved | - | - | - | - | - | - | - | - | |

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Page |
|---------|----------|-------------|-------------|----------|----------|--------------|---------------|--------------|--------------|--------------------------|
| (0xBD) | Reserved | - | - | - | - | - | - | - | - | |
| (0xBC) | Reserved | - | - | - | - | - | - | - | - | |
| (0xBB) | Reserved | - | - | - | - | - | - | - | - | |
| (0xBA) | Reserved | - | - | - | - | - | - | - | - | |
| (0xB9) | Reserved | - | - | - | - | - | - | - | - | |
| (0xB8) | Reserved | - | - | - | - | - | - | - | - | |
| (0xB7) | Reserved | - | - | - | - | - | - | - | - | |
| (0xB6) | Reserved | - | - | - | - | - | - | - | - | |
| (0xB5) | Reserved | - | - | - | - | - | - | - | - | |
| (0xB4) | Reserved | - | - | - | - | - | - | - | - | |
| (0xB3) | Reserved | - | - | - | - | - | - | - | - | |
| (0xB2) | Reserved | - | - | - | - | - | - | - | - | |
| (0xB1) | Reserved | - | - | - | - | - | - | - | - | |
| (0xB0) | Reserved | - | - | - | - | - | - | - | - | |
| (0xAF) | AC2CON | AC2EN | AC2IE | AC2IS1 | AC2IS0 | - | AC2M2 | AC2M1 | AC2M0 | page 218 |
| (0xAE) | AC1CON | AC1EN | AC1IE | AC1IS1 | AC1IS0 | AC1ICE | AC1M2 | AC1M1 | AC1M0 | page 217 |
| (0xAD) | AC0CON | AC0EN | AC0IE | AC0IS1 | AC0IS0 | - | AC0M2 | AC0M1 | AC0M0 | page 216 |
| (0xAC) | DACH | - / DAC9 | - / DAC8 | - / DAC7 | - / DAC6 | - / DAC5 | - / DAC4 | DAC9 / DAC3 | DAC8 / DAC2 | page 247 |
| (0xAB) | DAACL | DAC7 / DAC1 | DAC6 / DAC0 | DAC5 / - | DAC4 / - | DAC3 / - | DAC2 / - | DAC1 / - | DAC0 / | page 247 |
| (0xAA) | DACON | DAATE | DATS2 | DATS1 | DATS0 | - | DALA | DAOE | DAEN | page 246 |
| (0xA9) | Reserved | - | - | - | - | - | - | - | - | |
| (0xA8) | Reserved | - | - | - | - | - | - | - | - | |
| (0xA7) | Reserved | - | - | - | - | - | - | - | - | |
| (0xA6) | Reserved | - | - | - | - | - | - | - | - | |
| (0xA5) | PIM2 | - | - | PSEIE2 | PEVE2B | PEVE2A | - | - | PEOPE2 | page 162 |
| (0xA4) | PIFR2 | - | - | PSEIE1 | PEVE2B | PEVE2A | PRN21 | PRN20 | PEOP2 | page 163 |
| (0xA3) | PIM1 | - | - | PSEIE1 | PEVE1B | PEVE1A | - | - | PEOPE1 | page 162 |
| (0xA2) | PIFR1 | - | - | PSEIE1 | PEVE1B | PEVE1A | PRN11 | PRN10 | PEOP1 | page 163 |
| (0xA1) | PIM0 | - | - | PSEIE0 | PEVE0B | PEVE0A | - | - | PEOPE0 | page 162 |
| (0xA0) | PIFR0 | - | - | PSEIE0 | PEVE0B | PEVE0A | PRN01 | PRN00 | PEOP0 | page 163 |
| (0x9F) | Reserved | - | - | - | - | - | - | - | - | |
| (0x9E) | Reserved | - | - | - | - | - | - | - | - | |
| (0x9D) | Reserved | - | - | - | - | - | - | - | - | |
| (0x9C) | Reserved | - | - | - | - | - | - | - | - | |
| (0x9B) | Reserved | - | - | - | - | - | - | - | - | |
| (0x9A) | Reserved | - | - | - | - | - | - | - | - | |
| (0x99) | Reserved | - | - | - | - | - | - | - | - | |
| (0x98) | Reserved | - | - | - | - | - | - | - | - | |
| (0x97) | Reserved | - | - | - | - | - | - | - | - | |
| (0x96) | Reserved | - | - | - | - | - | - | - | - | |
| (0x95) | Reserved | - | - | - | - | - | - | - | - | |
| (0x94) | Reserved | - | - | - | - | - | - | - | - | |
| (0x93) | Reserved | - | - | - | - | - | - | - | - | |
| (0x92) | Reserved | - | - | - | - | - | - | - | - | |
| (0x91) | Reserved | - | - | - | - | - | - | - | - | |
| (0x90) | Reserved | - | - | - | - | - | - | - | - | |
| (0x8F) | Reserved | - | - | - | - | - | - | - | - | |
| (0x8E) | Reserved | - | - | - | - | - | - | - | - | |
| (0x8D) | Reserved | - | - | - | - | - | - | - | - | |
| (0x8C) | Reserved | - | - | - | - | - | - | - | - | |
| (0x8B) | OCR1BH | OCR1B15 | OCR1B14 | OCR1B13 | OCR1B12 | OCR1B11 | OCR1B10 | OCR1B9 | OCR1B8 | page 119 |
| (0x8A) | OCR1BL | OCR1B7 | OCR1B6 | OCR1B5 | OCR1B4 | OCR1B3 | OCR1B2 | OCR1B1 | OCR1B0 | page 119 |
| (0x89) | OCR1AH | OCR1A15 | OCR1A14 | OCR1A13 | OCR1A12 | OCR1A11 | OCR1A10 | OCR1A9 | OCR1A8 | page 119 |
| (0x88) | OCR1AL | OCR1A7 | OCR1A6 | OCR1A5 | OCR1A4 | OCR1A3 | OCR1A2 | OCR1A1 | OCR1A0 | page 119 |
| (0x87) | ICR1H | ICR115 | ICR114 | ICR113 | ICR112 | ICR111 | ICR110 | ICR19 | ICR18 | page 119 |
| (0x86) | ICR1L | ICR17 | ICR16 | ICR15 | ICR14 | ICR13 | ICR12 | ICR11 | ICR10 | page 119 |
| (0x85) | TCNT1H | TCNT115 | TCNT114 | TCNT113 | TCNT112 | TCNT111 | TCNT110 | TCNT19 | TCNT18 | page 119 |
| (0x84) | TCNT1L | TCNT17 | TCNT16 | TCNT15 | TCNT14 | TCNT13 | TCNT12 | TCNT11 | TCNT10 | page 119 |
| (0x83) | Reserved | - | - | - | - | - | - | - | - | |
| (0x82) | TCCR1C | FOC1A | FOC1B | - | - | - | - | - | - | page 118 |
| (0x81) | TCCR1B | ICNC1 | ICES1 | - | WGM13 | WGM12 | CS12 | CS11 | CS10 | page 117 |
| (0x80) | TCCR1A | COM1A1 | COM1A0 | COM1B1 | COM1B0 | - | - | WGM11 | WGM10 | page 114 |
| (0x7F) | DIDR1 | - | - | ACMP0D | AMP0PD | AMP0ND | ADC10D/ACMP1D | ADC9D/AMP1PD | ADC8D/AMP1ND | page 239 |
| (0x7E) | DIDR0 | ADC7D | ADC6D | ADC5D | ADC4D | ADC3D/ACMPMD | ADC2D/ACMP2D | ADC1D | ADC0D | page 239 |
| (0x7D) | Reserved | - | - | - | - | - | - | - | - | |
| (0x7C) | ADMUX | REFS1 | REFS0 | ADLAR | - | MUX3 | MUX2 | MUX1 | MUX0 | page 235 |
| (0x7B) | ADCSRB | ADHSM | - | - | - | ADTS3 | ADTS2 | ADTS1 | ADTS0 | page 237 |
| (0x7A) | ADCSRA | ADEN | ADSC | ADATE | ADIF | ADIE | ADPS2 | ADPS1 | ADPS0 | page 236 |

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Page | |
|-------------|----------|------------------------------------|-------------|----------|----------|----------|----------|-------------|-------------|---------------------------------------|--------------------------|
| (0x79) | ADCH | - / ADC9 | - / ADC8 | - / ADC7 | - / ADC6 | - / ADC5 | - / ADC4 | ADC9 / ADC3 | ADC8 / ADC2 | page 238 | |
| (0x78) | ADCL | ADC7 / ADC1 | ADC6 / ADC0 | ADC5 / - | ADC4 / - | ADC3 / - | ADC2 / - | ADC1 / - | ADC0 / - | page 238 | |
| (0x77) | AMP1CSR | AMP1EN | - | AMP1G1 | AMP1G0 | - | AMP1TS1 | AMP1TS1 | AMP1TS0 | page 244 | |
| (0x76) | AMP0CSR | AMP0EN | - | AMP0G1 | AMP0G0 | - | AMP0TS2 | AMP0TS1 | AMP0TS0 | page 243 | |
| (0x75) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x74) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x73) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x72) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x71) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x70) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x6F) | TIMSK1 | - | - | ICIE1 | - | - | OCIE1B | OCIE1A | TOIE1 | page 120 | |
| (0x6E) | TIMSK0 | - | - | - | - | - | OCIE0B | OCIE0A | TOIE0 | page 93 | |
| (0x6D) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x6C) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x6B) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x6A) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x69) | EICRA | ISC31 | ISC30 | ISC21 | ISC20 | ISC11 | ISC10 | ISC01 | ISC00 | page 75 | |
| (0x68) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x67) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x66) | OSCCAL | - | CAL6 | CAL5 | CAL4 | CAL3 | CAL2 | CAL1 | CAL0 | page 29 | |
| (0x65) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x64) | PRR | PRPSC2 | PRPSC1 | PRPSC0 | PRTIM1 | PRTIM0 | PRSPI | PRUSART | PRADC | page 37 | |
| (0x63) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x62) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x61) | CLKPR | CLKPCE | - | - | - | CLKPS3 | CLKPS2 | CLKPS1 | CLKPS0 | page 33 | |
| (0x60) | WDTCSR | WDIF | WDIE | WDP3 | WDCE | WDE | WDP2 | WDP1 | WDP0 | page 48 | |
| 0x3F (0x5F) | SREG | I | T | H | S | V | N | Z | C | page 11 | |
| 0x3E (0x5E) | SPH | SP15 | SP14 | SP13 | SP12 | SP11 | SP10 | SP9 | SP8 | page 14 | |
| 0x3D (0x5D) | SPL | SP7 | SP6 | SP5 | SP4 | SP3 | SP2 | SP1 | SP0 | page 14 | |
| 0x3C (0x5C) | Reserved | - | - | - | - | - | - | - | - | | |
| 0x3B (0x5B) | Reserved | - | - | - | - | - | - | - | - | | |
| 0x3A (0x5A) | Reserved | - | - | - | - | - | - | - | - | | |
| 0x39 (0x59) | Reserved | - | - | - | - | - | - | - | - | | |
| 0x38 (0x58) | Reserved | - | - | - | - | - | - | - | - | | |
| 0x37 (0x57) | SPMCSR | SPMIE | RWWWSB | - | RWWWSRE | BLBSET | PGWRT | PGERS | SPMEN | page 256 | |
| 0x36 (0x56) | Reserved | - | - | - | - | - | - | - | - | | |
| 0x35 (0x55) | MCUCR | SPIPS | - | - | PUD | - | - | IVSEL | IVCE | page 54 & page 62 | |
| 0x34 (0x54) | MCUSR | - | - | - | - | WDRF | BORF | EXTRF | PORF | page 44 | |
| 0x33 (0x53) | SMCR | - | - | - | - | SM2 | SM1 | SM0 | SE | page 35 | |
| 0x32 (0x52) | MSMCR | Monitor Stop Mode Control Register | | | | | | | | reserved | |
| 0x31 (0x51) | MONDR | Monitor Data Register | | | | | | | | reserved | |
| 0x30 (0x50) | ACSR | - | AC2IF | AC1IF | AC0IF | - | - | AC2O | AC1O | AC0O | page 219 |
| 0x2F (0x4F) | Reserved | - | - | - | - | - | - | - | - | | |
| 0x2E (0x4E) | SPDR | SPD7 | SPD6 | SPD5 | SPD4 | SPD3 | SPD2 | SPD1 | SPD0 | page 171 | |
| 0x2D (0x4D) | SPSR | SPIF | WCOL | - | - | - | - | - | SPI2X | page 171 | |
| 0x2C (0x4C) | SPCR | SPIE | SPE | DORD | MSTR | CPOL | CPHA | SPR1 | SPR0 | page 169 | |
| 0x2B (0x4B) | Reserved | - | - | - | - | - | - | - | - | | |
| 0x2A (0x4A) | Reserved | - | - | - | - | - | - | - | - | | |
| 0x29 (0x49) | PLLCSR | - | - | - | - | - | PLLF | PLLE | PLOCK | page 31 | |
| 0x28 (0x48) | OCR0B | OCR0B7 | OCR0B6 | OCR0B5 | OCR0B4 | OCR0B3 | OCR0B2 | OCR0B1 | OCR0B0 | page 93 | |
| 0x27 (0x47) | OCR0A | OCR0A7 | OCR0A6 | OCR0A5 | OCR0A4 | OCR0A3 | OCR0A2 | OCR0A1 | OCR0A0 | page 93 | |
| 0x26 (0x46) | TCNT0 | TCNT07 | TCNT06 | TCNT05 | TCNT04 | TCNT03 | TCNT02 | TCNT01 | TCNT00 | page 93 | |
| 0x25 (0x45) | TCCR0B | FOC0A | FOC0B | - | - | WGM02 | CS02 | CS01 | CS00 | page 91 | |
| 0x24 (0x44) | TCCR0A | COM0A1 | COM0A0 | COM0B1 | COM0B0 | - | - | WGM01 | WGM00 | page 89 | |
| 0x23 (0x43) | GTCCR | TSM | ICPSEL1 | - | - | - | - | - | PSRSYNC | page 78 | |
| 0x22 (0x42) | EEARH | - | - | - | - | EEAR11 | EEAR10 | EEAR9 | EEAR8 | page 19 | |
| 0x21 (0x41) | EEARL | EEAR7 | EEAR6 | EEAR5 | EEAR4 | EEAR3 | EEAR2 | EEAR1 | EEAR0 | page 19 | |
| 0x20 (0x40) | EEDR | EEDR7 | EEDR6 | EEDR5 | EEDR4 | EEDR3 | EEDR2 | EEDR1 | EEDR0 | page 19 | |
| 0x1F (0x3F) | EECR | - | - | - | - | EERIE | EEMWE | EEWE | EERE | page 20 | |
| 0x1E (0x3E) | GPOR0 | GPOR07 | GPOR06 | GPOR05 | GPOR04 | GPOR03 | GPOR02 | GPOR01 | GPOR00 | page 24 | |
| 0x1D (0x3D) | EIMSK | - | - | - | - | INT3 | INT2 | INT1 | INT0 | page 76 | |
| 0x1C (0x3C) | EIFR | - | - | - | - | INTF3 | INTF2 | INTF1 | INTF0 | page 76 | |
| 0x1B (0x3B) | GPOR3 | GPOR37 | GPOR36 | GPOR35 | GPOR34 | GPOR33 | GPOR32 | GPOR31 | GPOR30 | page 24 | |
| 0x1A (0x3A) | GPOR2 | GPOR27 | GPOR26 | GPOR25 | GPOR24 | GPOR23 | GPOR22 | GPOR21 | GPOR20 | page 24 | |
| 0x19 (0x39) | GPOR1 | GPOR17 | GPOR16 | GPOR15 | GPOR14 | GPOR13 | GPOR12 | GPOR11 | GPOR10 | page 24 | |
| 0x18 (0x38) | Reserved | - | - | - | - | - | - | - | - | | |
| 0x17 (0x37) | Reserved | - | - | - | - | - | - | - | - | | |
| 0x16 (0x36) | TIFR1 | - | - | ICF1 | - | - | OCF1B | OCF1A | TOV1 | page 120 | |

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Page |
|-------------|-----------------|--------|--------|--------|--------|--------|--------|--------|--------|-------------------------|
| 0x15 (0x35) | TIFR0 | – | – | – | – | – | OCF0B | OCF0A | TOV0 | page 94 |
| 0x14 (0x34) | Reserved | – | – | – | – | – | – | – | – | |
| 0x13 (0x33) | Reserved | – | – | – | – | – | – | – | – | |
| 0x12 (0x32) | Reserved | – | – | – | – | – | – | – | – | |
| 0x11 (0x31) | Reserved | – | – | – | – | – | – | – | – | |
| 0x10 (0x30) | Reserved | – | – | – | – | – | – | – | – | |
| 0x0F (0x2F) | Reserved | – | – | – | – | – | – | – | – | |
| 0x0E (0x2E) | PORTE | – | – | – | – | – | PORTE2 | PORTE1 | PORTE0 | page 74 |
| 0x0D (0x2D) | DDRE | – | – | – | – | – | DDE2 | DDE1 | DDE0 | page 74 |
| 0x0C (0x2C) | PINE | – | – | – | – | – | PINE2 | PINE1 | PINE0 | page 74 |
| 0x0B (0x2B) | PORTD | PORTD7 | PORTD6 | PORTD5 | PORTD4 | PORTD3 | PORTD2 | PORTD1 | PORTD0 | page 73 |
| 0x0A (0x2A) | DDRD | DDD7 | DDD6 | DDD5 | DDD4 | DDD3 | DDD2 | DDD1 | DDD0 | page 73 |
| 0x09 (0x29) | PIND | PIND7 | PIND6 | PIND5 | PIND4 | PIND3 | PIND2 | PIND1 | PIND0 | page 74 |
| 0x08 (0x28) | PORTC | PORTC7 | PORTC6 | PORTC5 | PORTC4 | PORTC3 | PORTC2 | PORTC1 | PORTC0 | page 73 |
| 0x07 (0x27) | DDRC | DDC7 | DDC6 | DDC5 | DDC4 | DDC3 | DDC2 | DDC1 | DDC0 | page 73 |
| 0x06 (0x26) | PINC | PINC7 | PINC6 | PINC5 | PINC4 | PINC3 | PINC2 | PINC1 | PINC0 | page 73 |
| 0x05 (0x25) | PORTB | PORTB7 | PORTB6 | PORTB5 | PORTB4 | PORTB3 | PORTB2 | PORTB1 | PORTB0 | page 73 |
| 0x04 (0x24) | DDRB | DDB7 | DDB6 | DDB5 | DDB4 | DDB3 | DDB2 | DDB1 | DDB0 | page 73 |
| 0x03 (0x23) | PINB | PINB7 | PINB6 | PINB5 | PINB4 | PINB3 | PINB2 | PINB1 | PINB0 | page 73 |
| 0x02 (0x22) | Reserved | – | – | – | – | – | – | – | – | |
| 0x01 (0x21) | Reserved | – | – | – | – | – | – | – | – | |
| 0x00 (0x20) | Reserved | – | – | – | – | – | – | – | – | |

- Note:
1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
 2. I/O Registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
 3. Some of the status flags are cleared by writing a logical one to them. Note that, unlike most other AVR, the CBI and SBI instructions will only operate on the specified bit, and can therefore be used on registers containing such status flags. The CBI and SBI instructions work with registers 0x00 to 0x1F only.
 4. When using the I/O specific commands IN and OUT, the I/O addresses 0x00 - 0x3F must be used. When addressing I/O Registers as data space using LD and ST instructions, 0x20 must be added to these addresses. The AT90PWM216/316 is a complex microcontroller with more peripheral units than can be supported within the 64 location reserved in Opcode for the IN and OUT instructions. For the Extended I/O space from 0x60 - 0xFF in SRAM, only the ST/STS/STD and LD/LDS/LDD instructions can be used.

5. Instruction Set Summary

| Mnemonics | Operands | Description | Operation | Flags | #Clocks |
|--|----------|--|---|------------|---------|
| ARITHMETIC AND LOGIC INSTRUCTIONS | | | | | |
| ADD | Rd, Rr | Add two Registers | $Rd \leftarrow Rd + Rr$ | Z,C,N,V,H | 1 |
| ADC | Rd, Rr | Add with Carry two Registers | $Rd \leftarrow Rd + Rr + C$ | Z,C,N,V,H | 1 |
| ADIW | RdI,K | Add Immediate to Word | $Rdh:Rdl \leftarrow Rdh:Rdl + K$ | Z,C,N,V,S | 2 |
| SUB | Rd, Rr | Subtract two Registers | $Rd \leftarrow Rd - Rr$ | Z,C,N,V,H | 1 |
| SUBI | Rd, K | Subtract Constant from Register | $Rd \leftarrow Rd - K$ | Z,C,N,V,H | 1 |
| SBC | Rd, Rr | Subtract with Carry two Registers | $Rd \leftarrow Rd - Rr - C$ | Z,C,N,V,H | 1 |
| SBCI | Rd, K | Subtract with Carry Constant from Reg. | $Rd \leftarrow Rd - K - C$ | Z,C,N,V,H | 1 |
| SBIW | RdI,K | Subtract Immediate from Word | $Rdh:Rdl \leftarrow Rdh:Rdl - K$ | Z,C,N,V,S | 2 |
| AND | Rd, Rr | Logical AND Registers | $Rd \leftarrow Rd \cdot Rr$ | Z,N,V | 1 |
| ANDI | Rd, K | Logical AND Register and Constant | $Rd \leftarrow Rd \cdot K$ | Z,N,V | 1 |
| OR | Rd, Rr | Logical OR Registers | $Rd \leftarrow Rd \vee Rr$ | Z,N,V | 1 |
| ORI | Rd, K | Logical OR Register and Constant | $Rd \leftarrow Rd \vee K$ | Z,N,V | 1 |
| EOR | Rd, Rr | Exclusive OR Registers | $Rd \leftarrow Rd \oplus Rr$ | Z,N,V | 1 |
| COM | Rd | One's Complement | $Rd \leftarrow 0xFF - Rd$ | Z,C,N,V | 1 |
| NEG | Rd | Two's Complement | $Rd \leftarrow 0x00 - Rd$ | Z,C,N,V,H | 1 |
| SBR | Rd,K | Set Bit(s) in Register | $Rd \leftarrow Rd \vee K$ | Z,N,V | 1 |
| CBR | Rd,K | Clear Bit(s) in Register | $Rd \leftarrow Rd \cdot (0xFF - K)$ | Z,N,V | 1 |
| INC | Rd | Increment | $Rd \leftarrow Rd + 1$ | Z,N,V | 1 |
| DEC | Rd | Decrement | $Rd \leftarrow Rd - 1$ | Z,N,V | 1 |
| TST | Rd | Test for Zero or Minus | $Rd \leftarrow Rd \cdot Rd$ | Z,N,V | 1 |
| CLR | Rd | Clear Register | $Rd \leftarrow Rd \oplus Rd$ | Z,N,V | 1 |
| SER | Rd | Set Register | $Rd \leftarrow 0xFF$ | None | 1 |
| MUL | Rd, Rr | Multiply Unsigned | $R1:R0 \leftarrow Rd \times Rr$ | Z,C | 2 |
| MULS | Rd, Rr | Multiply Signed | $R1:R0 \leftarrow Rd \times Rr$ | Z,C | 2 |
| MULSU | Rd, Rr | Multiply Signed with Unsigned | $R1:R0 \leftarrow Rd \times Rr$ | Z,C | 2 |
| FMUL | Rd, Rr | Fractional Multiply Unsigned | $R1:R0 \leftarrow (Rd \times Rr) \ll 1$ | Z,C | 2 |
| FMULS | Rd, Rr | Fractional Multiply Signed | $R1:R0 \leftarrow (Rd \times Rr) \ll 1$ | Z,C | 2 |
| FMULSU | Rd, Rr | Fractional Multiply Signed with Unsigned | $R1:R0 \leftarrow (Rd \times Rr) \ll 1$ | Z,C | 2 |
| BRANCH INSTRUCTIONS | | | | | |
| RJMP | k | Relative Jump | $PC \leftarrow PC + k + 1$ | None | 2 |
| IJMP | | Indirect Jump to (Z) | $PC \leftarrow Z$ | None | 2 |
| JMP | k | Direct Jump | $PC \leftarrow k$ | None | 3 |
| RCALL | k | Relative Subroutine Call | $PC \leftarrow PC + k + 1$ | None | 3 |
| ICALL | | Indirect Call to (Z) | $PC \leftarrow Z$ | None | 3 |
| CALL | k | Direct Call | $PC \leftarrow k$ | None | 4 |
| RET | | Subroutine Return | $PC \leftarrow STACK$ | None | 4 |
| RETI | | Interrupt Return | $PC \leftarrow STACK$ | I | 4 |
| CPSE | Rd,Rr | Compare, Skip if Equal | if $(Rd = Rr)$ $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| CP | Rd,Rr | Compare | $Rd - Rr$ | Z, N,V,C,H | 1 |
| CPC | Rd,Rr | Compare with Carry | $Rd - Rr - C$ | Z, N,V,C,H | 1 |
| CPI | Rd,K | Compare Register with Immediate | $Rd - K$ | Z, N,V,C,H | 1 |
| SBRC | Rr, b | Skip if Bit in Register Cleared | if $(Rr(b)=0)$ $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| SBRS | Rr, b | Skip if Bit in Register is Set | if $(Rr(b)=1)$ $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| SBIC | P, b | Skip if Bit in I/O Register Cleared | if $(P(b)=0)$ $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| SBIS | P, b | Skip if Bit in I/O Register is Set | if $(P(b)=1)$ $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| BRBS | s, k | Branch if Status Flag Set | if $(SREG(s) = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRBC | s, k | Branch if Status Flag Cleared | if $(SREG(s) = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BREQ | k | Branch if Equal | if $(Z = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRNE | k | Branch if Not Equal | if $(Z = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRCS | k | Branch if Carry Set | if $(C = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRCC | k | Branch if Carry Cleared | if $(C = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRSH | k | Branch if Same or Higher | if $(C = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRLO | k | Branch if Lower | if $(C = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRMI | k | Branch if Minus | if $(N = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRPL | k | Branch if Plus | if $(N = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRGE | k | Branch if Greater or Equal, Signed | if $(N \oplus V = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRLT | k | Branch if Less Than Zero, Signed | if $(N \oplus V = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRHS | k | Branch if Half Carry Flag Set | if $(H = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRHC | k | Branch if Half Carry Flag Cleared | if $(H = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRTS | k | Branch if T Flag Set | if $(T = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRTC | k | Branch if T Flag Cleared | if $(T = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRVS | k | Branch if Overflow Flag is Set | if $(V = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRVC | k | Branch if Overflow Flag is Cleared | if $(V = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRIE | k | Branch if Interrupt Enabled | if $(I = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRID | k | Branch if Interrupt Disabled | if $(I = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |

| Mnemonics | Operands | Description | Operation | Flags | #Clocks |
|--------------------------------------|----------|----------------------------------|--|---------|---------|
| BIT AND BIT-TEST INSTRUCTIONS | | | | | |
| SBI | P,b | Set Bit in I/O Register | $I/O(P,b) \leftarrow 1$ | None | 2 |
| CBI | P,b | Clear Bit in I/O Register | $I/O(P,b) \leftarrow 0$ | None | 2 |
| LSL | Rd | Logical Shift Left | $Rd(n+1) \leftarrow Rd(n), Rd(0) \leftarrow 0$ | Z,C,N,V | 1 |
| LSR | Rd | Logical Shift Right | $Rd(n) \leftarrow Rd(n+1), Rd(7) \leftarrow 0$ | Z,C,N,V | 1 |
| ROL | Rd | Rotate Left Through Carry | $Rd(0) \leftarrow C, Rd(n+1) \leftarrow Rd(n), C \leftarrow Rd(7)$ | Z,C,N,V | 1 |
| ROR | Rd | Rotate Right Through Carry | $Rd(7) \leftarrow C, Rd(n) \leftarrow Rd(n+1), C \leftarrow Rd(0)$ | Z,C,N,V | 1 |
| ASR | Rd | Arithmetic Shift Right | $Rd(n) \leftarrow Rd(n+1), n=0..6$ | Z,C,N,V | 1 |
| SWAP | Rd | Swap Nibbles | $Rd(3..0) \leftarrow Rd(7..4), Rd(7..4) \leftarrow Rd(3..0)$ | None | 1 |
| BSET | s | Flag Set | $SREG(s) \leftarrow 1$ | SREG(s) | 1 |
| BCLR | s | Flag Clear | $SREG(s) \leftarrow 0$ | SREG(s) | 1 |
| BST | Rr, b | Bit Store from Register to T | $T \leftarrow Rr(b)$ | T | 1 |
| BLD | Rd, b | Bit load from T to Register | $Rd(b) \leftarrow T$ | None | 1 |
| SEC | | Set Carry | $C \leftarrow 1$ | C | 1 |
| CLC | | Clear Carry | $C \leftarrow 0$ | C | 1 |
| SEN | | Set Negative Flag | $N \leftarrow 1$ | N | 1 |
| CLN | | Clear Negative Flag | $N \leftarrow 0$ | N | 1 |
| SEZ | | Set Zero Flag | $Z \leftarrow 1$ | Z | 1 |
| CLZ | | Clear Zero Flag | $Z \leftarrow 0$ | Z | 1 |
| SEI | | Global Interrupt Enable | $I \leftarrow 1$ | I | 1 |
| CLI | | Global Interrupt Disable | $I \leftarrow 0$ | I | 1 |
| SES | | Set Signed Test Flag | $S \leftarrow 1$ | S | 1 |
| CLS | | Clear Signed Test Flag | $S \leftarrow 0$ | S | 1 |
| SEV | | Set Twos Complement Overflow. | $V \leftarrow 1$ | V | 1 |
| CLV | | Clear Twos Complement Overflow | $V \leftarrow 0$ | V | 1 |
| SET | | Set T in SREG | $T \leftarrow 1$ | T | 1 |
| CLT | | Clear T in SREG | $T \leftarrow 0$ | T | 1 |
| SEH | | Set Half Carry Flag in SREG | $H \leftarrow 1$ | H | 1 |
| CLH | | Clear Half Carry Flag in SREG | $H \leftarrow 0$ | H | 1 |
| DATA TRANSFER INSTRUCTIONS | | | | | |
| MOV | Rd, Rr | Move Between Registers | $Rd \leftarrow Rr$ | None | 1 |
| MOVW | Rd, Rr | Copy Register Word | $Rd+1:Rd \leftarrow Rr+1:Rr$ | None | 1 |
| LDI | Rd, K | Load Immediate | $Rd \leftarrow K$ | None | 1 |
| LD | Rd, X | Load Indirect | $Rd \leftarrow (X)$ | None | 2 |
| LD | Rd, X+ | Load Indirect and Post-Inc. | $Rd \leftarrow (X), X \leftarrow X + 1$ | None | 2 |
| LD | Rd, -X | Load Indirect and Pre-Dec. | $X \leftarrow X - 1, Rd \leftarrow (X)$ | None | 2 |
| LD | Rd, Y | Load Indirect | $Rd \leftarrow (Y)$ | None | 2 |
| LD | Rd, Y+ | Load Indirect and Post-Inc. | $Rd \leftarrow (Y), Y \leftarrow Y + 1$ | None | 2 |
| LD | Rd, -Y | Load Indirect and Pre-Dec. | $Y \leftarrow Y - 1, Rd \leftarrow (Y)$ | None | 2 |
| LDD | Rd, Y+q | Load Indirect with Displacement | $Rd \leftarrow (Y + q)$ | None | 2 |
| LD | Rd, Z | Load Indirect | $Rd \leftarrow (Z)$ | None | 2 |
| LD | Rd, Z+ | Load Indirect and Post-Inc. | $Rd \leftarrow (Z), Z \leftarrow Z+1$ | None | 2 |
| LD | Rd, -Z | Load Indirect and Pre-Dec. | $Z \leftarrow Z - 1, Rd \leftarrow (Z)$ | None | 2 |
| LDD | Rd, Z+q | Load Indirect with Displacement | $Rd \leftarrow (Z + q)$ | None | 2 |
| LDS | Rd, k | Load Direct from SRAM | $Rd \leftarrow (k)$ | None | 2 |
| ST | X, Rr | Store Indirect | $(X) \leftarrow Rr$ | None | 2 |
| ST | X+, Rr | Store Indirect and Post-Inc. | $(X) \leftarrow Rr, X \leftarrow X + 1$ | None | 2 |
| ST | -X, Rr | Store Indirect and Pre-Dec. | $X \leftarrow X - 1, (X) \leftarrow Rr$ | None | 2 |
| ST | Y, Rr | Store Indirect | $(Y) \leftarrow Rr$ | None | 2 |
| ST | Y+, Rr | Store Indirect and Post-Inc. | $(Y) \leftarrow Rr, Y \leftarrow Y + 1$ | None | 2 |
| ST | -Y, Rr | Store Indirect and Pre-Dec. | $Y \leftarrow Y - 1, (Y) \leftarrow Rr$ | None | 2 |
| STD | Y+q, Rr | Store Indirect with Displacement | $(Y + q) \leftarrow Rr$ | None | 2 |
| ST | Z, Rr | Store Indirect | $(Z) \leftarrow Rr$ | None | 2 |
| ST | Z+, Rr | Store Indirect and Post-Inc. | $(Z) \leftarrow Rr, Z \leftarrow Z + 1$ | None | 2 |
| ST | -Z, Rr | Store Indirect and Pre-Dec. | $Z \leftarrow Z - 1, (Z) \leftarrow Rr$ | None | 2 |
| STD | Z+q, Rr | Store Indirect with Displacement | $(Z + q) \leftarrow Rr$ | None | 2 |
| STS | k, Rr | Store Direct to SRAM | $(k) \leftarrow Rr$ | None | 2 |
| LPM | | Load Program Memory | $R0 \leftarrow (Z)$ | None | 3 |
| LPM | Rd, Z | Load Program Memory | $Rd \leftarrow (Z)$ | None | 3 |
| LPM | Rd, Z+ | Load Program Memory and Post-Inc | $Rd \leftarrow (Z), Z \leftarrow Z+1$ | None | 3 |
| SPM | | Store Program Memory | $(Z) \leftarrow R1:R0$ | None | - |
| IN | Rd, P | In Port | $Rd \leftarrow P$ | None | 1 |
| OUT | P, Rr | Out Port | $P \leftarrow Rr$ | None | 1 |
| PUSH | Rr | Push Register on Stack | $STACK \leftarrow Rr$ | None | 2 |
| POP | Rd | Pop Register from Stack | $Rd \leftarrow STACK$ | None | 2 |
| MCU CONTROL INSTRUCTIONS | | | | | |
| NOP | | No Operation | | None | 1 |
| SLEEP | | Sleep | (see specific descr. for Sleep function) | None | 1 |

| Mnemonics | Operands | Description | Operation | Flags | #Clocks |
|-----------|----------|----------------|-------------------------------------|-------|---------|
| WDR | | Watchdog Reset | (see specific descr. for WDR/timer) | None | 1 |
| BREAK | | Break | For On-chip Debug Only | None | N/A |

6. Ordering Information

| Speed (MHz) | Power Supply | Ordering Code | Package | Operation Range |
|-------------|--------------|-----------------|---------|---------------------------|
| 16 | 2.7 - 5.5V | AT90PWM316-16SE | SO32 | Engineering Samples |
| 16 | 2.7 - 5.5V | AT90PWM316-16ME | QFN32 | Engineering Samples |
| 16 | 2.7 - 5.5V | AT90PWM216-16SE | SO24 | Engineering Samples |
| 16 | 2.7 - 5.5V | AT90PWM316-16SU | SO32 | Extended (-40°C to 105°C) |
| 16 | 2.7 - 5.5V | AT90PWM316-16MU | QFN32 | Extended (-40°C to 105°C) |
| 16 | 2.7 - 5.5V | AT90PWM216-16SU | SO24 | Extended (-40°C to 105°C) |

Note: All packages are Pb free, fully LHF

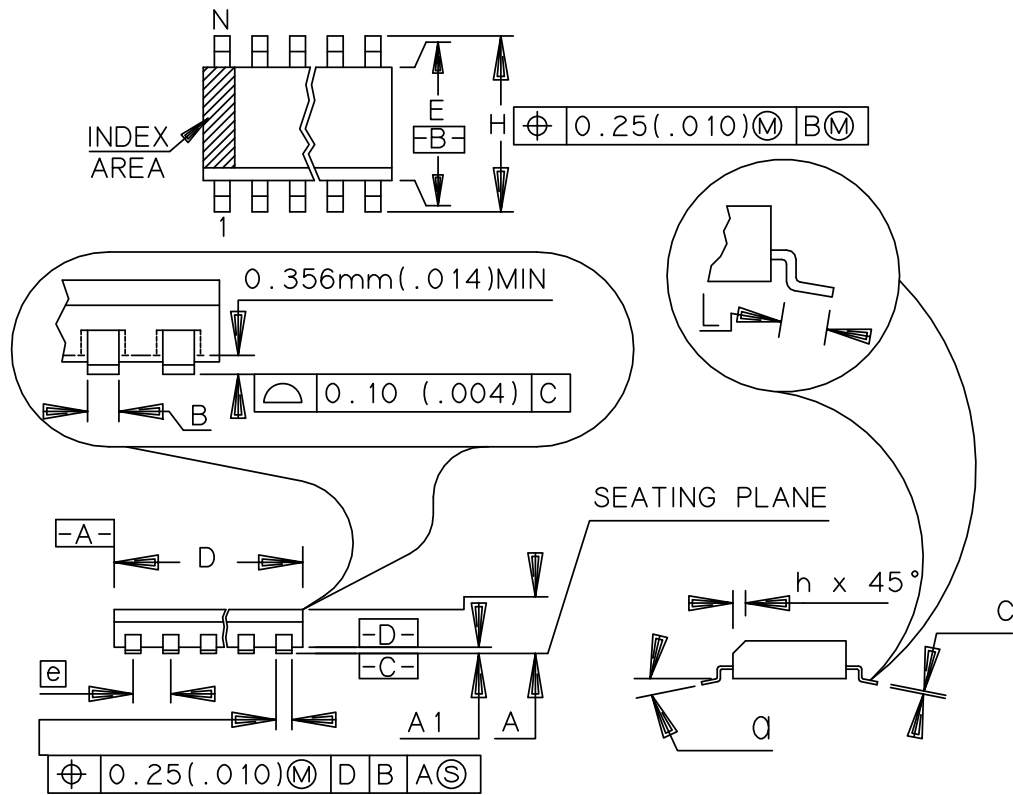
Note: This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

Note: Parts numbers are for shipping in sticks (SO) or in trays (QFN). These devices can also be supplied in Tape and Reel. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

7. Package Information

| Package Type | |
|--------------|--------------------------------|
| SO24 | 24-Lead, Small Outline Package |
| SO32 | 32-Lead, Small Outline Package |
| QFN32 | 32-Lead, Quad Flat No lead |

7.1 SO24



| | MM | | INCH | |
|----------|-------|-------|------|------|
| A | 2.35 | 2.65 | .093 | .104 |
| A1 | 0.10 | 0.30 | .004 | .012 |
| B | 0.35 | 0.49 | .014 | .019 |
| C | 0.23 | 0.32 | .009 | .013 |
| D | 15.20 | 15.60 | .599 | .614 |
| E | 7.40 | 7.60 | .291 | .299 |
| e | 1.27 | BSC | .050 | BSC |
| H | 10.00 | 10.65 | .394 | .419 |
| h | 0.25 | 0.75 | .010 | .029 |
| L | 0.40 | 1.27 | .016 | .050 |
| N | 24 | | 24 | |
| α | 0° | | 8° | |

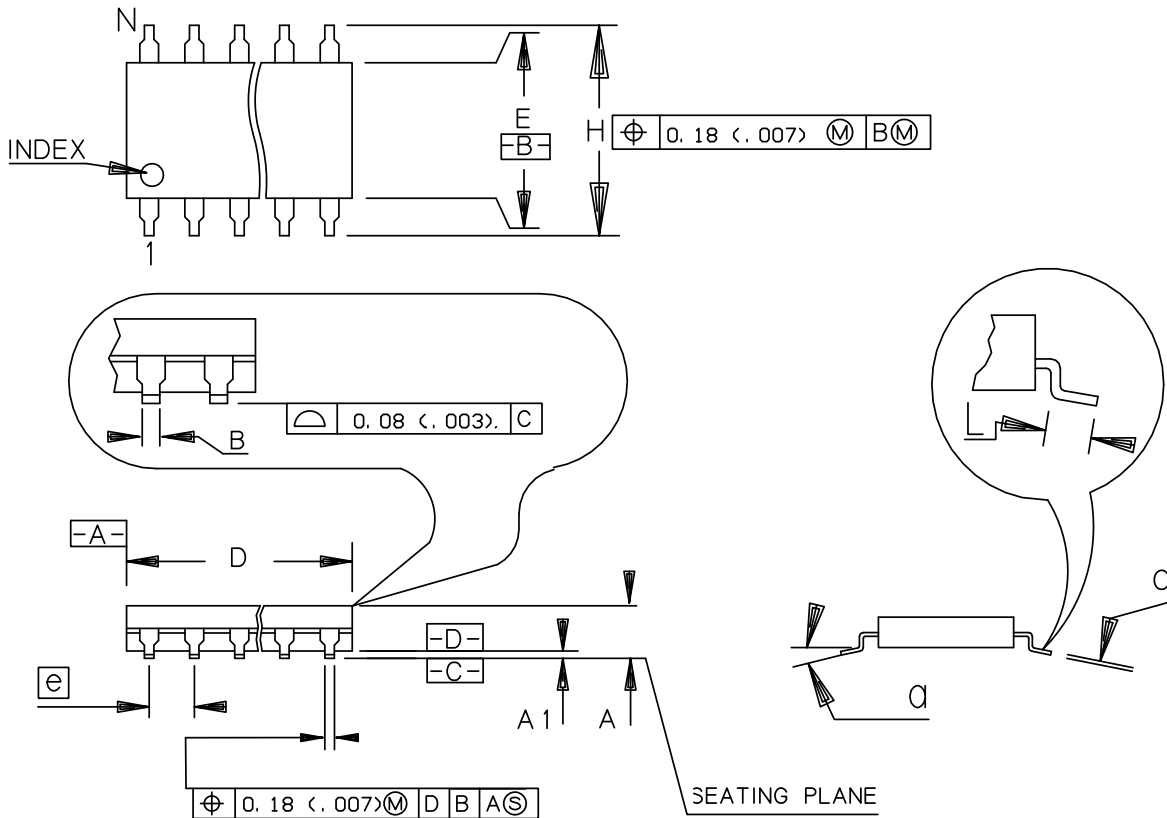
07/27/07

Atmel Atmel Nantes S.A.
La Chantrerie - BP 70602
44306 Nantes Cedex 3 - France

TITLE
TD, 24 - Lead, 0.300" Body Width
Plastic Gull Wing Small Outline Package (SOIC)


| | |
|--------------------------|------------------|
| DRAWING No. TD | REV. A |
|--------------------------|------------------|

7.2 SO32

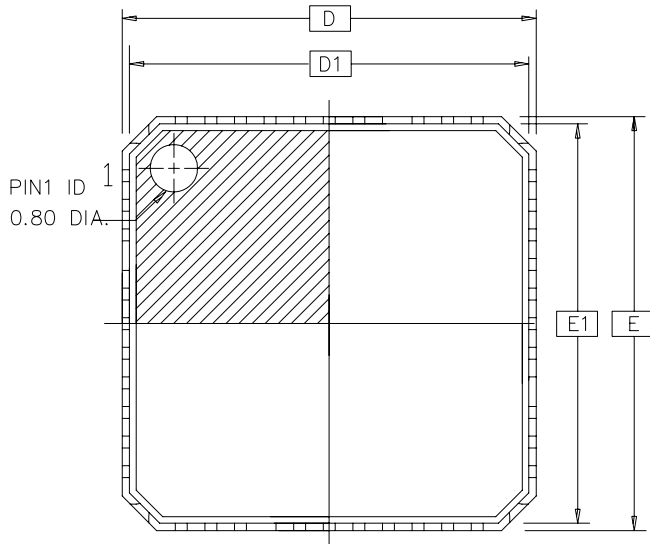


| | MM | | INCH | |
|----------|-------|-------|------|------|
| | Min | Max | Min | Max |
| A | 2.29 | 2.54 | .090 | .100 |
| A1 | 0.10 | 0.25 | .004 | .010 |
| B | 0.36 | 0.51 | .014 | .020 |
| C | 0.15 | 0.32 | .006 | .013 |
| D | 20.57 | 20.88 | .810 | .822 |
| E | 7.42 | 7.60 | .292 | .299 |
| e | 1.27 | BSC | .050 | BSC |
| H | 10.29 | 10.64 | .405 | .419 |
| L | 0.53 | 1.04 | .021 | .041 |
| N | 32 | | 32 | |
| α | 4° | | 4° | |

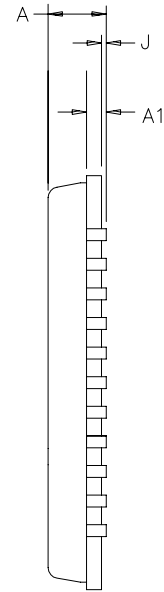
07/27/07

| | | | |
|--|--|--------------------|-------------|
|  Atmel Nantes S.A. La Chantrerie - BP 70602 44306 Nantes Cedex 3 - France | TITLE T4, 32 - Lead, 0.300" Body Width Plastic Gull Wing Small Outline Package (SOIC) | DRAWING No. | REV. |
| | | T4 | A |

7.3 QFN32

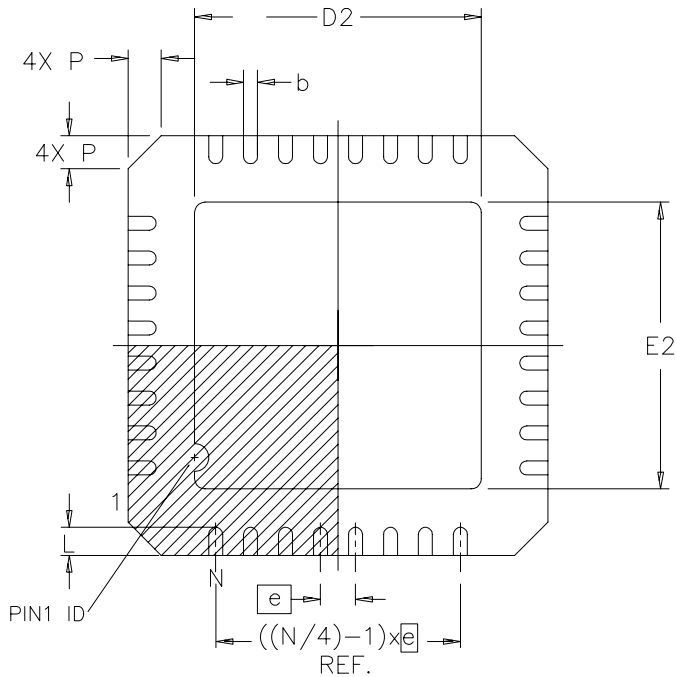


TOP VIEW



SIDE VIEW

DRAWINGS NOT SCALED



BOTTOM VIEW

| | MM | | | INCH | | |
|-------|----------|------|------|----------|------|------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.80 | - | 1.00 | .032 | - | .040 |
| J | 0.00 | 0.01 | 0.05 | .000 | .000 | .002 |
| A1 | 0.20 ref | | | .008 ref | | |
| D/E | 7.00 BSC | | | .276 BSC | | |
| D1/E1 | 6.75 BSC | | | .266 BSC | | |
| D2/E2 | 2.25 | - | 5.25 | .090 | - | .207 |
| N | 32 | | | | | |
| P | 0.24 | 0.42 | 0.60 | .009 | .016 | .024 |
| e | 0.65 BSC | | | .026 BSC | | |
| L | 0.35 | - | 0.75 | .014 | - | .030 |
| b | 0.23 | - | 0.35 | .009 | - | .014 |

Compliant JEDEC Standard MO-220 variation VKKC

NOTES: MLF PACKAGE FAMILY

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM(.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
- 3 DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED
BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
- 4 PACKAGE WARPAGE MAX 0.08mm.
- 5 THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE
PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
- 6 EXACT SHAPE AND SIZE OF THIS FIXTURE IS OPTIONAL

8. Errata AT90PWM216/316

8.1 Revision C

- DAC Driver linearity above 3.6V

1. DAC Driver linearity above 3.6V

With 5V V_{CC} , the DAC driver linearity is poor when DAC output level is above $V_{CC}-1V$. At 5V, DAC output for 1023 will be around 5V - 40mV.

Work around:

Use, when $V_{CC}=5V$, V_{REF} below $V_{CC}-1V$

Or, when $V_{REF}=V_{CC}=5V$, do not use codes above 800.

8.2 Revision B

- DAC Driver linearity above 3.6V
- PSC OCRxx Register update according to PLOCK2 usage

1. DAC Driver linearity above 3.6V

With 5V V_{CC} , the DAC driver linearity is poor when DAC output level is above $V_{CC}-1V$. At 5V, DAC output for 1023 will be around 5V - 40mV.

Work around:

Use, when $V_{CC}=5V$, V_{REF} below $V_{CC}-1V$

Or, when $V_{REF}=V_{CC}=5V$, do not use codes above 800.

2. PSC OCRxx Register update according to PLOCK2 usage

If the PSC is clocked from PLL, and if PLOCK2 bit is changed at the same time as PSC end of cycle occurs, and if OCRxx registers contents have been changed, then the updated OCRxx registers contents are not predictable.

The cause is a synchronization issue between two registers in two different clock domains (PLL clock which clocks PSC and CPU clock).

Workaround:

Enable the PSC end of cycle interrupt.

At the beginning of PSC EOC interrupt vector, change PLOCK value (OCRxx registers can be updated outside the interrupt vector).

This process guarantees that UPDATE and PLOCK actions will not occur at the same moment.

8.3 Revision A

- DAC Driver linearity above 3.6V
- PSC OCRxx Register update according to PLOCK2 usage

1. DAC Driver linearity above 3.6V

With 5V V_{CC} , the DAC driver linearity is poor when DAC output level is above $V_{CC}-1V$. At 5V, DAC output for 1023 will be around 5V - 40mV.

Work around:

Use, when $V_{CC}=5V$, V_{REF} below $V_{CC}-1V$

Or, when $V_{REF}=V_{CC}=5V$, do not uses codes above 800.

2. PSC OCRxx Register update according to PLOCK2 usage

If the PSC is clocked from PLL, and if PLOCK2 bit is changed at the same time as PSC end of cycle occurs, and if OCRxx registers contents have been changed, then the updated OCRxx registers contents are not predictable.

The cause is a synchronization issue between two registers in two different clock domains (PLL clock which clocks PSC and CPU clock).

Workaround:

Enable the PSC end of cycle interrupt.

At the beginning of PSC EOC interrupt vector, change PLOCK value (OCRxx registers can be updated outside the interrupt vector).

This process guarantees that UPDATE and PLOCK actions will not occur at the same moment.

9. Datasheet Revision History for AT90PWM216/316

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

9.1 Rev. 7710H – 07/2013

1. Removed “1. History” chapter.
2. Errata:
 - “Revision C” on page 23: Errata added.
 - “Revision B” on page 23: Errata added.
 - “Revision A” on page 24: Errata updated.

9.2 Rev. 7710G – 03/2013

1. Applied the Atmel new brand template that includes new logo and new addresses.
2. Added note to the MLF/QFN package: The Center GND PADDLE has to be connected to GND.
3. Updated the [Figure 2-1 on page 3](#). Pin 18 changed to AGND instead of GND.
4. Updated the [Figure 2-2 on page 4](#). Pin 24 changed to AGND instead of GND.
5. Added note to the MLF/QFN package: The Center GND PADDLE has to be connected to GND.
6. Updated [Figure 5-2 on page 18](#).
7. Updated [Table 6-2 on page 26](#).
8. Updated “MCU Control Register – MCUCR” on page 62. Added link for Bit 4: “[Configuring the Pin](#)” on page 57.
9. Corrected “typos” in “[Overview](#)” on page 122.
10. Updated “[Features](#)” on page 122. Correct feature is: **Abnormality protection function, emergency input to force all outputs to low level.**
11. Updated “[Center Aligned Mode](#)” on page 130. The label PSCn00 and PSCn01 are incorrect and are respectively replaced by PSCn0 and PSCn1.
12. Updated the formula of “The waveform frequency is defined by the following equation” in “[Normal Mode](#)” on page 134.
13. Updated the formula of f_{AVERAGE} in “[Enhanced Mode](#)” on page 135.
14. Updated “[Input Mode Operation](#)” on page 140. Added a link to the [Table 15-6](#).
15. Updated “[PSC Synchronization](#)” on page 151. The correct content: If the PSCn has its PARUNn bit set, then it can start at the same time as PSCn-1.
16. Updated “[PSC 1 Control Register – PCTL1](#)” on page 158. Bit 4 and Bit 3 linked to “[PSC Input Configuration](#)” on page 139.
17. Updated content description of Bit 1 and Bit 3 in “[PSC 2 Synchro and Output Configuration – PSOC2](#)” on page 154.
18. Updated “[Output Compare SA Register – OCRnSAH and OCRnSAL](#)” on page 155 and “[Output Compare RB Register – OCRnRBH and OCRnRBL](#)” on page 155. The registers are R/W and not only W.
- 19.
20. Updated “[Overview](#)” on page 215. Removed “or CLKi/O/2” from the overview description.
21. Updated [Figure 19-1 on page 216](#), “[Analog Comparator Block Diagram\(1\)\(2\)](#)” .

22. Updated [“Analog Comparator Status Register – ACSR” on page 219](#). Added Bit 3 - CLKPLL
23. Updated [“Amplifier” on page 239](#). The correct content: “The ADC starting is done by setting the ADSC (ADC Start conversion) bit in the ADCSRA register”.
24. Updated [Figure 20-15 on page 240](#) and [Figure 20-16 on page 241](#). Changed CKADC to CKADC2.
25. Updated [“PSC Output Behavior During Reset” on page 266](#). If PSCRV fuse equals 0 (programmed), the selected PSC outputs will be forced to high state. If PSCRV fuse equals 1 (unprogrammed), the selected PSC outputs will be forced to low state.
26. Updated [“Electrical Characteristics” on page 283](#). Added [“DAC Characteristics” on page 290](#).
27. Updated the [Table 25-1 on page 285](#). Replaced -40°C - 85°C with -40°C to 105°C
28. Updated [Table 25-5 on page 289](#). Replaced V_{INT} parameter by A_{REF} . Min and Max values updated.

9.3 Rev. 7710F – 09/11

1. Updated [Table 8-1 on page 41](#). Added V_{POR} and V_{CCR} in the table.
2. Updated [Table 8-2 on page 42](#). Added min and max values for 101 and 010.
3. Updated [Table 25-2 on page 286](#). $V_{CC} = 1.8 - 5.5V$ columns removed.

9.4 Rev. 7710E – 08/10

1. Updated [“Port C \(PC7..PC0\)” on page 9](#).
2. Inserted a footnote [“AT90PWM216 device is available in SOIC 24-pin Package and does not have the D2A \(DAC Output\) brought out to I/O pins.” on page 9](#).
3. Updated [“Idle Mode” on page 35](#) by removing the reference to ACD.
4. Updated [“Voltage Reference Enable Signals and Start-up Time” on page 44](#). Removed reference to ACBG.
4. Updated [Table 15-14 on page 157](#); [Table 15-15 on page 158](#) and [Table 15-16 on page 159](#)
5. Removed reference to the ACCKDIV from [“Analog Comparator” on page 215](#) and from [“Register Summary” on page 11](#).
6. Updated [“ADC Prescaler Selection” on page 237](#).
7. Updated [Table 25-5 on page 289](#) with Max and Min value for Internal Voltage Reference
8. Removed AC2SADE bit from [“Register Summary” on page 11](#).

9.5 Rev. 7710D

1. Updated table page 2.
2. Updated [“Absolute Maximum Ratings*” on page 283](#)

9.6 Rev. 7710C

1. Updated table page 2.
2. Updated [Section “Internal Calibrated RC Oscillator Operating Modes\(1\)\(2\)” on page 28.](#)
3. Updated [Section “Features” on page 245.](#)
4. Updated table in [Section “Electrical Characteristics” on page 283.](#)
5. Added section [Section “Calibrated Internal RC Oscillator Accuracy” on page 285.](#)
6. Updated [Table 25-5 on page 289.](#)
7. Updated [Figure 26-36 on page 312.](#)
8. Updated [Figure 26-37 on page 313.](#)
9. Updated [Figure 26-38 on page 313.](#)

9.7 Rev. 7710B

1. Updated “Section “In-System Reprogrammable Flash Program Memory”, page 17
2. Updated [“Figure 5-1 on page 17](#)
3. Updated [“Figure 6-1 on page 26](#)
4. Updated [“Figure 6-7 on page 30](#)
5. Updated [“Table 20-1 on page 227](#)
6. Updated “Section “ADC Noise Canceler”, page 228
7. Updated [“Table 20-6 on page 237](#)
8. Added [“Table 20-7 on page 238](#)
9. Updated “Section “Amplifier”, page 239
10. Updated [“Figure 20-15 on page 240](#)
11. Added [“Figure 20-16 on page 241](#)
12. Updated [“Figure 20-17 on page 242](#)
13. Updated “Section “Amplifier 0 Control and Status register – AMP0CSR”, page 243
14. Updated [“Table 20-9 on page 243](#)
15. Updated “Section “Amplifier 1 Control and Status register – AMP1CSR”, page 244
16. Updated [“Table 20-9 on page 243](#)
17. Updated [“Table 20-11 on page 244](#)
18. Updated [“Table 23-6 on page 263](#)
19. Updated [“Table 23-7 on page 263](#)
20. Updated [“Table 23-8 on page 263](#)
21. Updated “Section “DC Characteristics”, page 284
22. Updated [“Table 25-5 on page 289](#)
23. Updated “Section “Example 1”, page 298
24. Updated “Section “Example 2”, page 298
25. Updated “Section “Example 3”, page 298
26. Added [“Figure 26-22 on page 305](#)
27. Updated “Section “Instruction Set Summary”, page 15
28. Added “Section “Errata AT90PWM216/316”, page 23

9.8 Rev. 7710A

1. Document creation.



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