

## Features

- **Low-voltage and Standard-voltage Operation**
  - 2.7 ( $V_{CC} = 2.7V$  to 5.5V)
  - 1.8 ( $V_{CC} = 1.8V$  to 5.5V)
- **User-selectable Internal Organization**
  - 1K: 128 x 8 or 64 x 16
  - 2K: 256 x 8 or 128 x 16
  - 4K: 512 x 8 or 256 x 16
- **Three-wire Serial Interface**
- **2 MHz Clock Rate (5V)**
- **Self-timed Write Cycle (10 ms max)**
- **High Reliability**
  - **Endurance: 1 Million Write Cycles**
  - **Data Retention: 100 Years**
- **Automotive Grade, Extended Temperature and Lead-Free/Halogen-Free Devices Available**
- **8-lead PDIP, 8-lead JEDEC SOIC, 8-lead EIAJ SOIC, 8-lead MAP, 8-lead TSSOP, and 8-ball dBGA2 Packages**

## Description

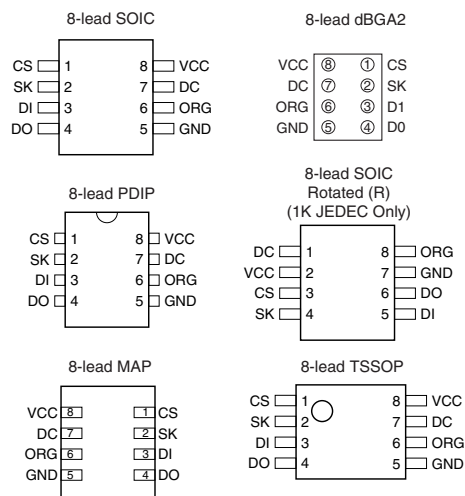
The AT93C46/56/66 provides 1024/2048/4096 bits of serial electrically erasable programmable read-only memory (EEPROM), organized as 64/128/256 words of 16 bits each (when the ORG pin is connected to VCC), and 128/256/512 words of 8 bits each (when the ORG pin is tied to ground). The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operations are essential. The AT93C46/56/66 is available in space-saving 8-lead PDIP, 8-lead JEDEC SOIC, 8-lead EIAJ SOIC, 8-lead MAP, 8-lead TSSOP, and 8-lead dBGA2 packages.

The AT93C46/56/66 is enabled through the Chip Select pin (CS) and accessed via a three-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SK). Upon receiving a Read instruction at DI, the address is decoded and the data is clocked out serially on the DO pin. The Write cycle is completely self-timed, and no separate Erase cycle is required before Write. The Write cycle is only enabled when the part is in the Erase/Write Enable state. When CS is brought high following the initiation of a Write cycle, the DO pin outputs the Ready/Busy status of the part.

The AT93C46/56/66 is available in 2.7V to 5.5V and 1.8V to 5.5V versions.

**Table 1.** Pin Configurations

Pin Name	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
VCC	Power Supply
ORG	Internal Organization
DC	Don't Connect



## Three-wire Serial EEPROMs

1K (128 x 8 or 64 x 16)

2K (256 x 8 or 128 x 16)

4K (512 x 8 or 256 x 16)

## AT93C46 AT93C56<sup>(1)</sup> AT93C66<sup>(2)</sup>

- Note: 1. This device is not recommended for new designs. Please refer to AT93C56A.
2. This device is not recommended for new designs. Please refer to AT93C66A.

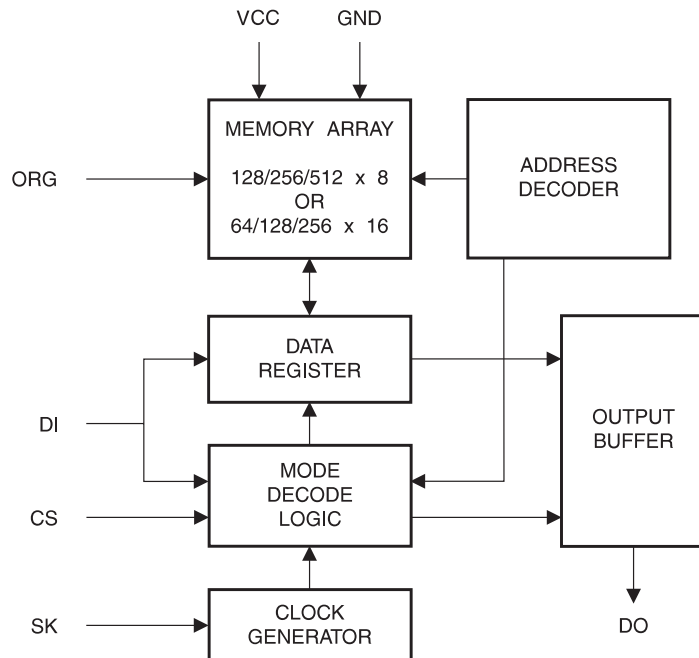


## Absolute Maximum Ratings\*

Operating Temperature .....	-55°C to +125°C
Storage Temperature .....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground .....	-1.0V to +7.0V
Maximum Operating Voltage .....	6.25V
DC Output Current.....	5.0 mA

\*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Figure 1. Block Diagram



Note: When the ORG pin is connected to VCC, the “x 16” organization is selected. When it is connected to ground, the “x 8” organization is selected. If the ORG pin is left unconnected and the application does not load the input beyond the capability of the internal 1 Meg ohm pullup, then the “x 16” organization is selected. The feature is not available on the 1.8V devices.

For the AT93C46, if “x 16” organization is the mode of choice and Pin 6 (ORG) is left unconnected, Atmel recommends using the AT93C46A device. For more details, see the AT93C46A datasheet.

**Table 2.** Pin Capacitance<sup>(1)</sup>

Applicable over recommended operating range from  $T_A = 25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$ ,  $V_{CC} = +5.0\text{V}$  (unless otherwise noted)

Symbol	Test Conditions	Max	Units	Conditions
$C_{OUT}$	Output Capacitance (DO)	5	pF	$V_{OUT} = 0\text{V}$
$C_{IN}$	Input Capacitance (CS, SK, DI)	5	pF	$V_{IN} = 0\text{V}$

Note: 1. This parameter is characterized and is not 100% tested.

**Table 3.** DC Characteristics

Applicable over recommended operating range from:  $T_{AI} = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = +1.8\text{V}$  to  $+5.5\text{V}$ ,  
 $T_{AE} = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = +1.8\text{V}$  to  $+5.5\text{V}$  (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
$V_{CC1}$	Supply Voltage			1.8		5.5	V
$V_{CC2}$	Supply Voltage			2.7		5.5	V
$V_{CC3}$	Supply Voltage			4.5		5.5	V
$I_{CC}$	Supply Current	$V_{CC} = 5.0\text{V}$	READ at 1.0 MHz		0.5	2.0	mA
			WRITE at 1.0 MHz		0.5	2.0	mA
$I_{SB1}$	Standby Current	$V_{CC} = 1.8\text{V}$	CS = 0V		0	0.1	$\mu\text{A}$
$I_{SB2}$	Standby Current	$V_{CC} = 2.7\text{V}$	CS = 0V		6.0	10.0	$\mu\text{A}$
$I_{SB3}$	Standby Current	$V_{CC} = 5.0\text{V}$	CS = 0V		17	30	$\mu\text{A}$
$I_{IL}$	Input Leakage	$V_{IN} = 0\text{V}$ to $V_{CC}$			0.1	1.0	$\mu\text{A}$
$I_{OL}$	Output Leakage	$V_{IN} = 0\text{V}$ to $V_{CC}$			0.1	1.0	$\mu\text{A}$
$V_{IL1}^{(1)}$	Input Low Voltage	$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$		-0.6		0.8	V
$V_{IH1}^{(1)}$	Input High Voltage			2.0		$V_{CC} + 1$	
$V_{IL2}^{(1)}$	Input Low Voltage	$1.8\text{V} \leq V_{CC} \leq 2.7\text{V}$		-0.6		$V_{CC} \times 0.3$	V
$V_{IH2}^{(1)}$	Input High Voltage			$V_{CC} \times 0.7$		$V_{CC} + 1$	
$V_{OL1}$	Output Low Voltage	$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	$I_{OL} = 2.1\text{ mA}$			0.4	V
$V_{OH1}$	Output High Voltage		$I_{OH} = -0.4\text{ mA}$	2.4			V
$V_{OL2}$	Output Low Voltage	$1.8\text{V} \leq V_{CC} \leq 2.7\text{V}$	$I_{OL} = 0.15\text{ mA}$			0.2	V
$V_{OH2}$	Output High Voltage		$I_{OH} = -100\ \mu\text{A}$	$V_{CC} - 0.2$			V

Note: 1.  $V_{IL}$  min and  $V_{IH}$  max are reference only and are not tested.

**Table 4. AC Characteristics**

Applicable over recommended operating range from  $T_{AI} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = \text{As Specified}$ ,  
 $CL = 1$  TTL Gate and  $100\text{ pF}$  (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
$f_{SK}$	SK Clock Frequency	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$	0 0 0		2 1 0.25	MHz
$t_{SKH}$	SK High Time	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$	250 250 1000			ns
$t_{SKL}$	SK Low Time	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$	250 250 1000			ns
$t_{CS}$	Minimum CS Low Time	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$	250 250 1000			ns
$t_{CSS}$	CS Setup Time	Relative to SK $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$	50 50 200			ns
$t_{DIS}$	DI Setup Time	Relative to SK $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$	100 100 400			ns
$t_{CSH}$	CS Hold Time	Relative to SK	0			ns
$t_{DIH}$	DI Hold Time	Relative to SK $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$	100 100 400			ns
$t_{PD1}$	Output Delay to "1"	AC Test $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$			250 250 1000	ns
$t_{PD0}$	Output Delay to "0"	AC Test $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$			250 250 1000	ns
$t_{SV}$	CS to Status Valid	AC Test $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$			250 250 1000	ns
$t_{DF}$	CS to DO in High Impedance	AC Test CS = $V_{IL}$ $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ $1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$			100 100 400	ns
$t_{WP}$	Write Cycle Time				10	ms
		$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	0.1	3		ms
Endurance <sup>(1)</sup>	5.0V, 25°C		1M			Write Cycles

Note: 1. This parameter is characterized and is not 100% tested.

**Table 5.** Instruction Set for the AT93C46

Instruction	SB	Op Code	Address		Data		Comments
			x 8	x 16	x 8	x 16	
READ	1	10	$A_6 - A_0$	$A_5 - A_0$			Reads data stored in memory, at specified address
EWEN	1	00	11XXXXXX	11XXXX			Write enable must precede all programming modes
ERASE	1	11	$A_6 - A_0$	$A_5 - A_0$			Erases memory location $A_n - A_0$
WRITE	1	01	$A_6 - A_0$	$A_5 - A_0$	$D_7 - D_0$	$D_{15} - D_0$	Writes memory location $A_n - A_0$
ERAL	1	00	10XXXXXX	10XXXX			Erases all memory locations. Valid only at $V_{CC} = 4.5V$ to $5.5V$
WRAL	1	00	01XXXXXX	01XXXX	$D_7 - D_0$	$D_{15} - D_0$	Writes all memory locations. Valid only at $V_{CC} = 4.5V$ to $5.5V$
EWDS	1	00	00XXXXXX	00XXXX			Disables all programming instructions

Note: The Xs in the address field represent *DON'T CARE* values and must be clocked.

**Table 6.** Instruction Set for the AT93C56<sup>(1)</sup> and AT93C66<sup>(2)</sup>

Instruction	SB	Op Code	Address		Data		Comments
			x 8	x 16	x 8	x 16	
READ	1	10	$A_8 - A_0$	$A_7 - A_0$			Reads data stored in memory, at specified address
EWEN	1	00	11XXXXXXXX	11XXXXXXXX			Write enable must precede all programming modes
ERASE	1	11	$A_8 - A_0$	$A_7 - A_0$			Erases memory location $A_n - A_0$
WRITE	1	01	$A_8 - A_0$	$A_7 - A_0$	$D_7 - D_0$	$D_{15} - D_0$	Writes memory location $A_n - A_0$
ERAL	1	00	10XXXXXXXX	10XXXXXXXX			Erases all memory locations. Valid only at $V_{CC} = 4.5V$ to $5.5V$
WRAL	1	00	01XXXXXXXX	01XXXXXXXX	$D_7 - D_0$	$D_{15} - D_0$	Writes all memory locations. Valid only at $V_{CC} = 5.0V \pm 10\%$ and Disable Register cleared
EWDS	1	00	00XXXXXXXX	00XXXXXXXX			Disables all programming instructions

Notes: 1. This device is not recommended for new designs. Please refer to AT93C56A.

2. This device is not recommended for new designs. Please refer to AT93C66A.

## Functional Description

The AT93C46/56/66 is accessed via a simple and versatile three-wire serial communication interface. Device operation is controlled by seven instructions issued by the host processor. *A valid instruction starts with a rising edge of CS and consists of a start bit (logic “1”) followed by the appropriate op code and the desired memory address location.*

**READ (READ):** The Read (READ) instruction contains the address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock SK. It should be noted that a dummy bit (logic “0”) precedes the 8- or 16-bit data output string.

**ERASE/WRITE ENABLE (EWEN):** To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the EWEN state, programming remains enabled until an EWDS instruction is executed or  $V_{CC}$  power is removed from the part.

**ERASE (ERASE):** The Erase (ERASE) instruction programs all bits in the specified memory location to the logical “1” state. The self-timed erase cycle starts once the Erase instruction and address are decoded. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns ( $t_{CS}$ ). A logic “1” at pin DO indicates that the selected memory location has been erased and the part is ready for another instruction.

**WRITE (WRITE):** The Write (WRITE) instruction contains the 8 or 16 bits of data to be written into the specified memory location. The self-timed programming cycle  $t_{WP}$  starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the Read/Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns ( $t_{CS}$ ). A logic “0” at DO indicates that programming is still in progress. A logic “1” indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions. *A Ready/Busy status cannot be obtained if the CS is brought high after the end of the self-timed programming cycle  $t_{WP}$ .*

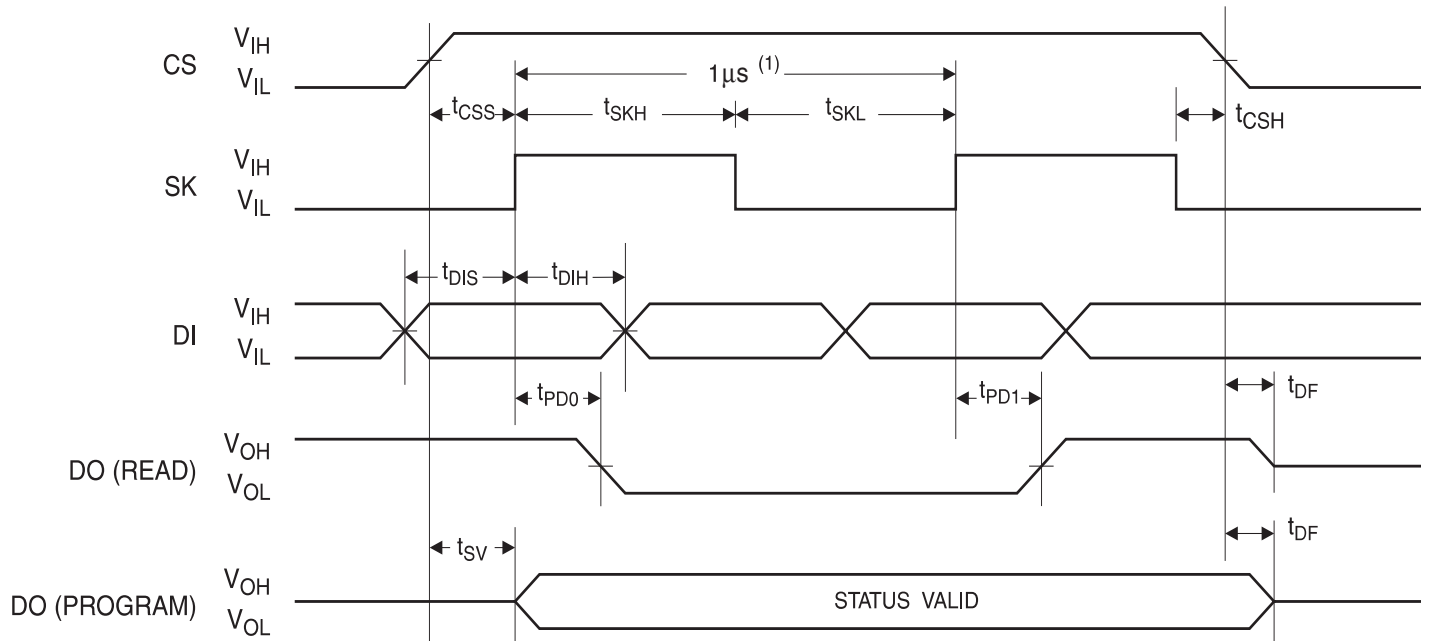
**ERASE ALL (ERAL):** The Erase All (ERAL) instruction programs every bit in the memory array to the logic “1” state and is primarily used for testing purposes. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns ( $t_{CS}$ ). The ERAL instruction is valid only at  $V_{CC} = 5.0V \pm 10\%$ .

**WRITE ALL (WRAL):** The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns ( $t_{CS}$ ). The WRAL instruction is valid only at  $V_{CC} = 5.0V \pm 10\%$ .

**ERASE/WRITE DISABLE (EWDS):** To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the Read instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

## Timing Diagrams

Figure 2. Synchronous Data Timing



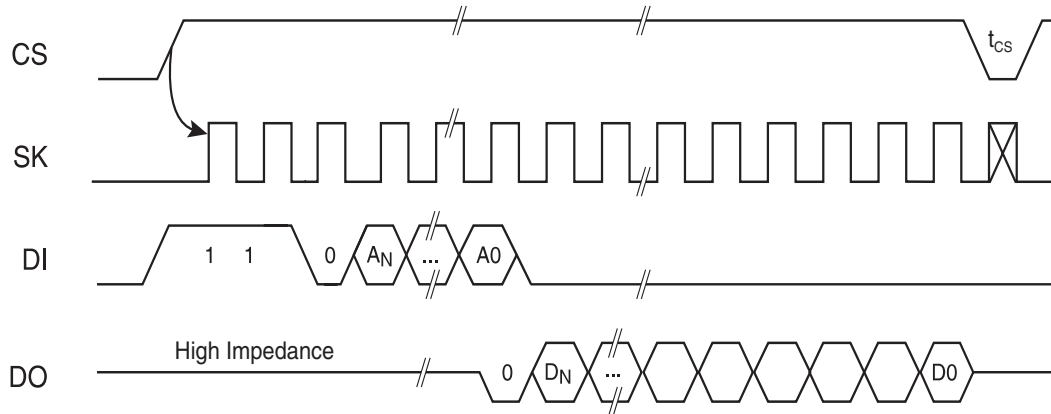
Note: 1. This is the minimum SK period.

Table 7. Organization Key for Timing Diagrams

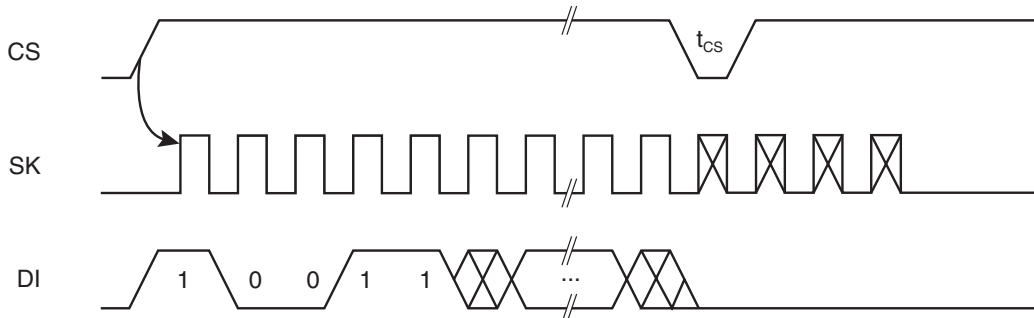
I/O	AT93C46 (1K)		AT93C56 (2K) <sup>(1)</sup>		AT93C66 (4K) <sup>(2)</sup>	
	x 8	x 16	x 8	x 16	x 8	x 16
A <sub>N</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>8</sub> <sup>(3)</sup>	A <sub>7</sub> <sup>(4)</sup>	A <sub>8</sub>	A <sub>7</sub>
D <sub>N</sub>	D <sub>7</sub>	D <sub>15</sub>	D <sub>7</sub>	D <sub>15</sub>	D <sub>7</sub>	D <sub>15</sub>

- Notes:
1. This device is not recommended for new designs. Please refer to AT93C56A.
  2. This device is not recommended for new designs. Please refer to AT93C66A.
  3. A<sub>8</sub> is a *don't care* value, but the extra clock is required.
  4. A<sub>7</sub> is a *don't care* value, but the extra clock is required.

**Figure 3. READ Timing**



**Figure 4. EWEN Timing**



**Figure 5. EWDS Timing**

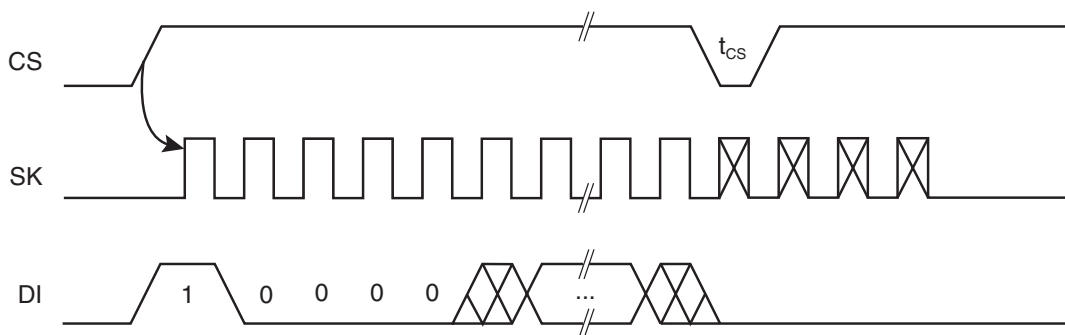




Figure 6. WRITE Timing

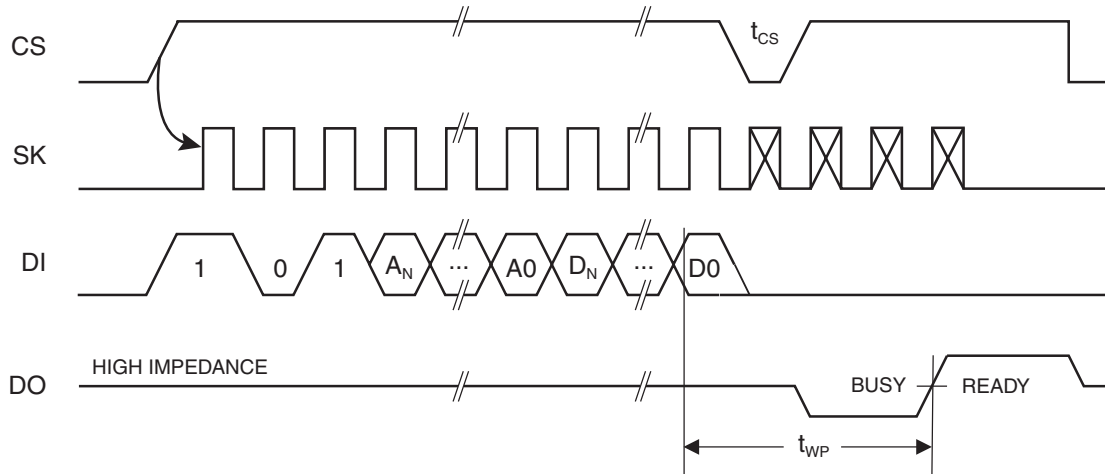
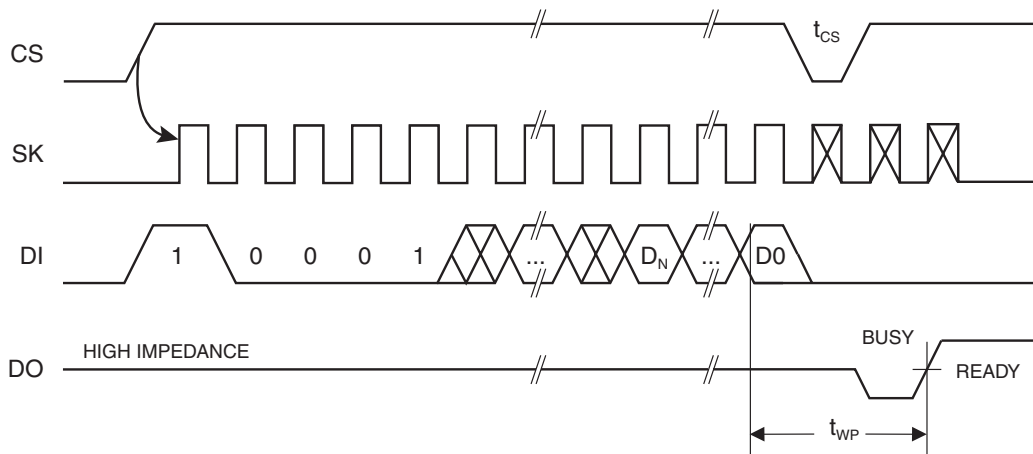
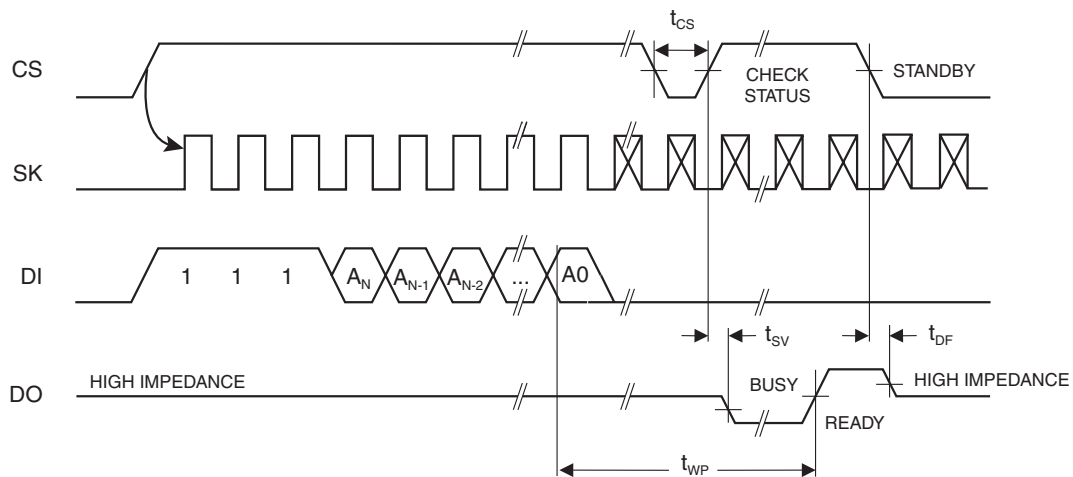


Figure 7. WRAL Timing<sup>(1)</sup>

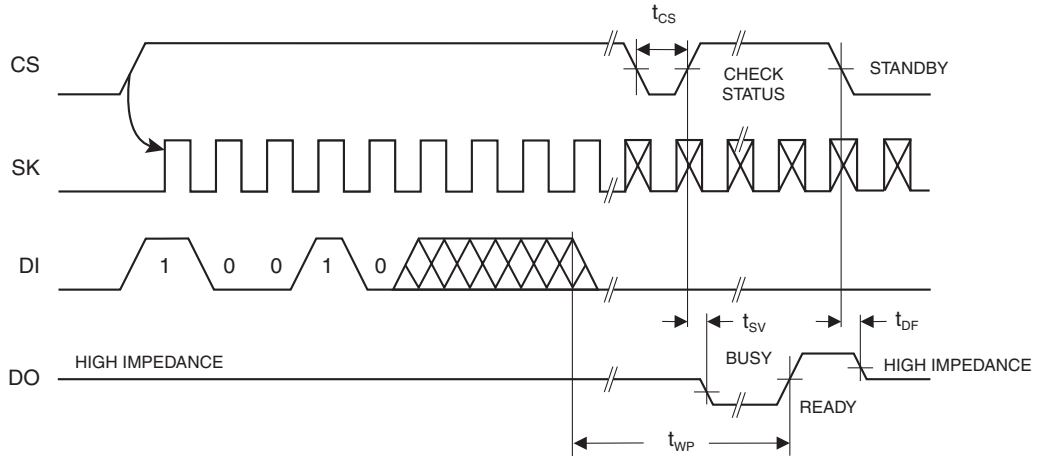


Note: 1. Valid only at  $V_{CC} = 4.5V$  to  $5.5V$ .

Figure 8. ERASE Timing



**Figure 9. ERAL Timing<sup>(1)</sup>**



Note: 1. Valid only at  $V_{CC} = 4.5V$  to  $5.5V$ .

## AT93C46 Ordering Information<sup>(1)</sup>

Ordering Code	Package	Operation Range
AT93C46-10PI-2.7 AT93C46-10SI-2.7 AT93C46R-10SI-2.7 AT93C46W-10SI-2.7 AT93C46-10TI-2.7	8P3 8S1 8S1 8S2 8A2	Industrial (-40°C to 85°C)
AT93C46-10PI-1.8 AT93C46-10SI-1.8 AT93C46R-10SI-1.8 AT93C46W-10SI-1.8 AT93C46-10TI-1.8	8P3 8S1 8S1 8S2 8A2	Industrial (-40°C to 85°C)
AT93C46-10PU-2.7 AT93C46-10PU-1.8 AT93C46-10SU-2.7 AT93C46-10SU-1.8 AT93C46W-10SU-2.7 AT93C46W-10SU-1.8 AT93C46-10TU-2.7 AT93C46-10TU-1.8 AT93C46Y1-10YU-2.7 AT93C46Y1-10YU-1.8 AT93C46Y5-10YU-2.7 AT93C46Y5-10YU-1.8 AT93C46U3-10UU-2.7 AT93C46U3-10UU-1.8	8P3 8P3 8S1 8S1 8S2 8S2 8A2 8A2 8Y1 8Y1 8Y5 8Y5 8U3-1 8U3-1	Lead-free/Halogen-free/ Industrial Temperature (-40°C to 85°C)
AT93C46-W2.7-11 <sup>(2)</sup> AT93C46-W1.8-11 <sup>(2)</sup>	Die Sale Die Sale	Industrial (-40°C to 85°C)

- Notes: 1. For 2.7V devices used in the 4.5V to 5.5V range, please refer to performance values in the Table 3 on page 3 and Table 4 on page 4.  
2. Available in waffle pack and wafer form, order as SL719 for wafer form. Bumped die available upon request.

Package Type	
<b>8P3</b>	8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
<b>8S1</b>	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
<b>8S2</b>	8-lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
<b>8A2</b>	8-lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
<b>8U3-1</b>	8-ball, Die Ball Grid Array Package (dBGAA2)
<b>8Y1</b>	8-lead, 4.90 mm x 3.00 mm Body, Dual Footprint, Non-leaded, Miniature Array Package (MAP)
<b>8Y5</b>	8-lead, 2.00 mm x 3.00 mm Body, Dual Footprint, Non-leaded, Miniature Array Package (MAP)
Options	
<b>-2.7</b>	Low Voltage (2.7V to 5.5V)
<b>-1.8</b>	Low Voltage (1.8V to 5.5V)
<b>R</b>	Rotated Pinout



## AT93C56<sup>(1)</sup> Ordering Information

Ordering Code <sup>(2)</sup>	Package	Operation Range
AT93C56-10PI-2.7	8P3	Industrial (-40°C to 85°C)
AT93C56-10SI-2.7	8S1	
AT93C56W-10SI-2.7	8S2	
AT93C56-10TI-2.7	8A2	
AT93C56Y1-10YI-2.7	8Y1	
AT93C56-10PI-1.8	8P3	Industrial (-40°C to 85°C)
AT93C56-10SI-1.8	8S1	
AT93C56W-10SI-1.8	8S2	
AT93C56-10TI-1.8	8A2	
AT93C56Y1-10YI-1.8	8Y1	

- Notes: 1. This device is not recommended for new designs. Please refer to AT93C56A.  
 2. For 2.7V devices used in the 4.5V to 5.5V range, please refer to performance values in Table 3 on page 3 and Table 4 on page 4.

Package Type	
<b>8P3</b>	8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
<b>8S1</b>	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
<b>8S2</b>	8-lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
<b>8A2</b>	8-lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
<b>8Y1</b>	8-lead, 4.90 mm x 3.00 mm Body, Dual Footprint, Non-leaded, Miniature Array Package (MAP)
Options	
<b>-2.7</b>	Low Voltage (2.7V to 5.5V)
<b>1.8</b>	Low Voltage (1.8V to 5.5V)

## AT93C66<sup>(1)</sup> Ordering Information

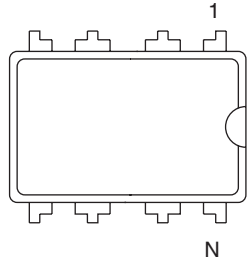
Ordering Code <sup>(2)</sup>	Package	Operation Range
AT93C66-10PI-2.7	8P3	Industrial (-40°C to 85°C)
AT93C66-10SI-2.7	8S1	
AT93C66W-10SI-2.7	8S2	
AT93C66-10TI-2.7	8A2	
AT93C66Y1-10YI-2.7	8Y1	
AT93C66-10PI-1.8	8P3	Industrial (-40°C to 85°C)
AT93C66-10SI-1.8	8S1	
AT93C66W-10SI-1.8	8S2	
AT93C66-10TI-1.8	8A2	
AT93C66Y1-10YI-1.8	8Y1	

- Notes:
1. This device is not recommended for new designs. Please refer to AT93C66A.
  2. For 2.7V devices used in the 4.5V to 5.5V range, please refer to performance values in Table 3 on page 3 and Table 4 on page 4.

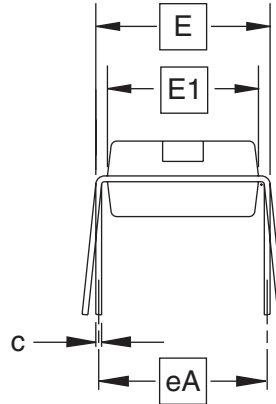
Package Type	
<b>8P3</b>	8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
<b>8S1</b>	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
<b>8S2</b>	8-lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
<b>8A2</b>	8-lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
<b>8Y1</b>	8-lead, 4.90 mm x 3.00 mm Body, Dual Footprint, Non-leaded, Miniature Array Package (MAP)
Options	
<b>-2.7</b>	Low Voltage (2.7V to 5.5V)
<b>-1.8</b>	Low Voltage (1.8V to 5.5V)

# Packaging Information

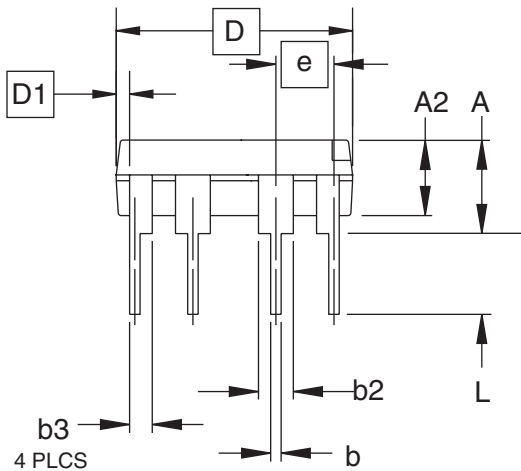
## 8P3 – PDIP



Top View



End View



Side View

**COMMON DIMENSIONS**  
(Unit of Measure = inches)

SYMBOL	MIN	NOM	MAX	NOTE
A			0.210	2
A2	0.115	0.130	0.195	
b	0.014	0.018	0.022	5
b2	0.045	0.060	0.070	6
b3	0.030	0.039	0.045	6
c	0.008	0.010	0.014	
D	0.355	0.365	0.400	3
D1	0.005			3
E	0.300	0.310	0.325	4
E1	0.240	0.250	0.280	3
e	0.100 BSC			
eA	0.300 BSC			4
L	0.115	0.130	0.150	2

- Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA for additional information.
  2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
  3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
  4. E and eA measured with the leads constrained to be perpendicular to datum.
  5. Pointed or rounded lead tips are preferred to ease insertion.
  6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

01/09/02



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**TITLE**

**8P3**, 8-lead, 0.300" Wide Body, Plastic Dual  
In-line Package (PDIP)

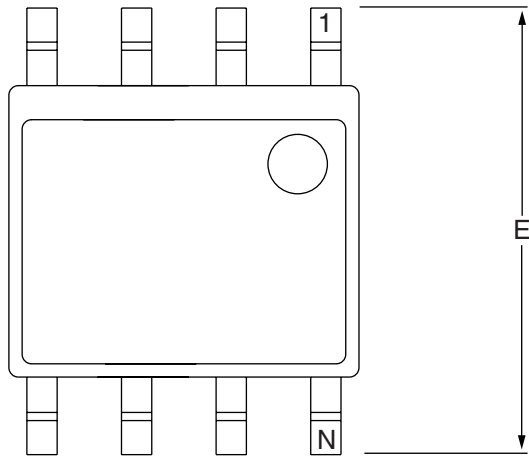
**DRAWING NO.**

8P3

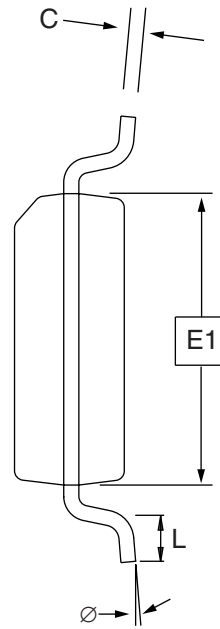
**REV.**

B

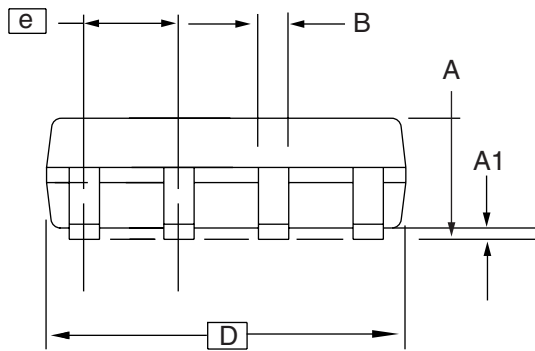
8S1 – JEDEC SOIC



Top View



End View



Side View

COMMON DIMENSIONS  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.00	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
∅	0°	–	8°	

Note: These drawings are for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.

10/7/03



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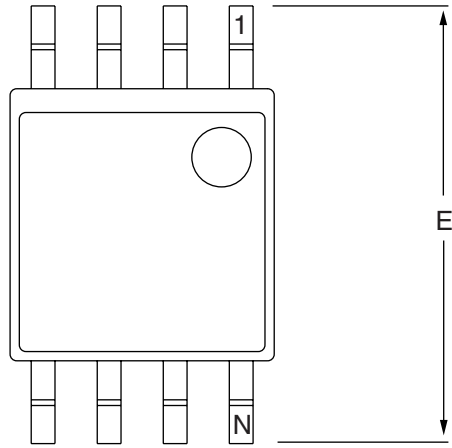
**TITLE**  
8S1, 8-lead (0.150" Wide Body), Plastic Gull Wing  
Small Outline (JEDEC SOIC)

**DRAWING NO.**  
8S1

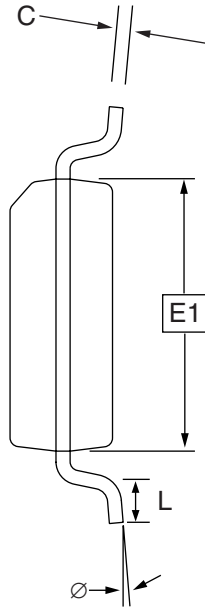
**REV.**  
B



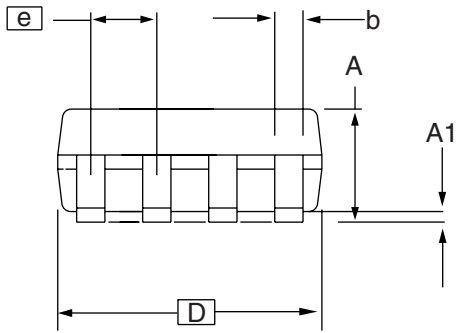
# 8S2 – EIAJ SOIC



Top View



End View



Side View

### COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.70		2.16	
A1	0.05		0.25	
b	0.35		0.48	5
C	0.15		0.35	5
D	5.13		5.35	
E1	5.18		5.40	2, 3
E	7.70		8.26	
L	0.51		0.85	
Ø	0°		8°	
e	1.27 BSC			4

- Notes: 1. This drawing is for general information only; refer to EIAJ Drawing EDR-7320 for additional information.  
 2. Mismatch of the upper and lower dies and resin burrs are not included.  
 3. It is recommended that upper and lower cavities be equal. If they are different, the larger dimension shall be regarded.  
 4. Determines the true geometric position.  
 5. Values b and C apply to pb/Sn solder plated terminal. The standard thickness of the solder layer shall be 0.010 +0.010/-0.005 mm.

10/7/03



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**TITLE**  
8S2, 8-lead, 0.209" Body, Plastic Small  
Outline Package (EIAJ)

**DRAWING NO.**  
8S2

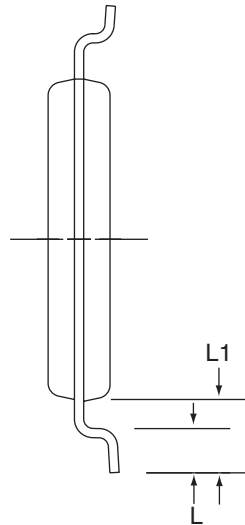
**REV.**  
C



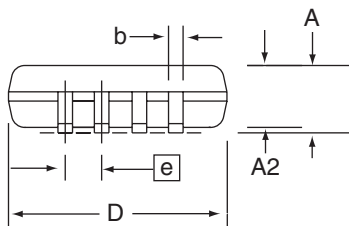
8A2 – TSSOP



Top View



End View



Side View

**COMMON DIMENSIONS**  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
D	2.90	3.00	3.10	2, 5
E	6.40 BSC			
E1	4.30	4.40	4.50	3, 5
A	-	-	1.20	
A2	0.80	1.00	1.05	
b	0.19	-	0.30	4
e	0.65 BSC			
L	0.45	0.60	0.75	
L1	1.00 REF			

- Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
  2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
  3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010 in) per side.
  4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
  5. Dimension D and E1 to be determined at Datum Plane H.

5/30/02



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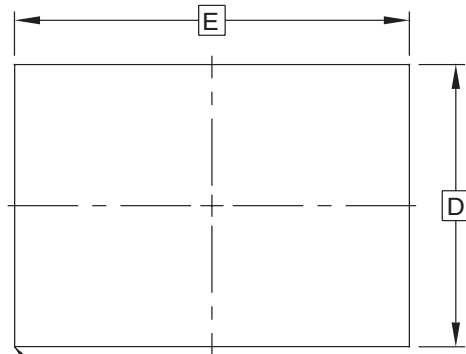
**TITLE**  
**8A2**, 8-lead, 4.4 mm Body, Plastic  
Thin Shrink Small Outline Package (TSSOP)

**DRAWING NO.**  
8A2

**REV.**  
B

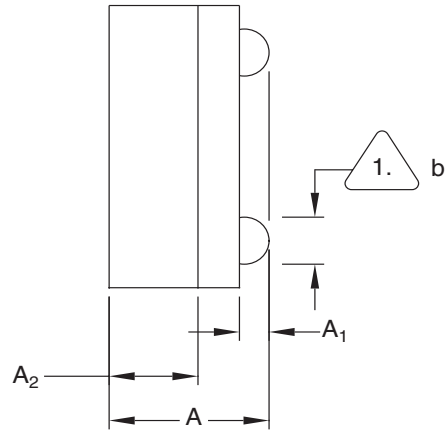


# 8U3-1 – dBGA2

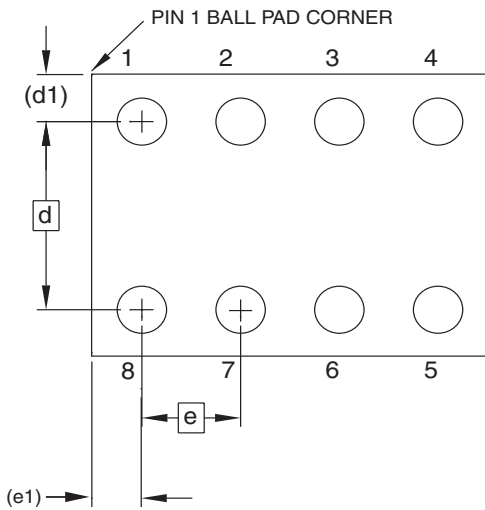


PIN 1 BALL PAD CORNER

Top View



Side View



Bottom View  
8 SOLDER BALLS

1. Dimension "b" is measured at the maximum solder ball diameter.

This drawing is for general information only.

**COMMON DIMENSIONS**  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.71	0.81	0.91	
A1	0.10	0.15	0.20	
A2	0.40	0.45	0.50	
b	0.20	0.25	0.30	
D	1.50 BSC			
E	2.00 BSC			
e	0.50 BSC			
e1	0.25 REF			
d	1.00 BSC			
d1	0.25 REF			

6/24/03



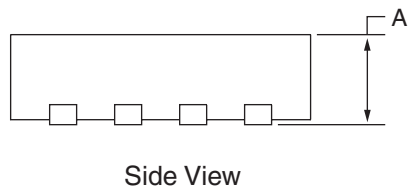
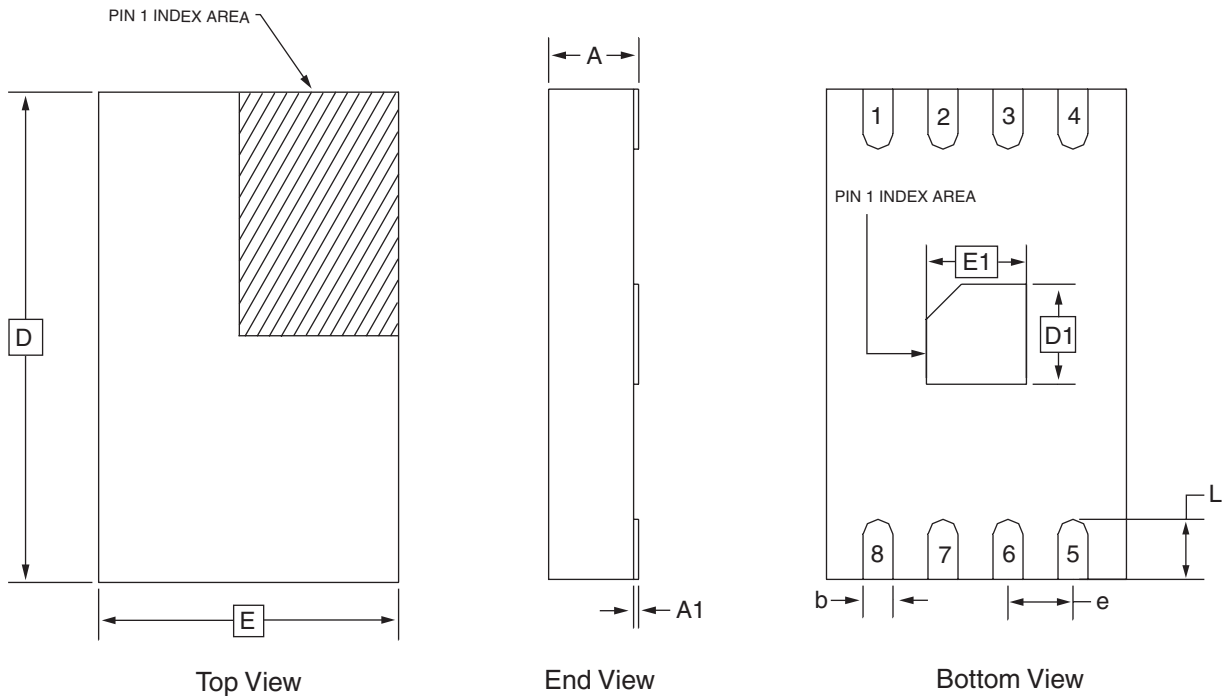
1150 E. Cheyenne Mtn. Blvd.  
Colorado Springs, CO 80906

**TITLE**  
8U3-1, 8-ball, 1.50 x 2.00 mm Body, 0.50 mm pitch,  
Small Die Ball Grid Array Package (dBGA2)

**DRAWING NO.**  
PO8U3-1

**REV.**  
A

8Y1 – MAP



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	0.90	
A1	0.00	-	0.05	
D	4.70	4.90	5.10	
E	2.80	3.00	3.20	
D1	0.85	1.00	1.15	
E1	0.85	1.00	1.15	
b	0.25	0.30	0.35	
e	0.65 TYP			
L	0.50	0.60	0.70	

2/28/03



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**TITLE**

**8Y1, 8-lead (4.90 x 3.00 mm Body) MSOP Array Package (MAP) Y1**

**DRAWING NO.**

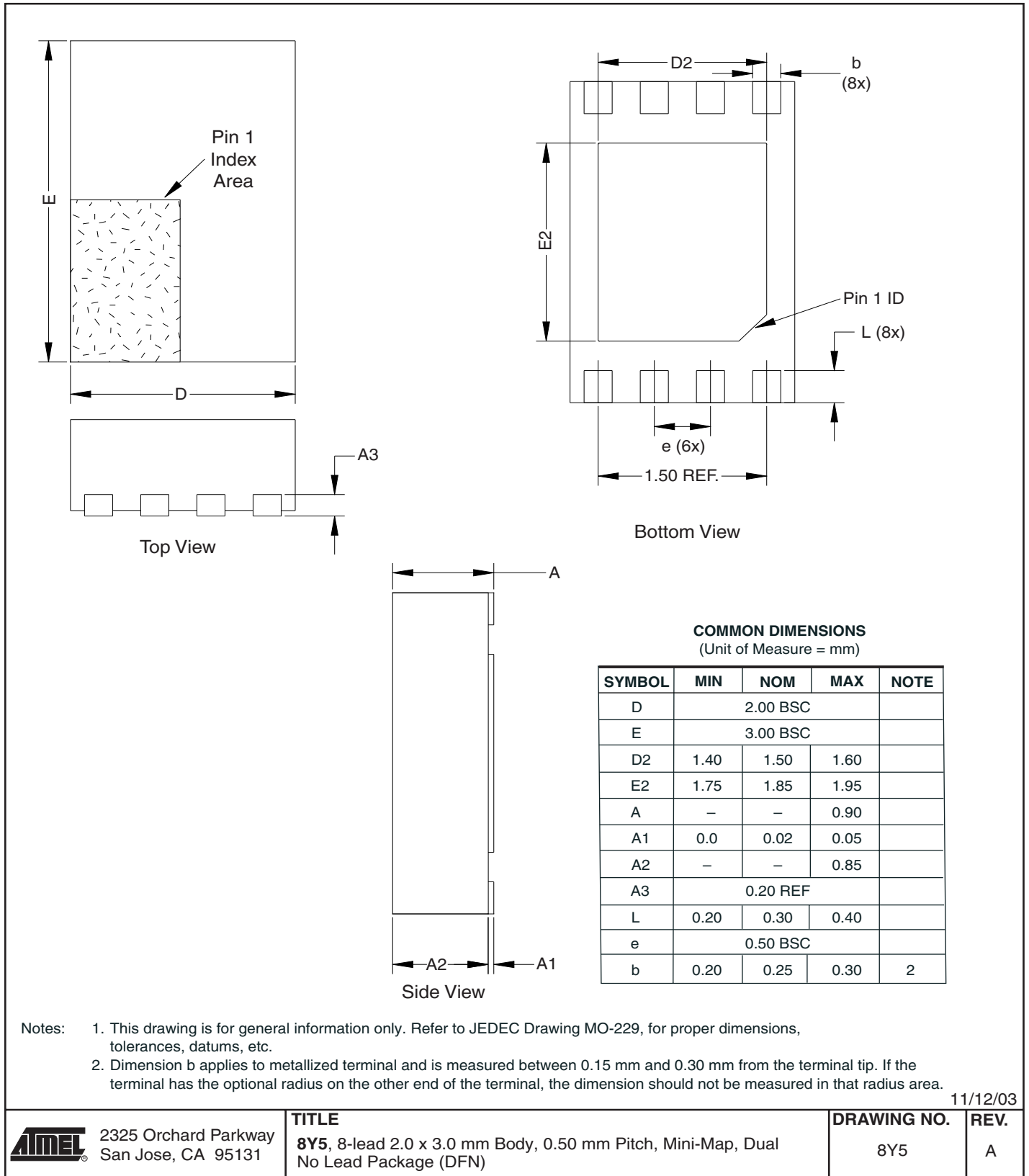
8Y1

**REV.**

C



# 8Y5 – MAP





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