Features

- Supply Voltage up to 40V
- Operating Voltage V_S = 5V to 27V
- Typically 10 µA Supply Current During Sleep Mode
- Typically 57 µA Supply Current in Silent Mode
- Linear Low-drop Voltage Regulator:
  - Normal, Fail-safe, and Silent Mode
  - ATA6623: V_{CC} = 3.3V ±2%
  - ATA6625: V_{CC} = 5.0V ±2%
  - Sleep Mode: V_{CC} is Switched Off
- V_{CC} Undervoltage Detection with Reset Open Drain Output NRES (4 ms Reset Time)
- Voltage Regulator is Short-circuit and Over-temperature Protected
- LIN Physical Layer According to LIN 2.0, 2.1 and SAEJ2602-2
- Wake-up Capability via LIN Bus (90 µs Dominant)
- TXD Time-out Timer
- Bus Pin is Overtemperature and Short-circuit Protected versus GND and Battery
- Advanced EMC and ESD Performance
- Fulfills the OEM “Hardware Requirements for LIN in Automotive Applications Rev1.0”
- Interference and Damage Protection According to ISO7637
- Package: SO8

LIN Bus Transceiver with Integrated Voltage Regulator

ATA6623
ATA6625
ATA6623C
ATA6625C

1. Description

ATA6623/ATA6625 is a fully integrated LIN transceiver, designed according to the LIN specification 2.0 and 2.1, with a low-drop voltage regulator (3.3V/5V/50 mA). The combination of voltage regulator and bus transceiver makes it possible to develop simple, but powerful, slave nodes in LIN Bus systems. ATA6623/ATA6625 is designed to handle the low-speed data communication in vehicles (for example, in convenience electronics). Improved slope control at the LIN driver ensures secure data communication up to 20 kBaud with an RC oscillator for the protocol handling. The bus output is designed to withstand high voltage. Sleep Mode (voltage regulator switched off) and Silent Mode (communication off; V_{CC} voltage on) guarantee minimized current consumption.

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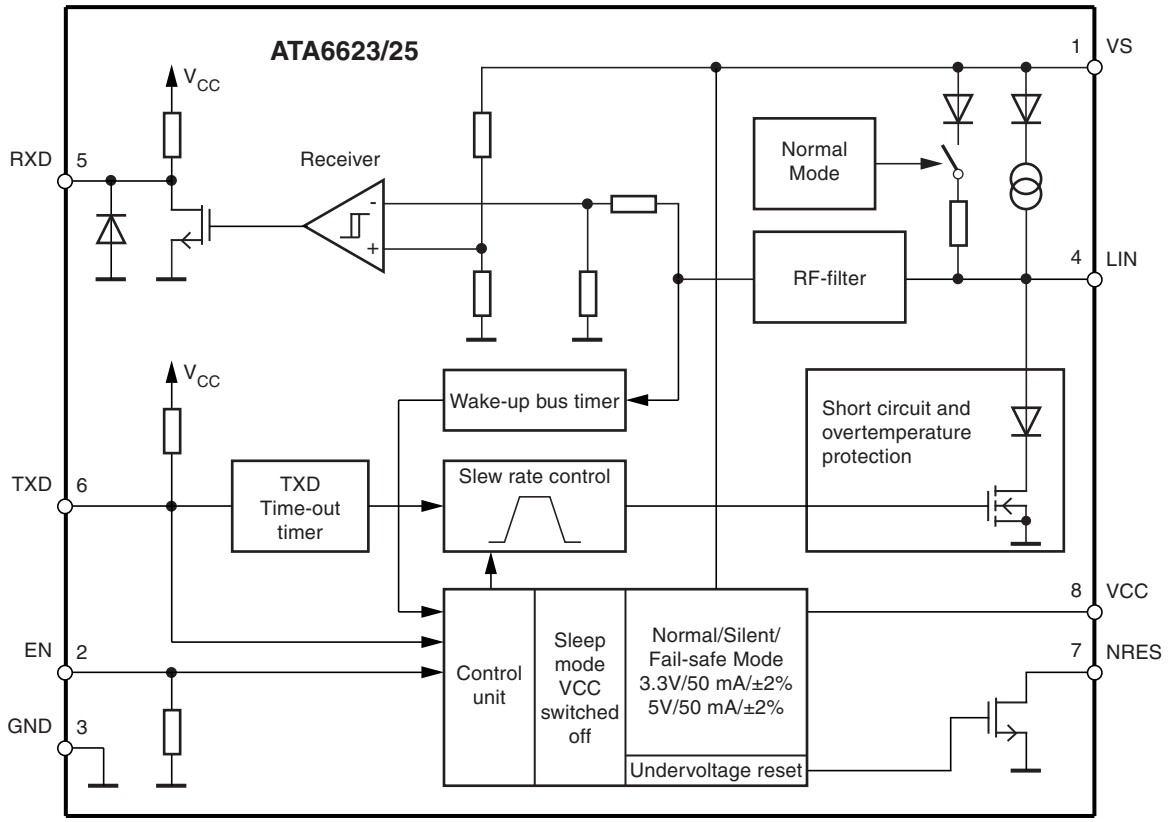
Figure 1-1. Block Diagram



2. Pin Configuration

Figure 2-1. Pinning SO8

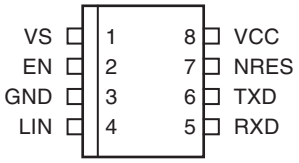


Table 2-1. Pin Description

Pin	Symbol	Function
1	VS	Battery supply
2	EN	Enables Normal Mode if the input is high
3	GND	Ground, heat sink
4	LIN	LIN bus line input/output
5	RXD	Receive data output
6	TXD	Transmit data input
7	NRES	Output undervoltage reset, low at reset
8	VCC	Output voltage regulator 3.3V/5V/50 mA

3. Functional Description

3.1 Physical Layer Compatibility

Since the LIN physical layer is independent from higher LIN layers (e.g., LIN protocol layer), all nodes with a LIN physical layer according to revision 2.x can be mixed with LIN physical layer nodes, which are according to older versions (i.e., LIN 1.0, LIN 1.1, LIN 1.2, LIN 1.3) without any restrictions.

3.2 Supply Pin (VS)

LIN operating voltage is V_S = 5V to 27V. An undervoltage detection is implemented to disable transmission if V_S falls below 5V, in order to avoid false bus messages. After switching on V_S, the IC starts with the Fail-safe Mode and the voltage regulator is switched on (i.e., 3.3V/5V/50 mA).

The supply current in Sleep Mode is typically 10 µA and 57 µA in Silent Mode.

3.3 Ground Pin (GND)

The IC does not affect the LIN Bus in the event of GND disconnection. It is able to handle a ground shift up to 11.5% of V_S.

3.4 Voltage Regulator Output Pin (VCC)

The internal 3.3V/5V voltage regulator is capable of driving loads with up to 50 mA, supplying the microcontroller and other ICs on the PCB and is protected against overload by means of current limitation and overtemperature shut-down. Furthermore, the output voltage is monitored and will cause a reset signal at the NRES output pin if it drops below a defined threshold V_{thun}.

3.5 Undervoltage Reset Output (NRES)

If the V_{CC} voltage falls below the undervoltage detection threshold of V_{thun}, NRES switches to low after tres_f (Figure 6-1 on page 11). Even if V_{CC} = 0V the NRES stays low, because it is internally driven from the V_S voltage. If V_S voltage ramps down, NRES stays low until V_S < 1.5V and then becomes highly resistant.

The implemented undervoltage delay keeps NRES low for t_{Reset} = 4 ms after V_{CC} reaches its nominal value.

3.6 Bus Pin (LIN)

A low-side driver with internal current limitation and thermal shutdown as well as an internal pull-up resistor according to LIN specification 2.x is implemented. The voltage range is from –27V to +40V. This pin exhibits no reverse current from the LIN bus to V_S, even in the event of a GND shift or V_{Batt} disconnection. The LIN receiver thresholds are compatible with the LIN protocol specification.

The fall time (from recessive to dominant) and the rise time (from dominant to recessive) are slope controlled.

3.7 Input Pin (TXD)

In Normal Mode the TXD pin is the microcontroller interface to control the state of the LIN output. TXD must be pulled to ground in order to drive the LIN bus low. If TXD is high or unconnected (internal pull-up resistor), the LIN output transistor is turned off and the bus is in the recessive state.

3.8 Dominant Time-out Function (TXD)

The TXD input has an internal pull-up resistor. An internal timer prevents the bus line from being driven permanently in the dominant state. If TXD is forced to low longer than t_{DOM} > 6 ms, the LIN bus driver is switched to the recessive state.

To reactivate the LIN bus driver, switch TXD to high (> 10 µs).

3.9 Output Pin (RXD)

This output pin reports the state of the LIN-bus to the microcontroller. LIN high (recessive state) is reported by a high level at RXD; LIN low (dominant state) is reported by a low level at RXD. The output has an internal pull-up resistor with typically 5 kΩ to V_{CC}. The AC characteristics are measured with an external load capacitor of 20 pF.

The output is short-circuit protected. In Unpowered Mode (that is, V_S = 0V), RXD is switched off.

3.10 Enable Input Pin (EN)

The Enable Input pin controls the operation mode of the device. If EN is high, the circuit is in Normal Mode, with transmission paths from TXD to LIN and from LIN to RXD both active. The VCC voltage regulator operates with 3.3V/5V/50 mA output capability.

If EN is switched to low while TXD is still high, the device is forced to Silent Mode. No data transmission is then possible, and the current consumption is reduced to I_{VS} typ. 57 µA. The VCC regulator has its full functionality.

If EN is switched to low while TXD is low, the device is forced to Sleep Mode. No data transmission is possible, and the voltage regulator is switched off.

4. Mode of Operation

Figure 4-1. Mode of Operation

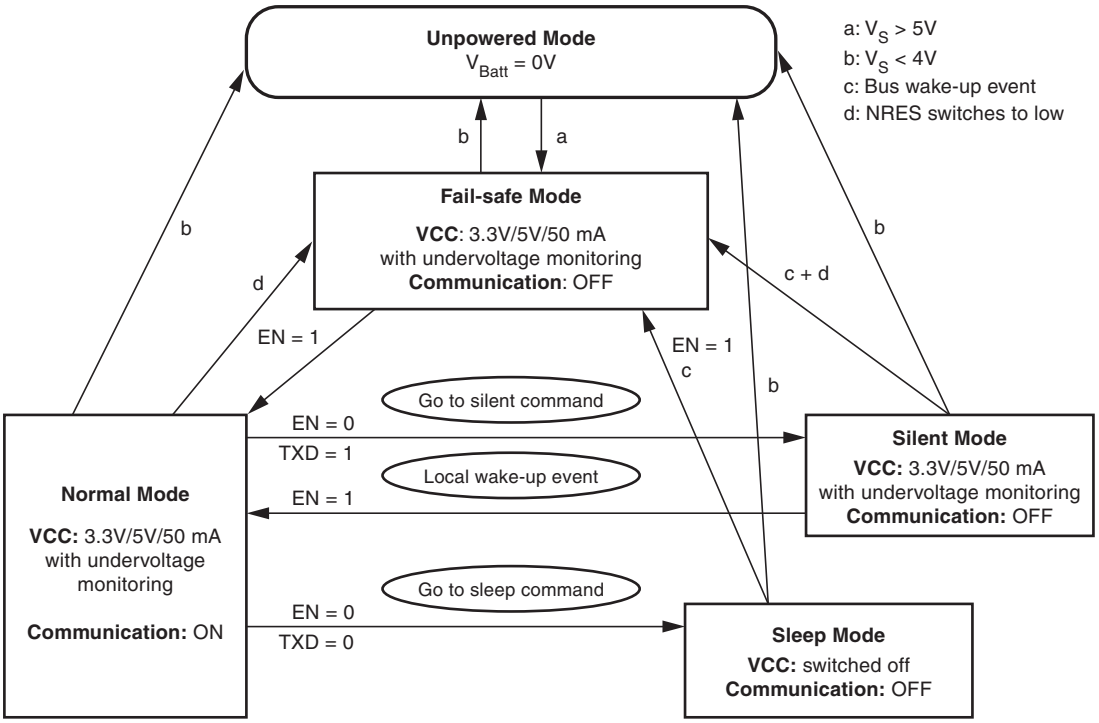


Table 4-1. Mode of Operation

Mode of Operation	Transceiver	V_{CC}	RXD	LIN
Fail safe	OFF	3.3V/5V	High, Except after wake-up	Recessive
Normal	ON	3.3V/5V	LIN depending	TXD depending
Silent	OFF	3.3V/5V	High	Recessive
Sleep	OFF	0V	0V	Recessive

4.1 Normal Mode

This is the normal transmitting and receiving Mode of the LIN Interface, in accordance with LIN specification 2.x. The V_{CC} voltage regulator operates with a 3.3V/5V output voltage, with a low tolerance of ±2% and a maximum output current of 50 mA.

If an undervoltage condition occurs, NRES is switched to low and the IC changes its state to Fail-safe Mode.

4.2 Silent Mode

A falling edge at EN while TXD is high switches the IC into Silent Mode. The TXD Signal has to be logic high during the Mode Select window (Figure 4-2 on page 7). The transmission path is disabled in Silent Mode. The overall supply current from V_{Batt} is a combination of the I_{VSsi} = 57 µA plus the V_{CC} regulator output current I_{VCC}.

The 3.3V/5V regulator with 2% tolerance can source up to 50 mA. In Silent Mode the internal slave termination between pin LIN and pin VS is disabled, and only a weak pull-up current (typically 10 µA) between pin LIN and pin VS is present. The Silent Mode can be activated independently from the current level on pin LIN.

If an undervoltage condition occurs, NRES is switched to low and the IC changes its state to Fail-safe Mode.

A voltage less than the LIN Pre-wake detection V_{LINL} at pin LIN activates the internal LIN receiver and switches on the internal slave termination between the LIN pin and the VS pin.

A falling edge at the LIN pin followed by a dominant bus level maintained for a certain time period (t_{bus}) and the following rising edge at pin LIN (see Figure 4-3 on page 7) results in a remote wake-up request.

The device switches from Silent Mode to Fail-safe Mode, and the remote wake-up request is indicated by a low level at pin RXD to interrupt the microcontroller (Figure 4-3 on page 7). EN high can be used to switch directly to Normal Mode.

Figure 4-2. Switch to Silent Mode

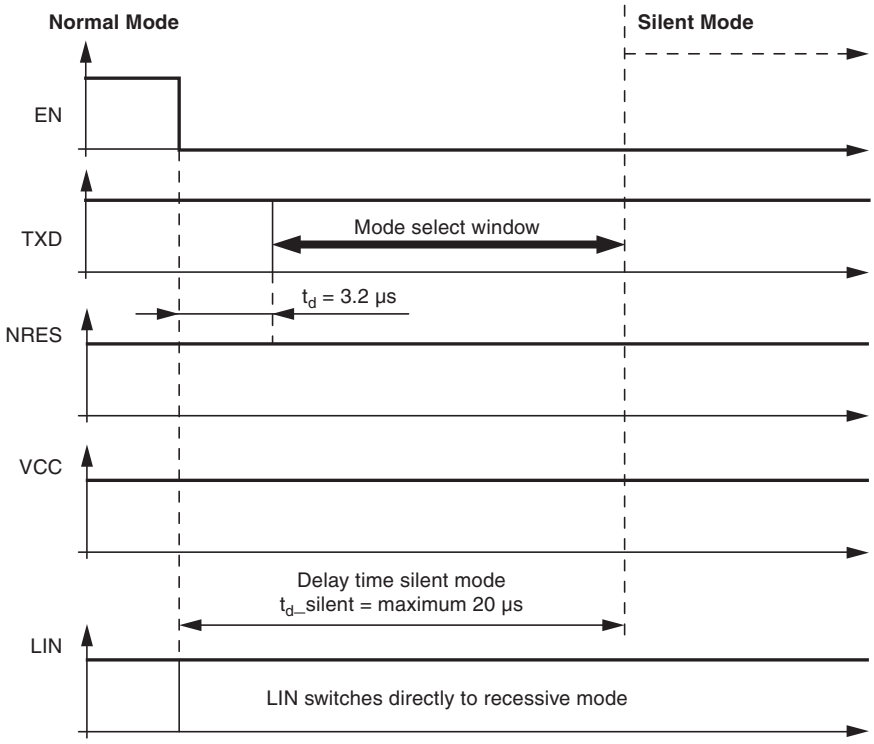
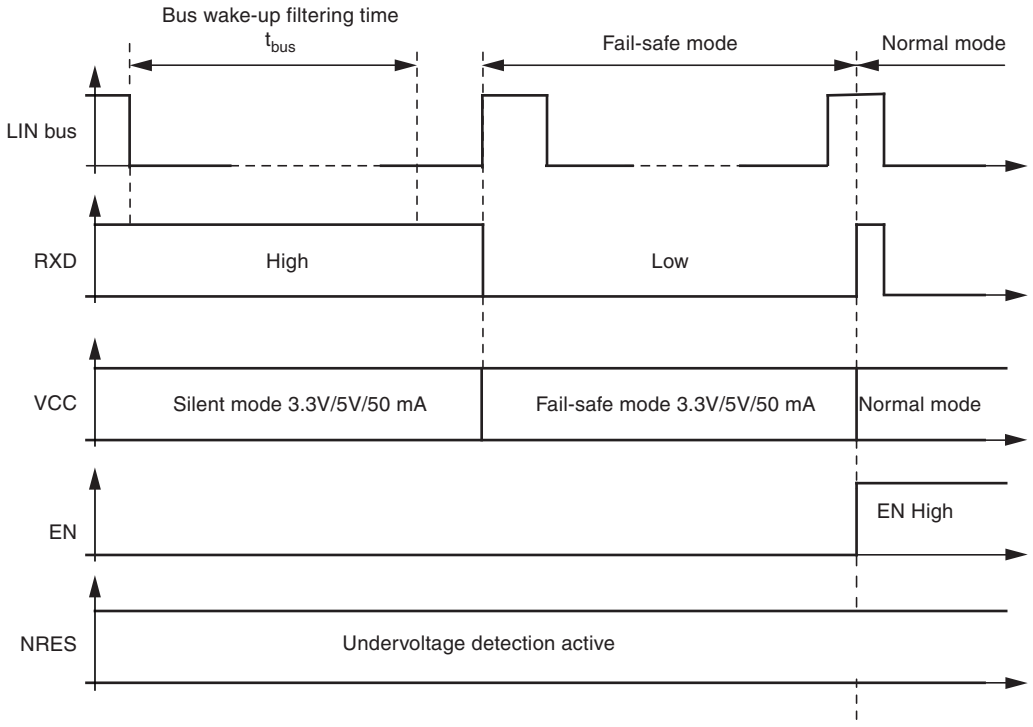


Figure 4-3. LIN Wake-up Waveform Diagram from Silent Mode



4.3 Sleep Mode

A falling edge at EN while TXD is low switches the IC into Sleep Mode. The TXD Signal has to be logic low during the Mode Select window (Figure 4-4 on page 8). To avoid influencing the LIN-pin during the switch to sleep mode, it is possible to switch the EN up to 3.2 µs earlier to LOW than the TXD. Even if the two falling edges at TXD and EN occur at the same time, the LIN line will remain uninfluenced.

In Sleep Mode the transmission path is disabled. The supply current $I_{VSsleep}$ from V_{Batt} is typically 10 µA. The V_{CC} regulator is switched off, NRES and RXD are low. The internal slave termination between pin LIN and pin VS is disabled, only a weak pull-up current (typically 10 µA) between pin LIN and pin VS is present. Sleep Mode can be activated independently from the current level on pin LIN.

A voltage less than the LIN Pre-wake detection V_{LINL} at pin LIN activates the internal LIN receiver and switches on the internal slave termination between the LIN pin and the VS pin.

A falling edge at the LIN pin followed by a dominant bus level maintained for a certain time period (t_{bus}) and a following rising edge at pin LIN results in a remote wake-up request. The device switches from Sleep Mode to Fail-safe Mode.

The V_{CC} regulator is activated, and the remote wake-up request is indicated by a low level at the RXD pin to interrupt the microcontroller (Figure 4-5 on page 9).

EN high can be used to switch directly from Sleep to Fail-safe Mode. If EN is still high after VCC ramp up and undervoltage reset time, the IC switches to Normal Mode.

Figure 4-4. Switch to Sleep Mode

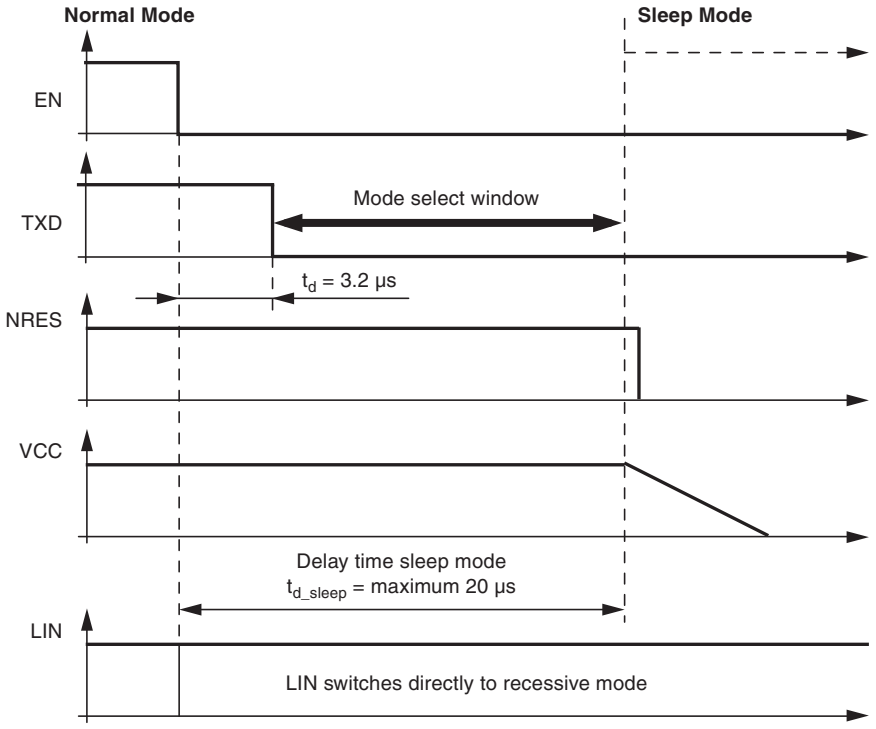
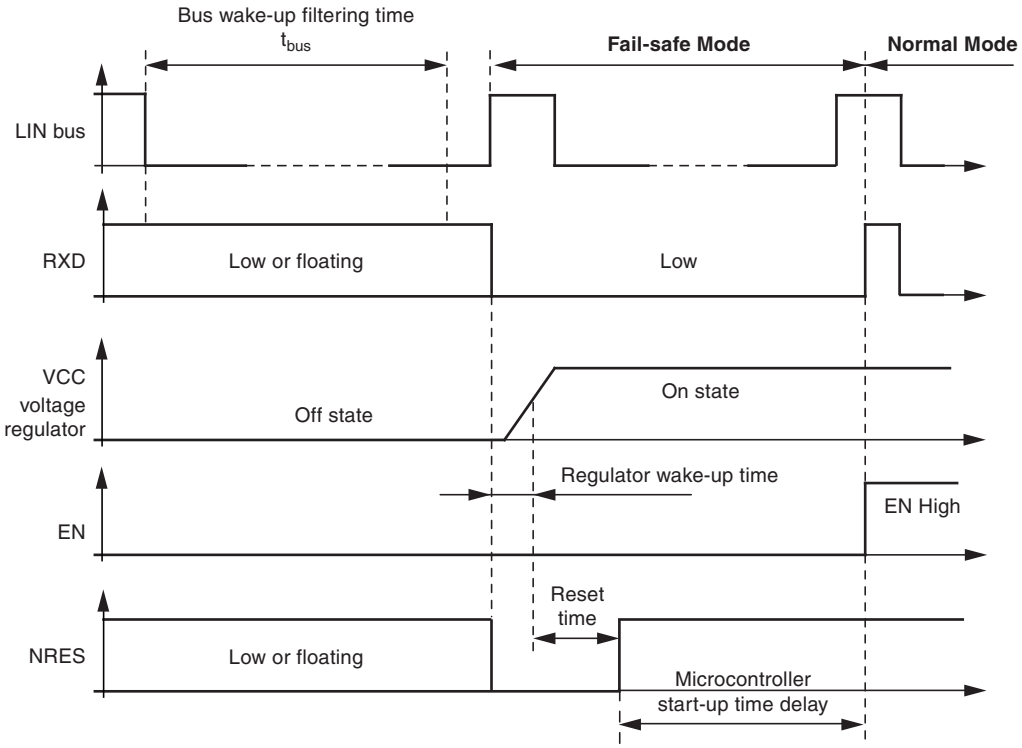


Figure 4-5. LIN Wake-up Diagram from Sleep Mode



4.4 Fail-safe Mode

At system power-up the device automatically switches to Fail-safe Mode. The voltage regulator is switched on (V_{CC} = 3.3V/5V/50 mA), (see Figure 6-1 on page 11). The NRES output switches to low for t_{res} = 4 ms and gives a reset to the microcontroller. LIN communication is switched off. The IC stays in this mode until EN is switched to high, and changes then to the Normal Mode. A power down of V_{Batt} (V_S < 4V) during Silent- or Sleep Mode switches the IC into the Fail-safe Mode after power up. A logic low at NRES switches the IC into Fail-safe Mode directly.

4.5 Unpowered Mode

If you connect battery voltage to the application circuit, the voltage at the VS pin increases according to the block capacitor (see Figure 6-1 on page 11). After VS is higher than the VS undervoltage threshold VS_{th}, the IC mode changes from Unpowered Mode to Fail-safe Mode. The VCC output voltage reaches its nominal value after t_{VCC}. This time, t_{VCC}, depends on the VCC capacitor and the load.

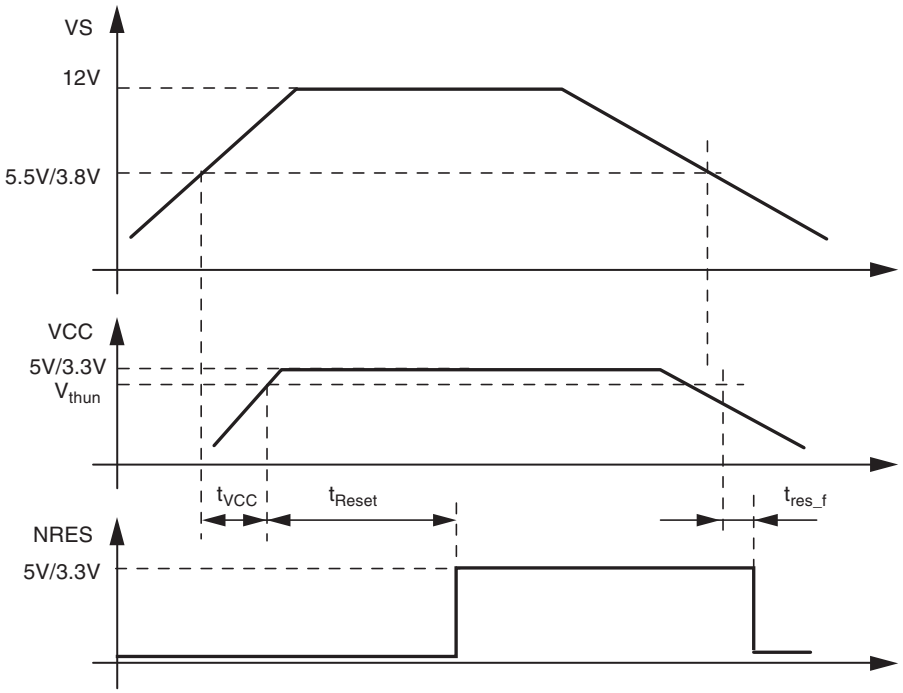
NRES is low for the reset time delay t_{Reset}; no mode change is possible during this time.

5. Fail-safe Features

- During a short-circuit at LIN to $V_{Battery}$, the output limits the output current to I_{BUS_lim}. Due to the power dissipation, the chip temperature exceeds T_{LINoff} and the LIN output is switched off. The chip cools down and after a hysteresis of T_{hys}, switches the output on again. RXD stays on high because LIN is high. During LIN overtemperature switch-off, the V_{CC} regulator is working independently.
- During a short-circuit from LIN to GND the IC can be switched into Sleep or Silent Mode. If the short-circuit disappears, the IC starts with a remote wake-up.
- The reverse current is very low < 2 µA at pin LIN during loss of V_{Batt}. This is optimal behavior for bus systems where some slave nodes are supplied from battery or ignition.
- During a short circuit at VCC, the output limits the output current to I_{VCClim}. Because of undervoltage, NRES switches to low and sends a reset to the microcontroller. The IC switches into Fail-safe Mode. If the chip temperature exceeds the value T_{VCCoff}, the V_{CC} output switches off. The chip cools down and after a hysteresis of T_{hys}, switches the output on again. Because of Fail-safe Mode, the V_{CC} voltage will switch on again although EN is switched off from the microcontroller. The microcontroller can then start with normal operation.
- Pin EN provides a pull-down resistor to force the transceiver into Recessive Mode if EN is disconnected.
- Pin RXD is set floating if V_{Batt} is disconnected.
- Pin TXD provides a pull-up resistor to force the transceiver into Recessive Mode if TXD is disconnected.
- If TXD is short-circuited to GND, it is possible to switch to Sleep Mode via ENABLE after tdom > 20 ms.

6. Voltage Regulator

Figure 6-1. V_{CC} Voltage Regulator: Ramp Up and Undervoltage



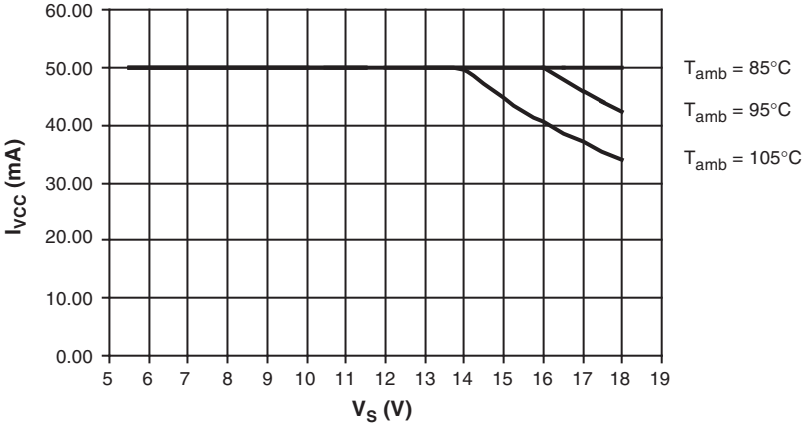
The voltage regulator needs an external capacitor for compensation and to smooth the disturbances from the microcontroller. It is recommended to use an electrolythic capacitor with C > 1.8 µF and a ceramic capacitor with C = 100 nF. The values of these capacitors can be varied by the customer, depending on the application.

With this special SO8 package (fused lead frame to pin 3) an R_{thja} of 80 K/W is achieved. Therefore, it is recommended to connect pin 3 with a wide GND plate on the printed board to get a good heat sink.

The main power dissipation of the IC is created from the V_{CC} output current I_{VCC}, which is needed for the application.

Figure 6-2 shows the safe operating area of the ATA6623/ATA6625.

Figure 6-2. Power Dissipation: Save Operating Area versus V_{CC} Output Current and Supply Voltage V_S at Different Ambient Temperatures Due to R_{thja} = 80 K/W



To program the microcontroller it may be necessary to supply the V_{CC} output via an external power supply while the V_S Pin of the system basis chip is disconnected. This issue does not occur with the system basis chip.

7. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Typ.	Max.	Unit
Supply voltage V_S	V_S	–0.3		+40	V
Pulse time ≤ 500 ms T_a = 25°C Output current I_{VCC} ≤ 50 mA	V_S			+40	V
Pulse time ≤ 2 min T_a = 25°C Output current I_{VCC} ≤ 50 mA	V_S			27	V
Logic pins (RxD, TxD, EN, NRES)		–0.3		+5.5	V
Output current NRES	I_{NRES}			+2	mA
LIN - DC voltage		–27		+40	V
V_{CC} - DC voltage		–0.3		+5.5	V
ESD according to IBEE LIN EMC Test specification 1.0 following IEC 61000-4-2 - Pin VS, LIN to GND		±6			KV
ESD HBM following STM5.1 with 1.5 kΩ/100 pF - Pin VS, LIN to GND		±6			KV
HBM ESD ANSI/ESD-STM5.1 JESD22-A114 AEC-Q100 (002)		±3			KV
CDM ESD STM 5.3.1		±750			V
Machine Model ESD AEC-Q100-RevF(003)		±200			V
Junction temperature	T_j	–40		+150	°C
Storage temperature	T_s	–55		+150	°C

8. Thermal Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance junction to ambient (free air)	R_{thja}			145	K/W
Special heat sink at GND (pin 3) on PCB	R_{thja}		80		K/W
Thermal shutdown of V_{CC} regulator	T_{VCCoff}	150	160	170	°C
Thermal shutdown of LIN output	T_{LINoff}	150	160	170	°C
Thermal shutdown hysteresis	T_{hys}		10		°C

9. Electrical Characteristics

5V < V_S < 27V, –40°C < T_j < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	**VS Pin**								
1.1	Nominal DC voltage range		VS	V_S	5	13.5	27	V	A
1.2	Supply current in Sleep Mode	Sleep Mode $V_{LIN} > V_S - 0.5V$ $V_S < 14V$ ($T_j = 25°C$)	VS	$I_{VSsleep}$	3	10	14	µA	A
		Sleep Mode $V_{LIN} > V_S - 0.5V$ $V_S < 14V$ ($T_j = 125°C$)	VS	$I_{VSsleep}$	5	11	16	µA	A
1.3	Supply current in Silent Mode	Bus recessive $V_S < 14V$ ($T_j = 25°C$) Without load at VCC	VS	I_{VSsi}	47	57	67	µA	A
		Bus recessive $V_S < 14V$ ($T_j = 125°C$) Without load at VCC	VS	I_{VSsi}	56	66	76	µA	A
1.4	Supply current in Normal Mode	Bus recessive $V_S < 14V$ Without load at VCC	VS	I_{VSrec}	0.3		0.8	mA	A
1.5	Supply current in Normal Mode	Bus dominant $V_S < 14V$ V_{CC} load current 50 mA	VS	I_{VSdom}	50		53	mA	A
1.6	Supply current in Fail-safe Mode	Bus recessive $V_S < 14V$ Without load at VCC	VS	$I_{VSspeed}$	200		500	µA	A
1.7	V_S undervoltage threshold		VS	V_{Sth}	4.0	4.5	5	V	A
1.8	VS undervoltage threshold hysteresis		VS	V_{Sth_hys}		0.2		V	A
2	**RXD Output Pin**								
2.1	Low level output sink current	Normal Mode $V_{LIN} = 0V$ $V_{RXD} = 0.4V$	RXD	I_{RXD}	1.3	2.5	8	mA	A
2.2	Low level output voltage	I_{RXD} = 1 mA	RXD	V_{RXDL}			0.4	V	A
2.3	Internal resistor to V_{CC}		RXD	R_{RXD}	3	5	7	kΩ	A
3	**TXD Input Pin**								
3.1	Low level voltage input		TXD	V_{TXDL}	–0.3		+0.8	V	A
3.2	High level voltage input		TXD	V_{TXDH}	2		V_{CC} + 0.3V	V	A
3.3	Pull-up resistor	$V_{TXD} = 0V$	TXD	R_{TXD}	125	250	400	kΩ	A
3.4	High level leakage current	V_{TXD} = VCC	TXD	I_{TXD}	–3		+3	µA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Charact1
erized on samples, D = Design parameter

9. Electrical Characteristics (Continued)

5V < V_S < 27V, –40°C < T_j < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
4	**EN Input Pin**								
4.1	Low level voltage input		EN	V_{ENL}	–0.3		+0.8	V	A
4.2	High level voltage input		EN	V_{ENH}	2		V_{CC} + 0.3V	V	A
4.3	Pull-down resistor	V_{EN} = VCC	EN	R_{EN}	50	125	200	kΩ	A
4.4	Low level input current	V_{EN} = 0V	EN	I_{EN}	–3		+3	µA	A
5	**NRES Open Drain Output Pin**								
5.1	Low level output voltage	$V_S \geq 5.5V$ I_{NRES} = 1 mA	NRES	V_{NRESL}			0.14	V	A
5.2	Low level output low	10 kΩ to 5V V_{CC} = 0V	NRES	V_{NRESLL}			0.14	V	A
5.3	Undervoltage reset time	$V_S \geq 5.5V$ C_{NRES} = 20 pF	NRES	t_{Reset}	2	4	6	ms	A
5.4	Reset debounce time for falling edge	$V_S \geq 5.5V$ C_{NRES} = 20 pF	NRES	t_{res_f}	1.5		10	µs	A
6	**VCC Voltage Regulator ATA6623**								
6.1	Output voltage V_{CC}	4V < VS < 18V (0 mA to 50 mA)	VCC	VCC_{nor}	3.234		3.366	V	A
6.2	Output voltage V_{CC} at low V_S	3V < VS < 4V	VCC	VCC_{low}	V_S – V_{Drop}		3.366	V	A
6.3	Regulator drop voltage	VS > 3V, I_{VCC} = –15 mA	VCC	V_{D1}			200	mV	A
6.4	Regulator drop voltage	VS > 3V, I_{VCC} = –50 mA	VCC	V_{D2}		500	700	mV	A
6.5	Line regulation	4V < VS < 18V	VCC	VCC_{line}		0.1	0.2	%	A
6.6	Load regulation	5 mA < I_{VCC} < 50 mA	VCC	VCC_{load}		0.1	0.5	%	A
6.7	Power supply ripple rejection	10 Hz to 100 kHz C_{VCC} = 10 µF VS = 14V, I_{VCC} = –15 mA	VCC		50			dB	D
6.8	Output current limitation	VS > 4V	VCC	I_{VCClim}	–240	–160	–85	mA	A
6.9	Load capacity	0.2Ω < ESR < 5Ω at 100 kHz	VCC	C_{load}	1.8	10		µF	D
6.10	VCC undervoltage threshold	Referred to VCC VS > 4V	VCC	V_{thunN}	2.8		3.2	V	A
6.11	Hysteresis of undervoltage threshold	Referred to VCC VS > 4V	VCC	$Vhys_{thun}$		150		mV	A
6.12	Ramp up time VS > 4V to VCC = 3.3V	C_{VCC} = 2.2 µF I_{load} = –5 mA at VCC	VCC	t_{VCC}		100	250	µs	A
7	**VCC Voltage Regulator ATA6625**								
7.1	Output voltage V_{CC}	5.5V < VS < 18V (0 mA to 50 mA)	VCC	VCC_{nor}	4.9		5.1	V	A
7.2	Output voltage V_{CC} at low V_S	4V < VS < 5.5V	VCC	VCC_{low}	$V_S – V_D$		5.1	V	A
7.3	Regulator drop voltage	VS > 4V, I_{VCC} = –20 mA	VCC	V_{D1}			250	mV	A
7.4	Regulator drop voltage	VS > 4V, I_{VCC} = –50 mA	VCC	V_{D2}		400	600	mV	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Charact1
erized on samples, D = Design parameter

9. Electrical Characteristics (Continued)

5V < V_S < 27V, –40°C < T_j < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
7.5	Regulator drop voltage	VS > 3.3V, I_{VCC} = –15 mA	VCC	V_{D3}			200	mV	A
7.6	Line regulation	5.5V < VS < 18V	VCC	VCC_{line}		0.1	0.2	%	A
7.7	Load regulation	5 mA < I_{VCC} < 50 mA	VCC	VCC_{load}		0.1	0.5	%	A
7.8	Power supply ripple rejection	10 Hz to 100 kHz C_{VCC} = 10 µF VS = 14V, I_{VCC} = –15 mA	VCC		50			dB	D
7.9	Output current limitation	VS > 5.5V	VCC	I_{VCClim}	–240	–160	–85	mA	A
7.10	Load capacity	0.2Ω < ESR < 5Ω at 100 kHz	VCC	C_{load}	1.8	10		µF	D
7.11	VCC undervoltage threshold	Referred to VCC VS > 5.5V	VCC	V_{thunN}	4.2		4.8	V	A
7.12	Hysteresis of undervoltage threshold	Referred to VCC VS > 5.5V	VCC	$Vhys_{thun}$		250		mV	A
7.13	Ramp up time VS > 5.5V to VCC = 5V	C_{VCC} = 2.2 µF I_{load} = –5 mA at VCC	VCC	t_{VCC}		130	300	µs	A
8	**LIN Bus Driver: Bus Load Conditions: Load 1 (Small): 1 nF, 1 kΩ, Load 2 (Large): 10 nF, 500Ω, Internal Pull-up R_{RXD} = 5 kΩ, C_{RXD} = 20 pF, Load 3 (Medium): 6.8 nF, 660Ω, Characterized on Samples 10.6 and 10.7 Specifies the Timing Parameters for Proper Operation at 20 kBit/s and 10.8 and 10.9 at 10.4 kBit/s**								
8.1	Driver recessive output voltage	Load1/Load2	LIN	V_{BUSrec}	0.9 × V_S		V_S	V	A
8.2	Driver dominant voltage	V_{VS} = 7V, R_{load} = 500Ω	LIN	$V_{\_LoSUP}$			1.2	V	A
8.3	Driver dominant voltage	V_{VS} = 18V, R_{load} = 500Ω	LIN	$V_{\_HiSUP}$			2	V	A
8.4	Driver dominant voltage	V_{VS} = 7V, R_{load} = 1000Ω	LIN	$V_{\_LoSUP\_1k}$	0.6			V	A
8.5	Driver dominant voltage	V_{VS} = 18V, R_{load} = 1000Ω	LIN	$V_{\_HiSUP\_1k}$	0.8			V	A
8.6	Pull–up resistor to V_S	The serial diode is mandatory	LIN	R_{LIN}	20	30	60	kΩ	A
8.7	Voltage drop at the serial diodes	In pull-up path with R_{slave} $I_{SerDiode}$ = 10 mA	LIN	$V_{SerDiode}$	0.4		1.0	V	D
8.8	LIN current limitation V_{BUS} = V_{Batt_max}		LIN	I_{BUS_lim}	40	120	200	mA	A
8.9	Input leakage current at the receiver including pull-up resistor as specified	Input Leakage current Driver off V_{BUS} = 0V V_{Batt} = 12V	LIN	$I_{BUS\_PAS\_dom}$	–1	–0.35		mA	A
8.10	Leakage current LIN recessive	Driver off 8V < V_{Batt} < 18V 8V < V_{BUS} < 18V $V_{BUS} \geq V_{Batt}$	LIN	$I_{BUS\_PAS\_rec}$		10	20	µA	A
8.11	Leakage current when control unit disconnected from ground. Loss of local ground must not affect communication in the residual network	GND_{Device} = V_S V_{Batt} = 12V 0V < V_{BUS} < 18V	LIN	$I_{BUS\_NO\_gnd}$	–10	+0.5	+10	µA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Charact1

erized on samples, D = Design parameter

9. Electrical Characteristics (Continued)

5V < V_S < 27V, –40°C < T_j < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
8.12	Leakage current at disconnected battery. Node has to sustain the current that can flow under this condition. Bus must remain operational under this condition.	V_{Batt} disconnected V_{SUP_Device} = GND 0V < V_{BUS} < 18V	LIN	$I_{BUS\_NO\_bat}$		0.1	2	µA	A
8.13	Capacitance on Pin LIN to GND		LIN	C_{LIN}			20	pF	D
9	**LIN Bus Receiver**								
9.1	Center of receiver threshold	V_{BUS_CNT} = (V_{th_dom} + V_{th_rec})/2	LIN	V_{BUS_CNT}	0.475 × V_S	0.5 × V_S	0.525 × V_S	V	A
9.2	Receiver dominant state	V_{EN} = 5V	LIN	V_{BUSdom}	–27		0.4 × V_S	V	A
9.3	Receiver recessive state	V_{EN} = 5V	LIN	V_{BUSrec}	0.6 × V_S		40	V	A
9.4	Receiver input hysteresis	V_{hys} = V_{th_rec} – V_{th_dom}	LIN	V_{BUShys}	0.028 × V_S	0.1 x V_S	0.175 × V_S	V	A
9.5	Pre-wake detection LIN High level input voltage		LIN	V_{LINH}	V_S – 2V		V_S + 0.3V	V	A
9.6	Pre-wake detection LIN Low level input voltage	Activates the LIN receiver	LIN	V_{LINL}	–27		V_S – 3.3V	V	A
10	**Internal Timers**								
10.1	Dominant time for wake–up via LIN bus	V_{LIN} = 0V	LIN	t_{bus}	30	90	150	µs	A
10.2	Time delay for mode change from Fail-safe into Normal Mode via pin EN	V_{EN} = 5V	EN	t_{norm}	5		20	µs	A
10.3	Time delay for mode change from Normal Mode to Sleep Mode via pin EN	V_{EN} = 0V	EN	t_{sleep}	2	7	15	µs	A
10.4	TXD dominant time out time	V_{TXD} = 0V	TXD	t_{dom}	6	13	20	ms	A
10.5	Time delay for mode change from Silent Mode into Normal Mode via EN	V_{EN} = 5V	EN	t_{s_n}	5	15	40	µs	A
10.6	Duty cycle 1	$TH_{Rec(max)}$ = 0.744 × V_S $TH_{Dom(max)}$ = 0.581 × V_S V_S = 7.0V to 18V t_{Bit} = 50 µs D1 = $t_{bus\_rec(min)}$/(2 × t_{Bit})	LIN	D1	0.396				A
10.7	Duty cycle 2	$TH_{Rec(min)}$ = 0.422 × V_S $TH_{Dom(min)}$ = 0.284 × V_S V_S = 7.6V to 18V t_{Bit} = 50 µs D2 = $t_{bus\_rec(max)}$/(2 × t_{Bit})	LIN	D2			0.581		A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Charact1
erized on samples, D = Design parameter

9. Electrical Characteristics (Continued)

5V < V_S < 27V, –40°C < T_j < 150°C; unless otherwise specified all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
10.8	Duty cycle 3	$TH_{Rec(max)} = 0.778 \times V_S$ $TH_{Dom(max)} = 0.616 \times V_S$ V_S = 7.0V to 18V t_{Bit} = 96 µs D3 = $t_{bus\_rec(min)}/(2 \times t_{Bit})$	LIN	D3	0.417				A
10.9	Duty cycle 4	$TH_{Rec(min)} = 0.389 \times V_S$ $TH_{Dom(min)} = 0.251 \times V_S$ V_S = 7.6V to 18V t_{Bit} = 96 µs D4 = $t_{bus\_rec(max)}/(2 \times t_{Bit})$	LIN	D4			0.590		A
10.10	Slope time falling and rising edge at LIN	V_S = 7.0V to 18V	LIN	t_{SLOPE_fall} t_{SLOPE_rise}	3.5		22.5	µs	A
11	**Receiver Electrical AC Parameters of the LIN Physical Layer LIN Receiver, RXD Load Conditions: C_{RXD} = 20 pF**								
11.1	Propagation delay of receiver Figure 9-1	V_S = 7.0V to 18V $t_{rx\_pd} = \max(t_{rx\_pdr}, t_{rx\_pdf})$	RXD	t_{rx_pd}			6	µs	A
11.2	Symmetry of receiver propagation delay rising edge minus falling edge	V_S = 7.0V to 18V $t_{rx\_sym} = t_{rx\_pdr} - t_{rx\_pdf}$	RXD	t_{rx_sym}	–2		+2	µs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Charact1
erized on samples, D = Design parameter

Figure 9-1. Definition of Bus Timing Characteristics

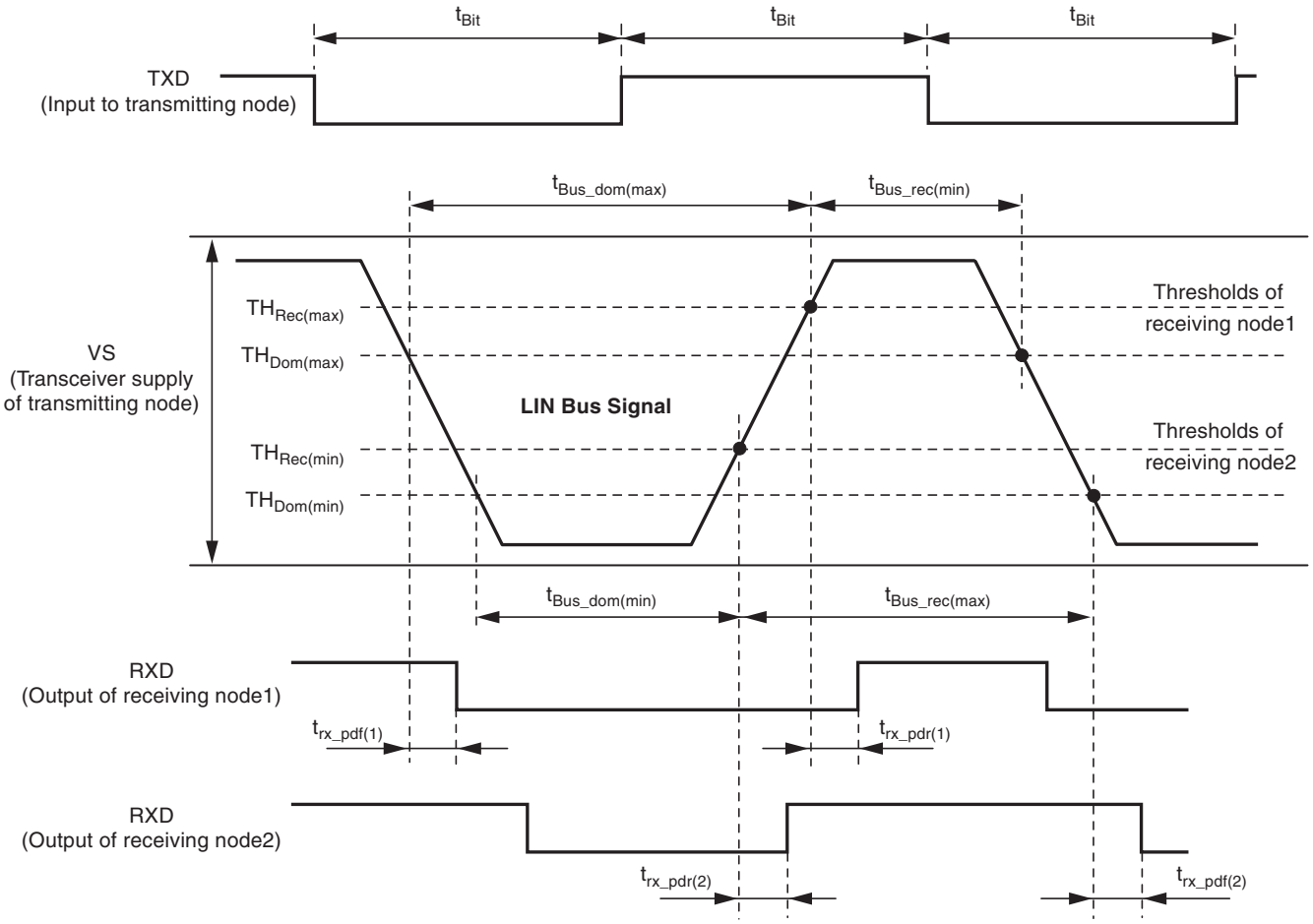
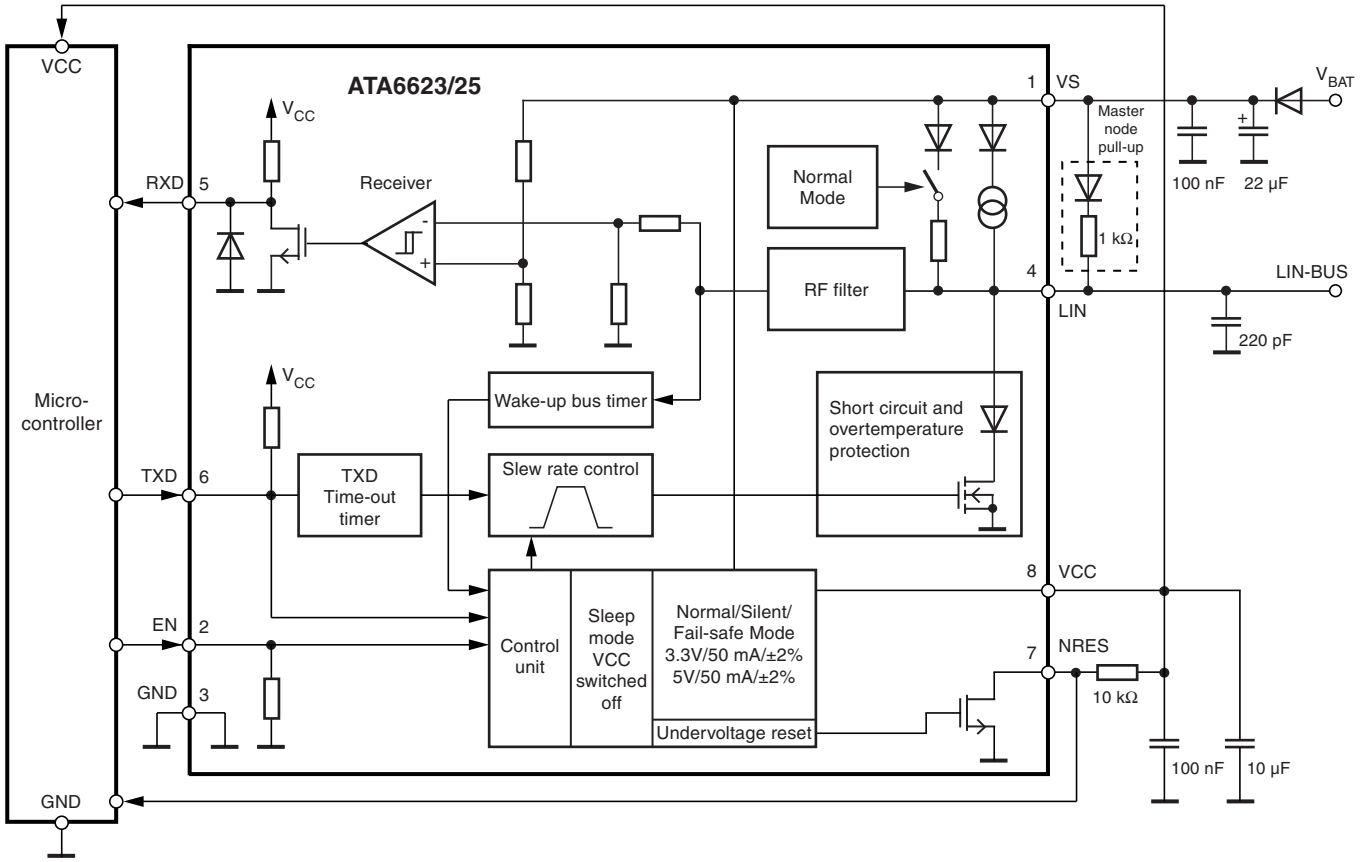


Figure 9-2. Application Circuit



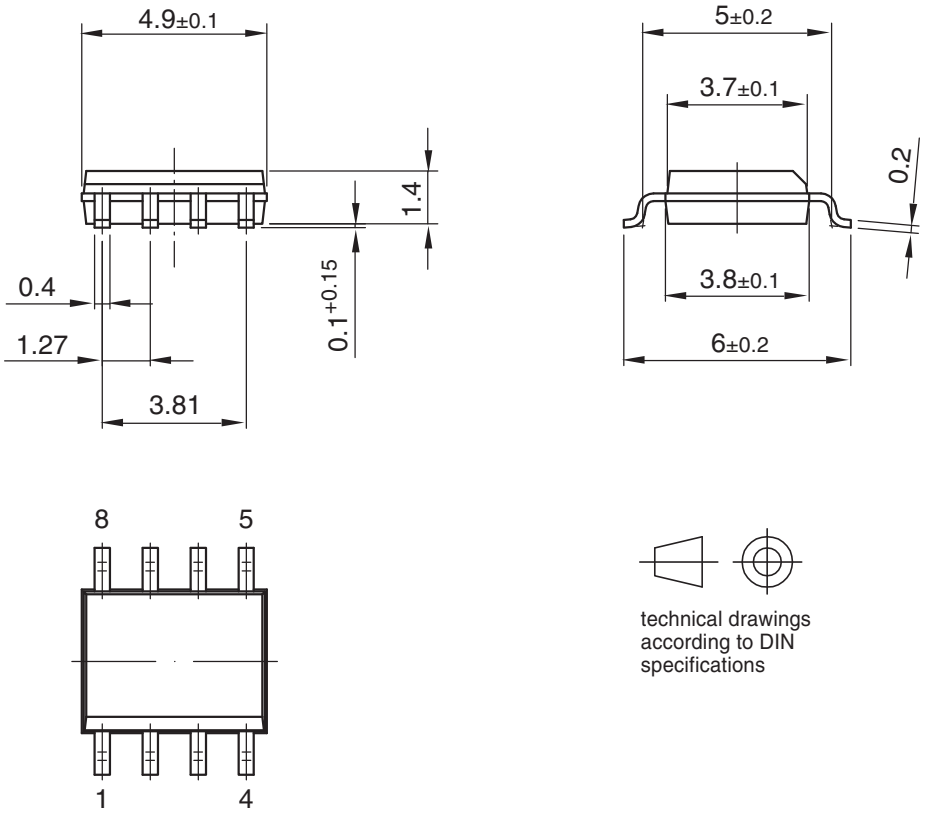
10. Ordering Information

Extended Type Number	Package	Remarks
ATA6623-TAPY	SO8	3.3V LIN system basis chip, Pb-free, 1k, taped and reeled
ATA6625-TAPY	SO8	5V LIN system basis chip, Pb-free, 1k, taped and reeled
ATA6623-TAQY	SO8	3.3V LIN system basis chip, Pb-free, 4k, taped and reeled
ATA6625-TAQY	SO8	5V LIN system basis chip, Pb-free, 4k, taped and reeled
ATA6623C-TAPY	SO8	3.3V LIN system basis chip, Pb-free, 1k, taped and reeled
ATA6625C-TAPY	SO8	5V LIN system basis chip, Pb-free, 1k, taped and reeled
ATA6623C-TAQY	SO8	3.3V LIN system basis chip, Pb-free, 4k, taped and reeled
ATA6625C-TAQY	SO8	5V LIN system basis chip, Pb-free, 4k, taped and reeled

11. Package Information

Package: SO 8

Dimensions in mm



Drawing-No.: 6.541-5031.01-4

Issue: 1; 15.08.06

12. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4957H-AUTO-05/10	• New Part numbers ATA6623C and ATA6625C added • Features on page 1 changed • Text under heading 3.3 on page 3 changed • Text under heading 3.9 on page 4 changed • Abs.Max.Rat.Table -> Values in row “ESD HBM following....” changed • El.Char.Table -> rows changed: 5.1, 5.2, 6.5, 6.6, 6.7, 6.8, 7.6, 7.7, 7.8,7.9, 10.2 • El.Char.Table -> row 8.13 added • Ord.Info.Table -> Part numbers ATA6623C and ATA6625C added
4957G-AUTO-09/09	• Figures changed: 1-1, 4-2, 4-3, 4-4, 4-5, 6-2, 9-2 • Sections changed: 3.1, 3.6, 3.8, 3.9, 3.10, 4.1, 4.2, 4.3, 5 • Description Text changed • Table 4-1 changed • Abs. Max. Ratings table changed • El. Characteristics table changed
4957F-AUTO-02/08	• “Pre-normal Mode” in “Fail-safe Mode” changed • Section 7 “Absolute Maximum Ratings” on page 13 changed • Section 8 “Electrical Characteristics” numbers 10.5 to 10.10 on pages 17 to 18 changed
4957E-AUTO-10/07	• Section 9 “Ordering Information” on page 20 changed
4957D-AUTO-07/07	• Features changed • Block diagram changed • Application diagram changed • Text changed under the headings: 3.2, 3.3, 3.4, 3.6, 3.7, 3.8, 3.9, 4, 4.1, 4.2, 4.3, 4.4, 4.5, 5.5, 5.6, 6 • Figure 4-2, 4-3, 4-4, 4-5, 8-2: changed • Figure title 6-1: text changed • Abs. Max. Ratings: row “Output current NRES” added • El. Char. table: values changed in the following rows: 1.3, 5.1, 5.3, 5.4, 6.9, 6.12, 7.9, 11.1

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4957C-AUTO-02/07	• Features on page 1 changed • Table 2-1 “Pin Description” on page 2 changed • Section 3-1 “Physical Layer Compatibility” on page 3 added • Section 3-2 “Supply Pin (VS) on page 3 changed • Section 3-3 “Ground Pin (GND) on page 3 changed • Section 3-8 “Dominant Time-out Function (TXD)” on page 4 changed • Section 4-1 “Normal Mode” on page 5 changed • Section 4-2 “Silent Mode” on page 5 changed • Figure 4-3 “LIN Wake-up Waveform Diagram from Silent Mode” on page 6 changed • Section 4.3 “Sleep Mode” on page 7 changed • Section 4-5 “Unpowered Mode” on page 7 changed • Figure 4-4 “Switch to Sleep Mode” on page 8 changed • Figure 4-6 “V_{CC} Voltage Regulator: Ramp up and Undervoltage” on page 9 changed • Section 5 “Fail-safe Features on page 9 changed • Section 6 “Voltage Regulator” on page 10 changed • Section 7 “Absolute Maximum Ratings” on page 11 changed • Section 8 “Electrical Characteristics” on pages 12 to 16 changed • Section 9 “Ordering Information” on page 18 changed

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