Features

- **Comprehensive Library of Standard Logic and I/O Cells**
- **ATC18 Core and I/O Cells Designed to Operate with V_{DD} = 1.8V ± 0.15V as Main Target Operating Conditions**
- **IO33 Pad Libraries Provide Interfaces to 3V Environments**
- **Memory Cells Compiled to the Precise Requirements of the Design**
- **Compatible with Atmel's Extensive Range of Microcontroller, DSP, Standard-interface and Application-specific Cells**
- **EDAC Library**
- **SEU Hardened DFF's**
- **Cold Sparring Buffers**
- **High Speed LVDS Buffers**
- **PCI Buffer**
- **Predefined die Sizes to Easily Accommodate Specified Packages**
- **MQFP Packages up to 352 pins (340 Signal Pins)**
- **MCGA Packages up to 625 pins (581 Signal Pins)**
- **Offered to QML Q Grade**

Description

The Atmel ATC18M is fabricated on a proprietary 0.18 µm, up to six-layer-metal CMOS process intended for use with a supply voltage of 1.8V ± 0.15V. Table 1 shows the range for which Atmel library cells have been characterized.

Table 1. Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	DC Supply Voltage	Core and Standard I/Os	1.65	1.8	1.95	V
$V_{DD3.3}$	DC Supply Voltage	3V Interface I/Os	3	3.3	3.6	V
V_I	DC Input Voltage		0		V_{DD}	V
V_O	DC Output Voltage		0		V_{DD}	V
TEMP	Operating Free Air Temperature Range	Military	-55		+125	°C

The Atmel cell libraries and megacell compilers have been designed in order to be compatible with each other. Simulation representations exist for three types of operating conditions. They correspond to three characterization conditions defined as follows:

- MIN conditions:
  - T_J = -55°C
  - V_{DD} (cell) = 1.95V
  - Process = fast
- TYP conditions:
  - T_J = +25°C
  - V_{DD} (cell) = 1.8V
  - Process = typ
- MAX conditions:
  - T_J = +125°C
  - V_{DD} (cell) = 1.65V
  - Process = slow

0.18 µm CMOS Cell-based ASIC for Military Use

ATC18M

Advanced Information

Rev. 4262A–AERO–07/03

Delays to tri-state are defined as delay to turn off (VGS < VT) of the driving devices. Output pad drain current corresponds to the output current of the pad when the output voltage is V_{OL} or V_{OH}. The output resistor of the pad and the voltage drop due to access resistors (in and out of the die) are taken into account. In order to have accurate timing estimates, all characterization has been run on electrical netlists extracted from the lay-out database.

Standard Cell Library SClib

The Atmel Standard Cell Library, SClib, contains a comprehensive set of a combination of logic and storage cells. The SClib library includes cells that belong to the following categories:

- Buffers and Gates
- Multiplexers
- Flip-flops
- Scan Flip-flops
- Latches
- Adders and Subtractors

Decoding the Cell Name

Table 2 shows the naming conventions for the cells in the SClib library. Each cell name begins with either a two-, three-, or four-letter code that defines the type of cell. This indicates the range of standard cells available.

Table 2. Cell Codes

Code	Description	Code	Description
AD	Adder	INVB	Balanced Inverter
AH	Half Adder	INVT	Inverting Tri-state Buffer
AS	Adder/Subtractor	LA	D Latch
AN	AND Gate	MI	Inverting Multiplexer
AOI	AND-OR-Invert Gate	MX	Multiplexer
AON	AND-OR-AND-Invert Gates	ND	NAND Gate
AOR	AND-OR Gate	NR	NOR Gate
BUFB	Balanced Buffer	OAI	OR-AND-Invert Gate
BUFF	Non-Inverting Buffer	OAN	OR-AND-OR-Invert Gates
BUFT	Non-Inverting Tri-state Buffer	OR	OR Gate
CG	Carry Generator	ORA	OR-AND Gate
CLK2	Clock Buffer	SD	Multiplexed Scan D Flip-flop
DF	D Flip-flop	SRLA	Set/Reset Latches with NAND input
DLA	Dual Input Latches	SU	Subtractor
H...	SEU Hardened Versions	XN	Exclusive NOR Gate
INV0	Inverter	XR	Exclusive OR Gate

Cell Matrices

Table 3 and Table 4 provide a quick reference to the storage elements in the SClib library. Note that all storage elements feature buffered clock inputs and buffered output.

Table 3. D Flip-flops

Macro Name	Set	Clear	Enabled D Input	1xDrive	2xDrive	Single Output	SEU Hardened
DFBRBx	•	•		•	•		
DFCRBx		•		•	•		
HDFBRBx	•	•		•	•		•
HDFCRBx		•		•	•		•
DFNRBx				•	•		
HDFVRBx				•	•		•
DFPRBx	•			•	•		
HDFPRBx	•			•	•		•
DENRQx			•	•	•	•	

Table 4. Scan Flip-flops

Macro Name	Set	Clear	1xDrive	2xDrive	Single Output	SEU Hardened
SDBRBx	•	•	•	•		
SDCRBx		•	•	•		
HSDBRBx	•	•	•	•		•
HSDCRBx		•	•	•		•
SDNRBx			•	•		
HSDNPBx			•	•		•
SDNRQx			•	•	•	
HSDNRQx			•	•		•

Input/Output Pad Cell Libraries IO18lib and IO33lib

The Atmel Input/Output Cell Library, IO18lib, contains a comprehensive list of input, output, bi-directional and tri-state cells. The ATC18M (1.8V) cell library includes one special sets of I/O cells, IO25lib and IO33lib, for interfacing with external 3.3V devices.

They will encompass the following types of cells:

- Bi-directional
- Tri-state outport
- Outputs
- Inputs
- PCI
- PECL
- LVDS (EIA-644)

All buffers will be capable of being used as “Cold Sparing” Buffers.

Compiled Memories

Based on Virage Logic Memory Compilers, for synchronized memories. Its maximum memory size compilation capability is:

SRAM	16K x 32 bits
DPRAM	8K x 32 bits
TPSF	1K x 16 bits

A set of EDAC can be used in combination with these memories so as to alleviate their SEU susceptibility.

Synthesized Memory

The synthesis of memories is based on Atmel GENESYS within the GATEAID software. It must be used only for small memories and when SEU hardened cells are needed.

The maximum memory sizes are as follows:

RAM	4K bits
TPRAM	4K bits
DPRAM	2K bits

Design Flow

Though only MODELSIM and NCSIM will be used as the golden simulators, the design kit will include the data and libraries needed for the following tools:

Tool	Supplier	Purpose
GATEAID2®	Atmel	Atmel Support tools
MODELSIM®	Mentor	VHDL®/VITAL® RTL + gate level simulation
NCSIM®	Cadence	VERILOG® RTL + gate level simulation
DESIGN COMPILER®	Synopsys®	HDL synthesis
BUILDGATES®	Cadence®	HDL synthesis
POWER COMPILER	Synopsys	Synthesis power optimization
DFT SUITE	Mentor®	Scan+ATPG (FastScan), JTAG (BSD-Architect), BIST (MBIST-Architect)
FE-ULTRA	Cadence	Floor-planning, physical knowledgeable synthesis, layout prototyping
PRIMETIME®	Synopsys	Static timing analysis
FORMALITY	Synopsys	Equivalence checking, formal proof

The Design flow can be described in two sections:

- The front-end done at the customer's premises
- The back-end at Atmel Technical Centers, provided that the front-end activity has been validated and accepted by Atmel during the Logic Review (LR) meeting.

The following table lists the activities and tools that will be used during the front-end design.

Function	Tool	Supplier
RTL SIMULATION	MODELSIM	Mentor
	NC-SIM	Cadence
CODE COVERAGE	VHDL-COVER	Transeda
RTL TO GATE SYNTHESIS	DESIGN-COMPILER	Synopsys
	BUILD-GATES	Cadence
POWER OPTIMIZATION	POWER-COMPILER	Synopsys
POWER ANALYSIS	PRIME-POWER	Synopsys
TEST INSERTION + ATPG	DFT-SUITE	Mentor
GATE LEVEL SIMULATION	MODELSIM	Mentor
	NC-SIM	Cadence
NETLIST TRANSLATION	NETCVT	Atmel
DESIGN RULES CHECK	STAR	Atmel

The following table lists the activities and the tools that will be used during the back-end design:

Activities	Function	Tool	Supplier
Bonding Diagram	Array Definition	MGTECHGEN	Atmel
	Pads Coordinates	PACO	Atmel
	Bonding Diagram	PIMTOOL	Atmel
	Pads Preplacement	P2DEF	Atmel
	Periphery Check	CAP	Atmel
	Ibis Model	GENIBIS	Atmel
Physical Implementation	Blocks Preplacement	SILVER	Atmel
	Virtual Layout Prototyping	FIRST ENCOUNTER	Cadence
	Physically Knowledgeable Synthesis	PKS	Cadence
	Power Routing	SNOW	Atmel
	Placement	QPLACE	Cadence
	Scan Chains Ordering	QP/SCAN	Cadence
	Placement-driven Violations Fix	QP/OPT	Cadence
	Clock Tree Synthesis	CTGEN®	Cadence
	Routing	NANOROUTE	Cadence
	Parasitics Extraction	HYPEREXTRACT	Cadence
	Final Violations Fix	QP/OPT	Cadence
	Eco Place & Route	SILICON ENSEMBLE	Cadence
	Layout Edition	SILVER	Atmel
	3d Extraction	FIRE&ICE	Cadence

Activities	Function	Tool	Supplier
Final Verifications	Static Timing Analysis	PRIMETIME	Synopsys
	Equivalence Checking	FORMALITY	Synopsys
	Back-annotated Simulation	MODELSIM	Mentor
		NC-SIM	Cadence
	Consumption Analysis	MGCOMET	Atmel
	Power Scheme Check	VOLTAGESTORM	Cadence
	Test Patterns	PATFORM	Atmel
	Gdsii Generation	SE2GDS	Atmel
	Cross-talk Analysis	CELTIC	Cadence
	Cross-talk Errors Fix	SILICON ENSEMBLE	Cadence
	Final Analysis	SIGNALSTORM	Cadence

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