Cell-based ASIC

ATC35 Summary

Features

- **Comprehensive Library of Standard Logic Cells**
- **ATC35 I/O Cells Designed to Operate with V_{DD} = 3.3V ± 0.3V as Main Target Operating Conditions**
- **IO35 Pad Library Provides Interface to 5V Environment**
- **Oscillators and Phase Locked Loops for Stable Clock Sources**
- **Memory Cells Compiled to the Precise Requirements of the Design**
- **Compatible with Atmel's Extensive Range of Microcontroller, DSP, Standard Interface and Application Specific Cells**
- **High-Performance Analog Cells can be Developed on Request**

Description

The Atmel ATC35 (AT56K) process is a proprietary 0.35 micron three-layer-metal CMOS process intended for use with a supply voltage of 3.3V ± 0.3V. The following table shows the range for which Atmel library cells have been characterized.

Table 1. Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD3}	DC Supply Voltage	Core and Standard I/Os	3.0	3.3	3.6	V
V_{DD5}	DC Supply Voltage	5V Interface I/Os	4.5	5.0	5.5	V
V_I	DC Input Voltage		0		V_{DD}	V
V_O	DC Output Voltage		0		V_{DD}	V
TEMP	Operating Free Air Temperature Range	Industrial	-55		+85	°C

The Atmel cell libraries and megacell compilers have been designed in order to be compatible with each other. Simulation representations exist for three types of operating conditions. They correspond to three characterization conditions defined as follows:

- MIN conditions:
  T_J = -55°C
  V_{DD} (cell) = 3.60V
  Process = fast (industrial best case)
- TYP conditions:
  T_J = +25°C
  V_{DD} (cell) = 3.30V
  Process = typ (industrial typical case)
- MAX conditions:
  T_J = +100°C
  V_{DD} (cell) = 3.00V
  Process = slow (industrial worst case)

Delays to tristate are defined as delay to turn off (VGS < VT) of the driving devices. Output pad drain current corresponds to the output current of the pad when the output voltage is V_{OL} or V_{OH}. The output resistor of the pad and the voltage drop due to access resistors (in and out of the die) are taken into account. In order to have accurate timing estimates, all characterization has been run on electrical netlists extracted from the layout database.

Rev. 1063CS–CBIC–01/03

Standard Cell Library SClib

The Atmel Standard Cell Library, SClib, contains a comprehensive set of combinational logic and storage cells. The SClib library includes cells which belong to the following categories:

- Buffers and Gates
- Multiplexers
- Flip-flops
- Scan Flip-flops
- Latches
- Adders and Subtractors

Decoding the Cell Name

The table below shows the naming conventions for the cells in the SClib library. Each cell name begins with either a two-, three-, or four-letter code that defines the type of cell. This indicates the range of standard cells available.

Table 2. Cell Codes

Code	Description	Code	Description
AD	Adder	LASR	Set/Reset Latch
AN	AND Gate	MI	Inverting Multiplexer
AOI	AND-OR-Invert Gate	MFF	Multiplexed flip-flop with Feedback
AON	AND-OR-AND-Invert Gates	MX	Multiplexer
AOR	AND-OR Gate	ND	NAND Gate
BH	Bus Holder	NR	NOR Gate
BUFF	Non-Inverting Buffer	OAI	OR-AND-Invert Gate
BUFT	Non-Inverting 3-State Buffer	OAN	OR-AND-OR-Invert Gates
CLK2	Clock Buffer	OR	OR Gate
DE	D-Enabled Flip-Flop	ORA	OR-AND Gate
DF	D Flip-Flop	SD	Multiplexed Scan D Flip-Flop
INV0	Inverter	SE	Multiplexed Scan Enable D Flip-Flop
INVB	Balanced Inverter	SRLAB	Set/Reset Latches with NAND input
INVT	Inverting 3-State Buffer	SU	Subtractor
JK	JK Flip-Flop	XN	Exclusive NOR Gate
LA	D Latch	XR	Exclusive OR Gate

Cell Matrices

The following three tables provide a quick reference to the storage elements in the SClib library. Note that all storage elements feature buffered clock inputs and buffered output.

Table 3. JK Flip-flops

Macro Name	Set	Clear	1x Drive	2x Drive
JKBRBx	•	•	•	•

Table 4. D Flip-flops

Macro Name	Set	Clear	Enabled D Input	1x Drive	2x Drive	Single Output
DFBRBx	•	•		•	•	
DFCRBx		•		•	•	
DFCRQx		•		•	•	•
DFCRNx		•		•	•	
DFNRBx				•	•	
DFNRQx				•	•	•
DFPRBx	•			•	•	
DEPRQx	•		•	•	•	•
DECRQx		•	•	•	•	•

Table 5. Scan Flip-flops

Macro Name	Set	Clear	1x Drive	2x Drive	Single Output
DENRQx			•	•	•
MFFNRBx			•	•	
SDBRBx	•	•	•	•	
SDCRBx		•	•	•	
SDCRNx		•	•	•	•
SDCRQx		•	•	•	•
SDNRBx			•	•	
SDNRNx			•	•	•
SDNRQx			•	•	•
SDPRBx	•		•	•	
SECRQx		•	•	•	•
SENRQx			•	•	•
SEPRQx	•		•	•	•

Input/Output Pad Cell Libraries IOlib and IO35lib

The Atmel Input/Output Cell Library, IOlib, contains a comprehensive list of input, output, bidirectional and tristate cells. The ATC35 (AT56K) (3.3V) cell library includes a special set of I/O cells, IO35lib, for interfacing with external 5V devices.

Voltage Levels

The IOlib library is made up exclusively of low-voltage chip interface circuits powered by a voltage in the range of 3.0V to 3.6V. The library is compatible with the SClib 3-volt standard cells library.

Power and Ground Pads

Designers are strongly encouraged to provide three kinds of power pairs for the IOlib library. These are “AC”, “DC” and core power pairs. AC power is used by the I/O to switch its output from one state to the other. This switching generates noise in the AC power buses on the chip. DC power is used by the I/O to maintain its output in a steady state. The best noise performance is achieved when the DC power buses on the chip are free of noise; designers are encouraged to use separate power pairs for AC and DC power to prevent most of the noise in the AC power buses from reaching the DC power buses. The same power pairs can be used to supply both DC power to the I/Os and power to the core without affecting noise performance.

Table 6. VSS Power Pad Combinations

Core	Switching I/O	Quiet I/O	Library Cell Name	Signal Name
Vssi	VssAC	VssDC		
•			PV0I	VSS
	•		PV0A	VSS
		•	PV0D	VSS
	•	•	PV0E	VSS
•		•	PV0B	VSS
•	•	•	PV0F	VSS

Table 7. VDD Power Pad Combinations

Core	Switching I/O	Quiet I/O	Library Cell Name	Signal Name
Vddi	VddAC	VddDC		
•			PVDI	VDD
	•		PVDA	VDD
		•	PVDD	VDD
	•	•	PVDE	VDD
•		•	PVDB	VDD
•	•	•	PVDF	VDD

1063CS–CBIC–01/03

Cell Matrices

Table 8. CMOS Pads

CMOS Cell Name	3-State I/O	Output Only	3-State Output Only	Drive Strength	Pad Sites Used
PC3B01	•			1x	1
PC3B02	•			2x	1
PC3B03	•			3x	1
PC3B04	•			4x	1
PC3B05	•			5x	1
PC3O01		•		1x	1
PC3O02		•		2x	1
PC3O03		•		3x	1
PC3O04		•		4x	1
PC3O05		•		5x	1
PC3T01			•	1x	1
PC3T02			•	2x	1
PC3T03			•	3x	1
PC3T04			•	4x	1
PC3T05			•	5x	1

Table 9. TTL Pads

TTL Cell Name	3-State I/O	Output Only	3-State Output Only	Drive Strength	Pad Sites Used
PT3B01	•			2 mA	1
PT3B02	•			4 mA	1
PT3B03	•			8 mA	1
PT3O01		•		2 mA	1
PT3O02		•		4 mA	1
PT3O03		•		8 mA	1
PT3T01			•	2 mA	1
PT3T02			•	4 mA	1
PT3T03			•	8 mA	1

Table 10. CMOS/TTL Input Only Pad

CMOS Cell Name	Input Levels	Schmitt Input Level Shifter	Non-Inverting	Inverting	Pad Sites Used
PC3D01	CMOS		•		1
PC3D11	CMOS			•	1
PC3D21	CMOS	•	•		1
PC3D31	CMOS	•		•	1

Note: All 3-state I/Os, 3-state output only and input pads are also available with pull-up and pull-down device.

Table 11. Core-driven Clock Buffer Pads

Cell Name	Drive Strength	Non-Inverting	vddDC Pad	Pad Sites Used
PC3C01	1x	•	•	1
PC3C02	2x	•	•	1
PC3C03	3x	•	•	1
PC3C04	4x	•	•	1

IO35lib Low Slew Rate Cells

All IO35lib cells are slew rate controlled. Advantage has been taken of the 3.3V to 5V level shifter (which is slow by construction) to reduce the slew rate without reducing speed.

Table 12. IO35lib Pads

5V Interface Pad Name	3-State I/O	Output Only	3-State Output Only	Input Only	Drive Strength	Pad Sites Used
mc5b0x	•				2 mA, 4 mA, 8 mA, 16 mA	1
mc5d00				•		1
mc5o0x		•			2 mA, 4 mA, 8 mA, 16 mA	1
mc5t0x			•		2 mA, 4 mA, 8 mA, 16 mA	1

Note: All 3-state I/Os, 3-state output only and input pads are also available with pull-up and pull-down device.

Table 13. IO35lib Power Pads

Cell Name	Power Bus Connections				Pad Sites Used
	vssi	mixvss	vddi	mixvdd	
mv0e		•			1
mv0i	•				1
mv3i			•		1
mv5e				•	1
mc45frell, mc45freur	•	•		•	4
mc45frelr, mc45freul				•	4
mc45fr0ll, mc45fr0ur		•			4

Oscillator Cell Library Osclib

The Atmel CBIC oscillator library provides stable clock sources. This library makes the following cells available:

Crystal Oscillators and Power on Reset

The Atmel two-pad oscillators are designed with the Pierce three-point oscillator structure. For operation with most standard crystals, no external capacitors are needed. It may be necessary to add external capacitors on xin and xout to ground in special cases.

Clock output is low at off state (onosc = 0).

The oscillators provide a test mode (test = 1 and onosc = 1), clock = not (xin).

The Atmel Power-on-reset cell is dedicated to reset the internal circuit at power up and when the battery falls low.

Table 14 gives available oscillator and POR cells.

Table 14. Oscillator and POR Cells

Cell Name	Description
osc33k	Low-power, optimized for 32.786 kHz crystal
osc16m	16 MHz crystal oscillator
osc27m	27 MHz crystal oscillator
GNDYPOR	Ground pad for periphery with power on reset. Static and dynamic reset with internal hysteresis.

Phase Locked Loops

The Atmel PLLs are systems designed for synchronizing an internal chip clock with an input reference clock or multiplicating an input reference clock. Table 15 gives available phase locked loop cells.

Table 15. Phase Locked Loop Cells

Cell Name	Description
pll020m1	5 - 20 MHz single-pad phase locked loop
pll080m1	20 - 80 MHz single-pad phase locked loop
pll220m1	80 - 220 MHz single-pad phase locked loop

Basic Analog Cell Library AnaLib

The Atmel CBIC Analog Library makes the following parts available:

- Multiplexer modules
  - Multiplexers to minimize cross-talk (for use with high-impedance nodes).
  - Multiplexers to minimize ON resistance.
- Analog input and output cells
- Analog power and ground cells

General-purpose Analog Library GPlib

The General-purpose Analog Cell Library is composed of cells performing various analog functions.

Currently available are regulators, power management cells, op amps, comparators, low-speed ADCs and DACs.

Atmel Compiled Megacell Library

The Atmel Compiled Megacell Library enables compilation of megacells for the functions ARAM (Advanced Random Access Memory), Dual-Port RAM, FIFO (First In First Out), ROM, and LROM (Large ROM) according to the user's precise requirements.

The Atmel megacells can be instanced as often as required in designs and can be used in parallel with cells from all other Atmel CBIC libraries. All the megacell representations required for schematic entry, simulation, layout generation, place and route, and verification are created automatically.

The Built-In Self-Test (BIST) option, in terms of a netlist of standard cells surrounding the megacell, is supported for all megacells except the LROM (in this release).

FIFO and FIFO with BIST are available through the Cgenerate as netlists of standard cells surrounding a Dual-Port RAM Megacell.

Compiled ARAM Megacells

The Atmel ARAM compiler builds Clocked Embedded Self-timed Static RAMs from a set of input parameters, for example, the number of words and the word width. The Atmel ARAM generator is capable of creating many different sizes of RAM. In addition, for any given size, many configurations are possible. The differences in these configurations can be found in the aspect ratio and in performances.

The range of permitted ARAM megacell configurations is as follows:

```
Max number of bits   256K bits
Number of words      64, .. 32768   multiples of 32
Number of rows        32, .. 256    multiples of 16
Number of columns per bit   2, 4, 8
(words per row per block)
Number of blocks            1, 2, 4, 8, 16
Number of bits in a word:
if no. of blocks = 1   1, .. 128 increment of 1
if no. of blocks > 1   4, .. 32 if no. of columns per bit = 2
                       2, .. 16 if no. of columns per bit = 4
                       1, .. 8 if no. of columns per bit = 8
```

The following table lists all ARAM inputs and outputs and their pin capacitances.

Pin Name	Comment	Capacitance (pF)
ME	Clock (Trigger) Input	0.014
WE_	(Read)(Write not) Input	0.086
ADD<i>	Address Input	0.084
DI<j>	Data Input	0.019
DO<j>	Data Output	2.50 (max load)
VDD	Supply	
GND	Ground	

The following tables show the range of performances for particular ARAM configurations without BIST and without C_{Load}. Access time (t_{ACC}) and cycle time (t_{CYC}) refer to Max industrial conditions, whereas Dynamic Power dissipation refers to typical conditions.

Word Size = 8								
Word Depth	256	512	1K	2K	4K	8K	16K	32K
Width (mm)	0.264	0.430	0.430	1.514	1.514	2.844	5.607	5.607
Height (mm)	0.609	0.634	1.078	0.647	1.091	1.097	1.097	1.984
Access Time (t_{ACC}) (nsec)	5.53	5.78	6.52	7.08	7.81	8.62	9.36	10.83
Cycle Time (t_{CYC}) (nsec)	5.53	5.78	6.74	7.08	8.26	9.10	9.74	12.68
Dynamic Power (mW/MHz)	0.20	0.33	0.43	0.29	0.37	0.64	0.84	0.96

Word Size = 16								
Word Depth	128	256	512	1K	2K	4K	8K	16K
Width (mm)	0.430	0.430	0.765	0.765	2.852	2.852	5.607	5.607
Height (mm)	0.387	0.609	0.634	1.078	0.647	1.091	1.091	1.978
Access Time (t_{ACC}) (nsec)	5.33	5.70	5.95	6.69	8.38	9.11	9.86	11.33
Cycle Time (t_{CYC}) (nsec)	5.33	5.70	5.95	6.94	8.38	9.54	10.18	13.12
Dynamic Power (mW/MHz)	0.26	0.39	0.66	0.85	0.63	0.79	1.08	1.22

Compiled Dual-Port RAM Megacells

The Atmel Dual-Port RAM is a read/write memory that allows access to and from its memory cells by two independent ports (identified as Port A and Port B). There are no constraints on the timing of the ports relative to each other except in the case of address contention. Although the ports are constructed from the same circuitry, the possible I/O configurations are different:

- Port A may be selected with read/write or read-only capability
- Port B can have read/write or write-only capability

The two ports may have different wordlengths, provided that the ratio is an integral power of 2 (1, 2, 4, 8, 16, 32 or 64). The product (wordlength x address space) must be the same for the two ports.

The memory cell corresponds to a standard full CMOS six-transistor cell with the benefit of extremely low standby power dissipation. (There are actually eight or ten transistors per cell, according to the configuration of the port A).

Dual-Port RAM operates in single-edge clock controlled mode during read operations, and a double-edge controlled mode during write operations. Addresses are clocked internally on the rising edge of the clock signal (ME). Any change of address without rising edge of ME is not considered.

In read mode, the rising clock edge triggers a data read without any significant constraint on the length of the ME pulse. In write mode, data applied to the inputs is latched on the falling edge of ME or the rising edge of WE_, whichever comes earlier, and is then written in memory.

The range of permitted Dual-Port RAM Megacell configurations is as follows:

```
Number of rows:  4, ...128
Number of cols:  2, ...128
Number of words: 8, ...16384
Bits per word:   1, ...64
Total size:      8, ...16384
Port A configuration:  read/write, read-only
Port B configuration:  read/write, write-only
```

The following table lists all DPR inputs and outputs and their pin capacitances. Pin names are suffixed with the port nature A or B:

Pin Name	Comment	Capacitance (pF)
ME	Clock Input	0.020
WE_	Write Enable Input	0.013
ADD<i>	Address Input	0.018
DI<j>	Data Input	0.012
DO<j>	Data Output	3.55 (max load)
VDD	Supply	
GND	Ground	

The following tables show the range of performances for particular Dual Port RAM configurations, without BIST and without output load. Access time (t_{ACC}) and cycle time (t_{CYC}) refer to Max industrial conditions, whereas Dynamic Power dissipation refers to typical conditions. All examples have the same configuration for both port A and port B, with Read/Write capability.

Word Size = 8					
Word Depth	128	256	512	1K	2K
Rows x Columns	32 x 32	64 x 32	64 x 64	128 x 64	128 x 128
Width (mm)	0.416	0.422	0.685	0.702	1.228
Height (mm)	0.384	0.615	0.620	1.082	1.087
Access Time (t_{ACC}) (nsec)	3.30	3.68	4.06	4.81	5.55
Cycle Time (t_{CYC}) (nsec)	5.89	6.41	6.92	7.43	7.95
Dynamic Power (mW/MHz)	0.31	0.46	0.81	1.36	2.59

Word Size = 16					
Word Depth	64	128	256	512	1K
Rows x Columns	32 x 32	64 x 32	64 x 64	128 x 64	128 x 128
Width (mm)	0.416	0.422	0.685	0.702	1.228
Height (mm)	0.387	0.618	0.614	1.076	1.081
Access Time (t_{ACC}) (nsec)	3.27	3.65	3.98	4.72	5.36
Cycle Time (t_{CYC})(nsec)	5.38	6.01	6.41	6.92	7.43
Dynamic Power (mW/MHz)	0.32	0.46	0.82	1.37	2.6

Compiled FIFO Megacells

A compiled FIFO (first-in first-out data flow) megacell is implemented as a soft macro built around a Dual-Port RAM.

The compiled FIFO is a buffer memory that allows access to its memory cells by two independent ports. The read port is referred to as port A, the write port is labelled port B. Both ports are controlled by independent clock signals and contain address counters which are incremented during every clock cycle.

The FIFO block makes use of a compiled Dual-Port RAM with the configuration port A read-only and port B write-only.

```
Number of rows:  2, ...128 in increments of 2
Number of words: 8, 16, 32, ...16384
Bits per word:   1, ...64
Total size:      8, ...16384
```

The word lengths of both ports may be different, but their ratio must be one of (1, 2, 4, 8, 16, 32 or 64).

The following is a list of pins which will be found on the symbol of a module:

- CKOUT is the clock input for port A (read port).
- CKIN is the clock input for port B (write port).
- DIN<0:i-1> Data input lines.
- DOUT<0:i-1> Data output lines.
- RESETZ The clear signal.
- EMPTY The empty flag.
- FULL The full flag.
- Supply (VDD) and ground (GND).

The following table shows the estimated range of performance for particular FIFO configurations, without BIST, and without output load. Access time (t_{ACC}) and cycle time (t_{CYC}) refer to Max industrial conditions, whereas Dynamic Power dissipation refers to typical conditions. All examples have the same configuration for both port A and port B, with Read/Write capability. There is no additional flag.

Word Size	**4**	**8**	**16**	**32**	**64**
Word Depth	16	32	64	128	256
Rows x Columns	8 x 8	16 x 16	32 x 32	64 x 64	128 x 128
Width (mm)	0.235	0.307	0.455	0.724	1.267
Height (mm)	0.169	0.227	0.342	0.573	1.035
Access Time (t_{ACC}) (nsec)	2.72	2.91	3.27	3.97	5.37
Cycle Time (t_{CYC}) (nsec)	4.55	4.86	5.38	5.89	7.56
Dynamic Power (mW/MHz)	0.10	0.15	0.31	0.80	2.58

Compiled ROM Megacells

Compiled memories are diffusion-programmed ROMs with a synchronous access protocol. The generated ROM Megacell is a single edge control ROM. Rising edge of the memory enable signal (ME) latches the addresses and starts the read operation.

The internal idle state of the memory plane is the precharge state. The next clock cycle can start with the next ME rising edge, once the precharge is complete.

The generator takes care of complementing the required address space to the nearest physical size possible in case of number of words being not equal to an integral power of two.

The range of permitted ROM configurations is as follows :

```
Number of words:         9...16384
Number of Address Bits:  4...14
Bits per words:          1...128
Total size:              9...131072  (128K)
Number of Columns:       4...512
Number of Rows:          4...256
```

The memory plane is organized in multiples of 4 rows, and multiples of 4, 8, 16, 32 or 64 columns.

The following table lists all ROM inputs and outputs and their pin capacitances:

Pin Name	Comment	Capacitance (pF)
ME	Clock Input	0.029
OE	Output Enable Input	0.007
ADD<i>	Address Input	0.010
DO<j>	Data Output	0.016 (if tristate)
		3.20 (max load)

The following tables show the range of performances for particular ROM configurations.

Access time (t_{ACC}) and cycle time (t_{CYC}) refer to Max industrial conditions, whereas Dynamic Power dissipation refers to typical conditions.

Word Size = 8							
Word Depth	16	32	64	128	256	512	1K
Width (mm)	0.234	0.234	0.234	0.234	0.297	0.297	0.423
Height (mm)	0.158	0.164	0.177	0.203	0.203	0.254	0.254
Access Time (t_{ACC}) (nsec)	3.62	3.66	3.73	3.89	3.93	4.23	3.66
Cycle Time (t_{CYC}) (nsec)	5.88	5.91	5.99	6.14	6.18	6.48	6.56
Dynamic Power (mW/MHz)	0.20	0.21	0.21	0.22	0.24	0.28	0.35

Word Size = 16							
Word Depth	16	32	64	128	256	512	1K
Width (mm)	0.297	0.297	0.297	0.297	0.297	0.423	0.423
Height (mm)	0.158	0.164	0.177	0.203	0.254	0.254	0.357
Access Time (t_{ACC}) (nsec)	3.66	3.70	3.77	3.93	4.23	4.31	4.92
Cycle Time (t_{CYC}) (nsec)	5.95	5.99	6.06	6.21	6.51	6.59	7.19
Dynamic Power (mW/MHz)	0.34	0.35	0.35	0.37	0.41	0.48	0.63

Compiled LROM Megacells

The LROM (Large ROM) compiler allows the system designer to acheive high-density and low-power applications. Multi-block megacells with total capacity up to 4M-bits can be generated by the LROM compiler.

Compiled memories are diffusion-programmed ROMs with a synchronous access protocol, as is for the ROM. The compiler expects a programming file: lrom<xyz>.prg that contains the LROM pattern. If the .prg file is not available, a random contents is automatically generated. Unlike the ROM compiler, only buffered outputs can be acheived using the LROM compiler.

The range of permitted LROM configurations is as follows:

```
Total size:      64K...4M
Number of words: 2K...512K
Bits per word:   8, 16 or 32
Number of address bits:11...19
The memory is organized in multiple blocks of 64K bits each.
Number of blocks:           1...32
Number of rows per block:   256
Number of columns per block:256
```

I/O pins in compiled megacells are the following:

me input: Memory Enable.

add<i> inputs: Address.

do<i> outputs: buffered output data.

vdd and gnd: power and ground supplies.

The following table shows the performances for some LROM configurations. Access time (t_{ACC}), cycle time (t_{CYC}) and Dynamic Power dissipation refer to Max industrial conditions.

Word Size = 16				
Word Depth	16K	32K	64K	128K
Width (mm)	0.979	3.570	1.863	1.863
Height (mm)	0.858	0.539	1.716	3.078
Access Time (t_{ACC}) (nsec)	11.37	11.84	12.53	15.19
Cycle Time (t_{CYC}) (nsec)	14.15	14.40	15.30	19.14
Dynamic Power (mW/MHz)	0.26	0.56	0.75	0.90

Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 487-2600

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
TEL (41) 26-426-5555
FAX (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
TEL (33) 2-40-18-18-18
FAX (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
TEL (33) 4-42-53-60-00
FAX (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
TEL (44) 1355-803-000
FAX (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
TEL (49) 71-31-67-0
FAX (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
TEL (33) 4-76-58-30-00
FAX (33) 4-76-58-34-80

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

1063CS–CBIC–01/03 0M