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## Appendix B - ATmega88 Automotive Specification at 1.8V

This document contains information specific to devices operating at voltage between 1.8V and 5.5V. Only deviations with standard operating characteristics are covered in this appendix, all other information can be found in the complete Automotive datasheet. The complete ATmega88 automotive datasheet can be found on [www.atmel.com](http://www.atmel.com)



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**8-bit AVR<sup>®</sup>  
Microcontroller  
with 8K Bytes  
In-System  
Programmable  
Flash**

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**ATmega88  
Automotive**

**Appendix B**

7738C-AVR-11/09



## 1. Electrical Characteristics

### 1.1 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Test Conditions	Unit
Operating Temperature	-55 to +150	°C
Storage Temperature	-65 to +175	°C
Voltage on any Pin except $\overline{\text{RESET}}$ with respect to Ground	-0.5 to $V_{CC}+0.5$	V
Voltage on $\overline{\text{RESET}}$ with respect to Ground	-0.5 to +13.0	V
Maximum Operating Voltage	6.0	V
DC Current per I/O Pin	30	mA
DC Current $V_{CC}$ and GND	200.0	

### 1.2 DC Characteristics

$T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 1.8\text{V}$  to  $5.5\text{V}$  (unless otherwise noted)

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Input Low Voltage, except XTAL1 and $\overline{\text{RESET}}$ pin	$V_{CC} = 1.8\text{V}$ to $5.5\text{V}$	$V_{IL}$	-0.5		$0.1V_{CC}^{(1)}$	V
Input High Voltage, except XTAL1 and $\overline{\text{RESET}}$ pins	$V_{CC} = 1.8\text{V}$ to $5.5\text{V}$	$V_{IH}$	$0.75V_{CC}^{(2)}$		$V_{CC} + 0.5$	V
Input Low Voltage, XTAL1 pin	$V_{CC} = 1.8\text{V}$ to $5.5\text{V}$	$V_{IL1}$	-0.5		$+0.1V_{CC}^{(1)}$	V
Input High Voltage, XTAL1 pin	$V_{CC} = 1.8\text{V}$ to $5.5\text{V}$	$V_{IH1}$	$0.9V_{CC}^{(2)}$		$V_{CC} + 0.5$	V
Input Low Voltage, $\overline{\text{RESET}}$ pin	$V_{CC} = 1.8\text{V}$ to $5.5\text{V}$	$V_{IL2}$	-0.5		$+0.1V_{CC}^{(1)}$	V
Input High Voltage, $\overline{\text{RESET}}$ pin	$V_{CC} = 1.8\text{V}$ to $5.5\text{V}$	$V_{IH2}$	$0.9V_{CC}^{(2)}$		$V_{CC} + 0.5$	V
Input Low Voltage, $\overline{\text{RESET}}$ pin as I/O	$V_{CC} = 1.8\text{V}$ to $5.5\text{V}$	$V_{IL3}$	-0.5		$+0.1V_{CC}^{(1)}$	V
Input High Voltage, $\overline{\text{RESET}}$ pin as I/O	$V_{CC} = 1.8\text{V}$ to $5.5\text{V}$	$V_{IH3}$	$0.6V_{CC}^{(2)}$		$0.7V_{CC}$	V

- Notes:
- “Max” means the highest value where the pin is guaranteed to be read as low
  - “Min” means the lowest value where the pin is guaranteed to be read as high
  - Although each I/O port can sink more than the test conditions (0.5 mA at  $V_{CC} = 1.8\text{V}$ ) under steady state conditions (non-transient), the following must be observed:
    - The sum of all IOL, for ports B0 - B5, should not exceed 50 mA.  
If IOL exceeds the test condition, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test condition.
  - Although each I/O port can source more than the test conditions (0.5 mA at  $V_{CC} = 1.8\text{V}$ ) under steady state conditions (non-transient), the following must be observed:
    - The sum of all IOH, for ports B0 - B5 should not exceed 50 mA.  
If IOH exceeds the test condition, VOH may exceed the related specification. Pins are not guaranteed to source current greater than the listed test condition.
  - Minimum  $V_{CC}$  for Power-down is 2.5V.

## 1.2 DC Characteristics (Continued)

$T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 1.8\text{V}$  to  $5.5\text{V}$  (unless otherwise noted) (Continued)

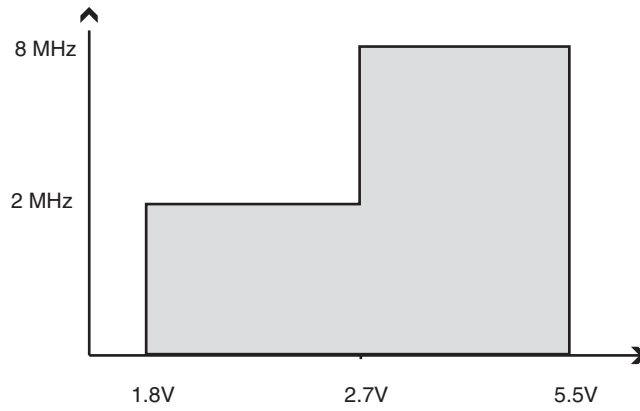
Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Output Low Voltage <sup>(3)</sup> , I/O pin except RESET	$I_{OL} = 0.5\text{ mA}$ , $V_{CC} = 1.8\text{V}$	$V_{OL}$			0.25	V
Output High Voltage <sup>(4)</sup> , I/O pin except RESET	$I_{OH} = -0.5\text{ mA}$ , $V_{CC} = 1.8\text{V}$	$V_{OH}$	1.25			V
Input Leakage Current I/O Pin	$V_{CC} = 5.5\text{V}$ , pin low (absolute value)	$I_{IL}$			1	$\mu\text{A}$
Input Leakage Current I/O Pin	$V_{CC} = 5.5\text{V}$ , pin high (absolute value)	$I_{IH}$			1	$\mu\text{A}$
Reset Pull-up Resistor		$R_{RST}$	30		60	$\text{k}\Omega$
I/O Pin Pull-up Resistor		$R_{PU}$	20		50	$\text{k}\Omega$
Power Supply Current <sup>(5)</sup>	Active 2 MHz, $V_{CC} = 1.8\text{V}$	$I_{CC}$		0.8	1.2	$\text{mA}$
	Idle 2 MHz, $V_{CC} = 1.8\text{V}$			0.2	0.4	$\text{mA}$
Power-down mode	WDT disabled, $V_{CC} = 1.8\text{V}$ WDT enabled, $V_{CC} = 1.8\text{V}$			0.2 4	18 24	$\mu\text{A}$
Analog Comparator Input Offset Voltage	$V_{CC} = 2.7\text{V}$ $V_{in} = V_{CC}/2$	$V_{ACIO}$		<10	40	$\text{mV}$
Analog Comparator Input Leakage Current	$V_{CC} = 2.7\text{V}$ $V_{in} = V_{CC}/2$	$I_{ACLK}$	-50		+50	$\text{nA}$
Analog Comparator Propagation Delay	$V_{CC} = 2.7\text{V}$	$t_{ACPD}$		500		$\text{ns}$

- Notes:
1. "Max" means the highest value where the pin is guaranteed to be read as low
  2. "Min" means the lowest value where the pin is guaranteed to be read as high
  3. Although each I/O port can sink more than the test conditions (0.5 mA at  $V_{CC} = 1.8\text{V}$ ) under steady state conditions (non-transient), the following must be observed:
    - 1] The sum of all  $I_{OL}$ , for ports B0 - B5, should not exceed 50 mA.  
If  $I_{OL}$  exceeds the test condition,  $V_{OL}$  may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test condition.
  4. Although each I/O port can source more than the test conditions (0.5 mA at  $V_{CC} = 1.8\text{V}$ ) under steady state conditions (non-transient), the following must be observed:
    - 1] The sum of all  $I_{OH}$ , for ports B0 - B5 should not exceed 50 mA.  
If  $I_{OH}$  exceeds the test condition,  $V_{OH}$  may exceed the related specification. Pins are not guaranteed to source current greater than the listed test condition.
  5. Minimum  $V_{CC}$  for Power-down is 2.5V.

### 1.3 Maximum Speed versus $V_{CC}$

Maximum frequency is dependent on  $V_{CC}$ .

**Figure 1-1.** Maximum Frequency versus  $V_{CC}$



## 1.4 ADC Characteristics

$T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 1.8\text{V}$  to  $5.5\text{V}$  (unless otherwise noted)

Parameters	Test Conditions	Symbol	Min	Typ	Max	Unit
Resolution	$-40^\circ\text{C}$ to $+85^\circ\text{C}$ - 1.8V to 2.7V ADC clock = 125 kHz			10		Bits
	$-40^\circ\text{C}$ to $+85^\circ\text{C}$ - 2.7V to 5.5V ADC clock = 200 kHz			10		Bits
Absolute accuracy	$V_{CC} = 1.8\text{V}$ , $V_{Ref} = 1.8\text{V}$	TUE		2.2	3.5	LSB
	$V_{CC} = 4.0\text{V}$ , $V_{Ref} = 4.0\text{V}$			2.1	3.5	LSB
Integral Non Linearity	$V_{CC} = 1.8\text{V}$ , $V_{Ref} = 1.8\text{V}$	INL		0.6	2.0	LSB
	$V_{CC} = 4.0\text{V}$ , $V_{Ref} = 4.0\text{V}$			0.5	1.5	LSB
Differential Non Linearity	$V_{CC} = 1.8\text{V}$ , $V_{Ref} = 1.8\text{V}$	DNL		0.4	1.0	LSB
	$V_{CC} = 4.0\text{V}$ , $V_{Ref} = 4.0\text{V}$			0.3	0.7	LSB
Gain error			-3.5	-1.5	3.5	LSB
Offset error			-3.5	2.0	3.5	LSB
Clock frequency	$V_{CC} = 1.8\text{V}$ to $2.7\text{V}$		50		125	kHz
	$V_{CC} = 2.7\text{V}$ to $5.5\text{V}$		50		200	kHz
Analog Supply Voltage		$A_{V_{CC}}$	$V_{CC} - 0.3$		$V_{CC} + 0.3$	V
Reference Voltage		$V_{REF}$	1.0		$A_{V_{CC}}$	V
Input Voltage		$V_{IN}$	GND		$V_{REF} - 50\text{mV}$	V
Input Bandwidth				38.5		kHz
Internal Voltage Reference		$V_{INT}$	1.0	1.1	1.2	V
Reference Input Resistance		$R_{REF}$	22.4	32	41.6	k $\Omega$
Analog Input Resistance		$R_{AIN}$		100		M $\Omega$

## 2. Ordering Information

**Table 2-1.** ATmega88

Speed (MHz)	Power Supply	ISP Flash	Ordering Code	Package	Operation Range
2-8	1.8V to 5.5V	8 KB	ATmega88V-15MT	PN	Automotive (−40°C to +85°C)
2-8	1.8V to 5.5V	8 KB	ATmega88V-15AT	MA	Automotive (−40°C to +85°C)

## 3. Package Information

**Table 3-1.** Package Types

Package Type	
<b>PN</b>	32-pad, 5 × 5 × 1.0 mm body, lead pitch 0.50 mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF): E2/D2 3.1 ±0.1 mm
<b>MA</b>	MA, 32 - Lead, 7 × 7 mm Body Size, 1.0 mm Body Thickness 0.5 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)

Figure 3-1. PN

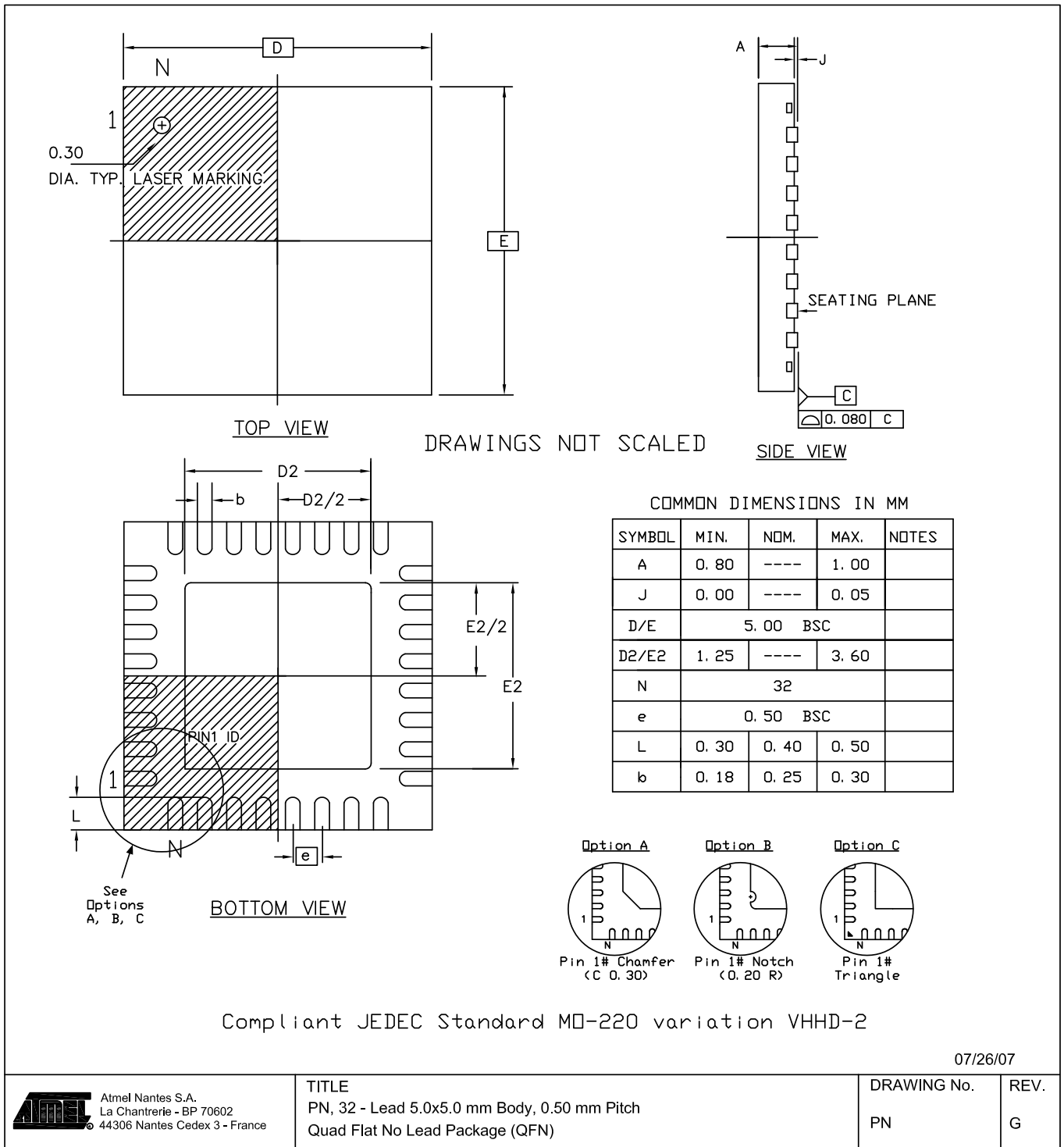
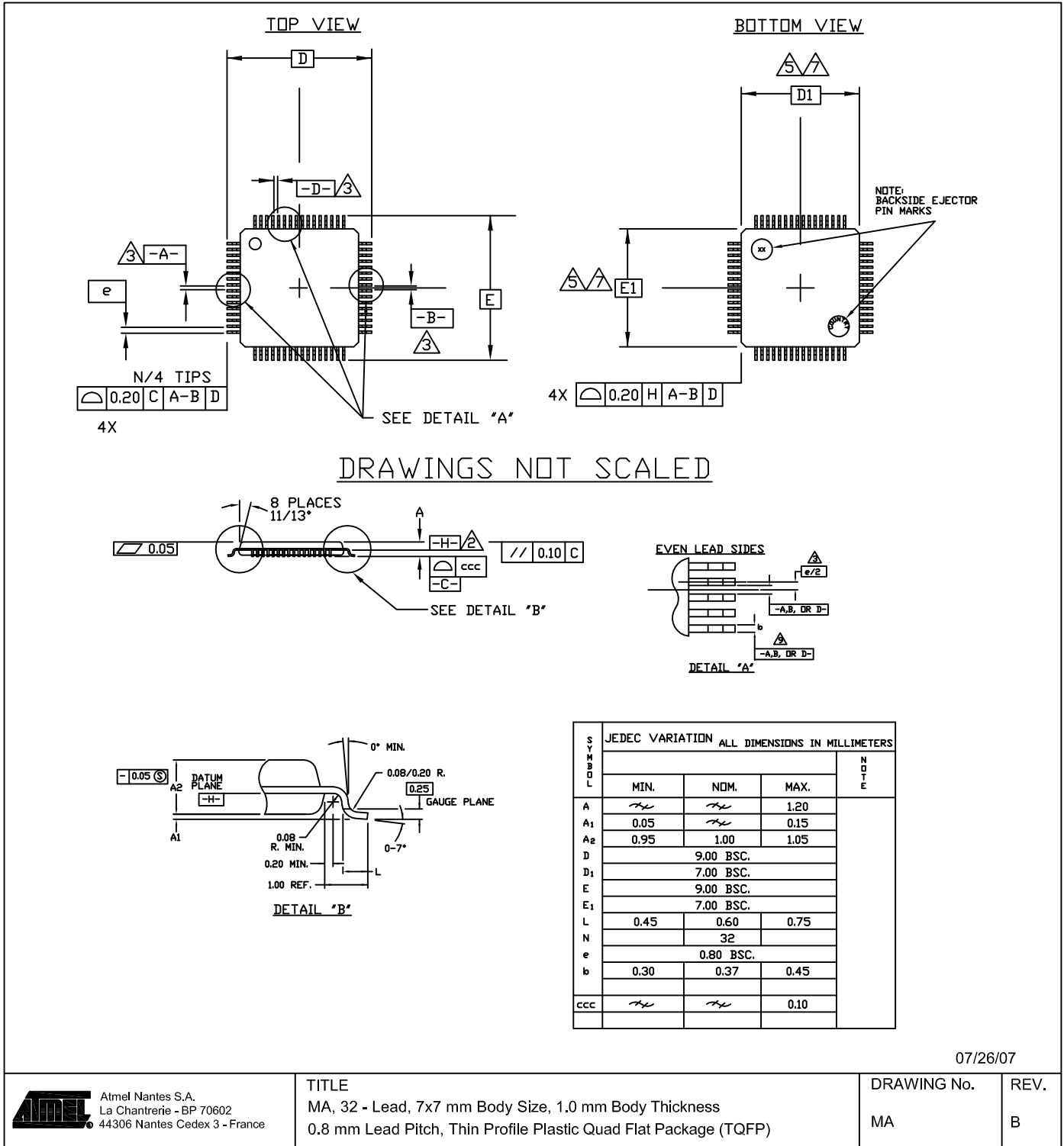


Figure 3-2. MA





## 4. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
7738C-AVR-11/09	<ul style="list-style-type: none"><li>• ADC specification updates</li></ul>
7738B-AVR-07/09	<ul style="list-style-type: none"><li>• Package MA updated</li></ul>
7738A-AVR-07/07	<ul style="list-style-type: none"><li>• Document Creation</li></ul>



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