DATA SHEET

AU2902
Low power quad operational amplifier

Product data
Supersedes data of 1994 Aug 31
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Low power quad operational amplifier AU2902

DESCRIPTION

The AU2902 consists of four independent, high-gain, internally frequency-compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages.

UNIQUE FEATURES

In the linear mode, the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

The unity gain crossover frequency and the input bias current are temperature-compensated.

FEATURES

- Internally frequency-compensated for unity gain
- Large DC voltage gain: 100 dB
- Wide bandwidth (unity gain): 1 MHz (temperature-compensated)
- Wide power supply range Single supply: 3 V_{DC} to 30 V_{DC} or dual supplies: ±1.5 V_{DC} to ±15 V_{DC}
- Very low supply current drain: essentially independent of supply voltage (1 mW/op amp at +5 V_{DC})
- Low input bias current: 45 nA_{DC} (temperature-compensated)
- Low input offset voltage: 2 mV_{DC} and offset current: 5nA_{DC}
- Differential input voltage range equal to the power supply voltage
- Large output voltage: 0 V_{DC} to V_{CC} – 1.5 V_{DC} swing

PIN CONFIGURATION

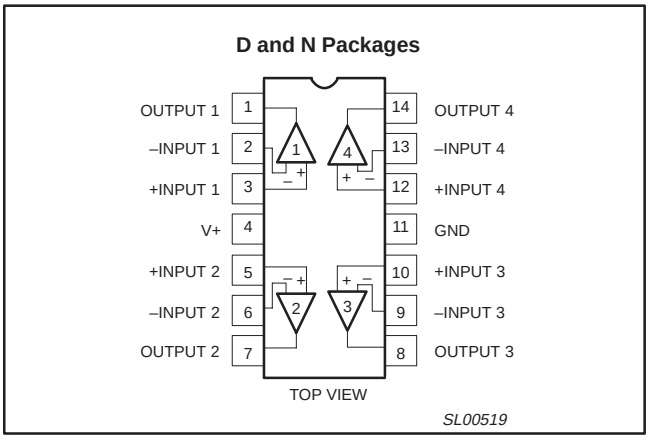


Figure 1. Pin Configuration

EQUIVALENT SCHEMATIC

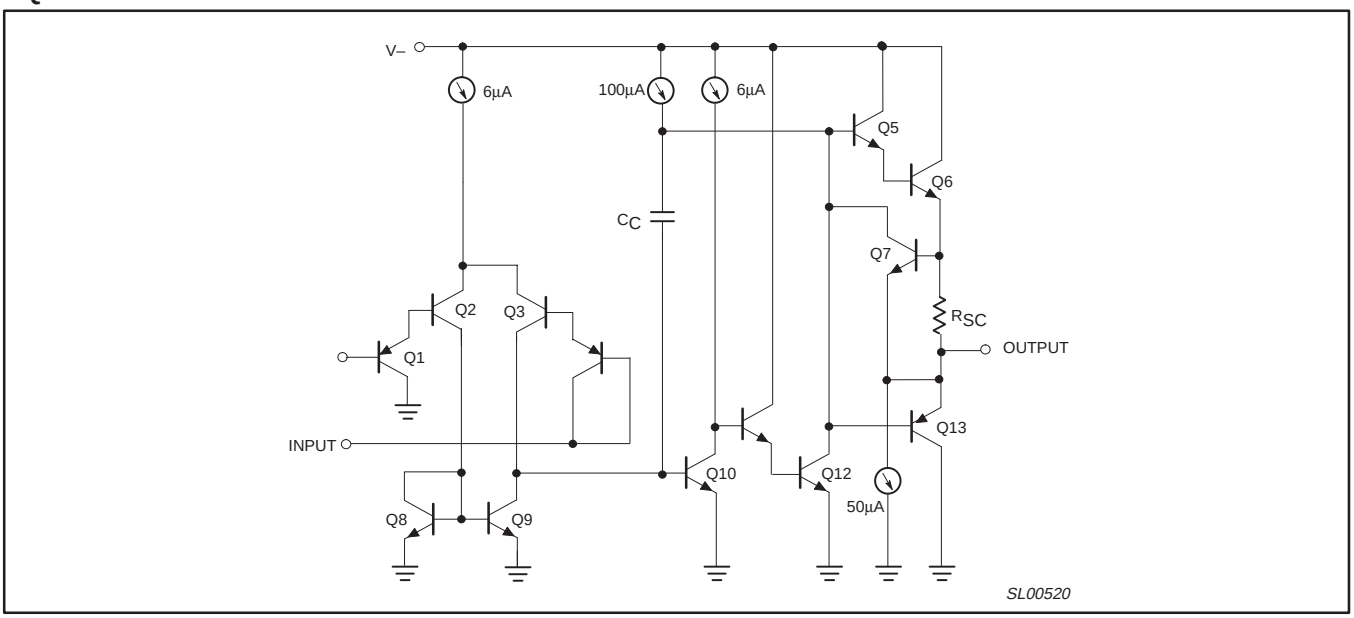


Figure 2. Equivalent Schematic

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Small Outline (SO) Package	–40 °C to +125 °C	AU2902D	SOT108-1
14-Pin Plastic Dual In-Line Package (DIP)	–40 °C to +125 °C	AU2902N	SOT27-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	32 or ±16	V_{DC}
V_{IN}	Differential input voltage	32	V_{DC}
V_{IN}	Input voltage	–0.3 to +32	V_{DC}
P_{DMAX}	Maximum power dissipation; T_{amb} = 25 °C (still-air)[1] N package D package	 1420 1040	 mW mW
	Output short-circuit to GND; one amplifier V_{CC} < 15 V_{DC} and T_{amb} = 25 °C	Continuous	
I_{IN}	Input current (V_{IN} < –0.3 V) [3]	50	mA
T_{amb}	Operating ambient temperature range	–40 to +125	°C
T_{stg}	Storage temperature range	–65 to +150	°C
T_{sld}	Lead soldering temperature (10 sec max)	230	°C

NOTES:

1. Derate above 25 °C at the following rates:
   N package at 11.4 mW/°C
   D package at 8.3 mW/°C
2. Short-circuits from the output to V_{CC}+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA, independent of the magnitude of V_{CC}. At values of supply voltage in excess of +15 V_{DC} continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input bias clamps. In addition, there is also lateral NPN parasitic transistor action on the IC chip. This action can cause the output voltages of the op amps to go to the V+ rail (or to ground for a large overdrive) during the time that the input is driven negative.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	AU2902			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage[1]	R_S = 0 Ω		±2	±3	mV
		R_S = 0 Ω, over temp.			±5	mV
$\Delta V_{OS}/\Delta T$	Temperature drift	R_S = 0 Ω, over temp.		7		µV/°C
I_{BIAS}	Input current[2]	$I_{IN}(+)$ or $I_{IN}(-)$		45	250	nA
		$I_{IN}(+)$ or $I_{IN}(-)$; over temp.		40	500	nA
$\Delta I_{BIAS}/\Delta T$	Temperature drift	Over temp.		50		pA/°C
I_{OS}	Offset current	$I_{IN}(+)-I_{IN}(-)$		±5	±50	nA
		$I_{IN}(+) - I_{IN}(-)$; over temp.			±150	nA
$\Delta I_{OS}/\Delta T$	Temperature drift	Over temp.		10		pA/°C
V_{CM}	Common-mode voltage range[3]	$V_{CC} \leq 30$ V	0		$V_{CC} - 1.5$	V
		$V_{CC} \leq 30$ V; over temp.	0		$V_{CC} - 2$	V
CMRR	Common-mode rejection ratio	V_{CC} = 30 V	65	70		dB
V_{OUT}	Output voltage swing	R_L = 2 kΩ; V_{CC} = 30 V; over temp.	26			V
V_{OH}	Output voltage high	$R_L \geq 10$ kΩ; V_{CC} = 30 V; over temp.	27	28		V
V_{OL}	Output voltage low	$R_L \leq 10$ kΩ; V_{CC} = 5 V; over temp.		5	20	mV
I_{CC}	Supply current	$R_L = \infty$; V_{CC} = 30 V; over temp.		1.5	3	mA
		$R_L = \infty$; V_{CC} = 5 V; over temp.		0.7	1.2	mA
A_{VOL}	Large-signal voltage gain	V_{CC} = 15 V (for large V_O swing); $R_L \geq 2$ kΩ	25	100		V/mV
		V_{CC} = 15V (for large V_O swing); $R_L \geq 2$ kΩ; over temp.	15			V/mV
	Amplifier-to-amplifier coupling[5]	f = 1 kHz to 20 kHz; input referred		–120		dB
PSRR	Power supply rejection ratio	R_S = 0 Ω	65	100		dB
I_{OUT}	Output current, Source	$V_{IN}+$ = +1 V; $V_{IN}-$ = 0 V; V_{CC} = 15 V	20	40		mA
		$V_{IN}+$ = +1 V; $V_{IN}-$ = 0 V; V_{CC} = 15 V; over temp.	10	20		mA
	Output current, Sink	$V_{IN}-$ = +1 V, $V_{IN}+$ = 0 V; V+ = 15 V	10	20		mA
		$V_{IN}-$ = +1 V; $V_{IN}+$ = 0 V; V_{CC} = 15 V; over temp.	5	8		mA
		$V_{IN}-$ = +1 V; $V_{IN}+$ = 0 V; V_O = 200 mV	12	50		µA
I_{SC}	Short–circuit current[4]		10	40	60	mA
V_{DIFF}	Differential input voltage[3]				V_{CC}	V
GBW	Unity gain bandwidth			1		MHz
SR	Slew rate			0.3		V/µs
V_{NOISE}	Input noise voltage	f = 1 kHz		40		nV/√Hz

NOTES:

1. $V_O \approx 1.4\ V_{DC}$, R_S = 0 Ω with V_{CC} from 5 V to 30 V and over full input common-mode range (0 V_{DC}+ to V_{CC} –1.5 V).
2. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V_{CC} –1.5, but either or both inputs can go to +32 V without damage.
4. Short-circuits from the output to V_{CC} can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA independent of the magnitude of V_{CC}. At values of supply voltage in excess of +15 V_{DC}, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
5. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of coupling increases at higher frequencies.

TYPICAL PERFORMANCE CHARACTERISTICS

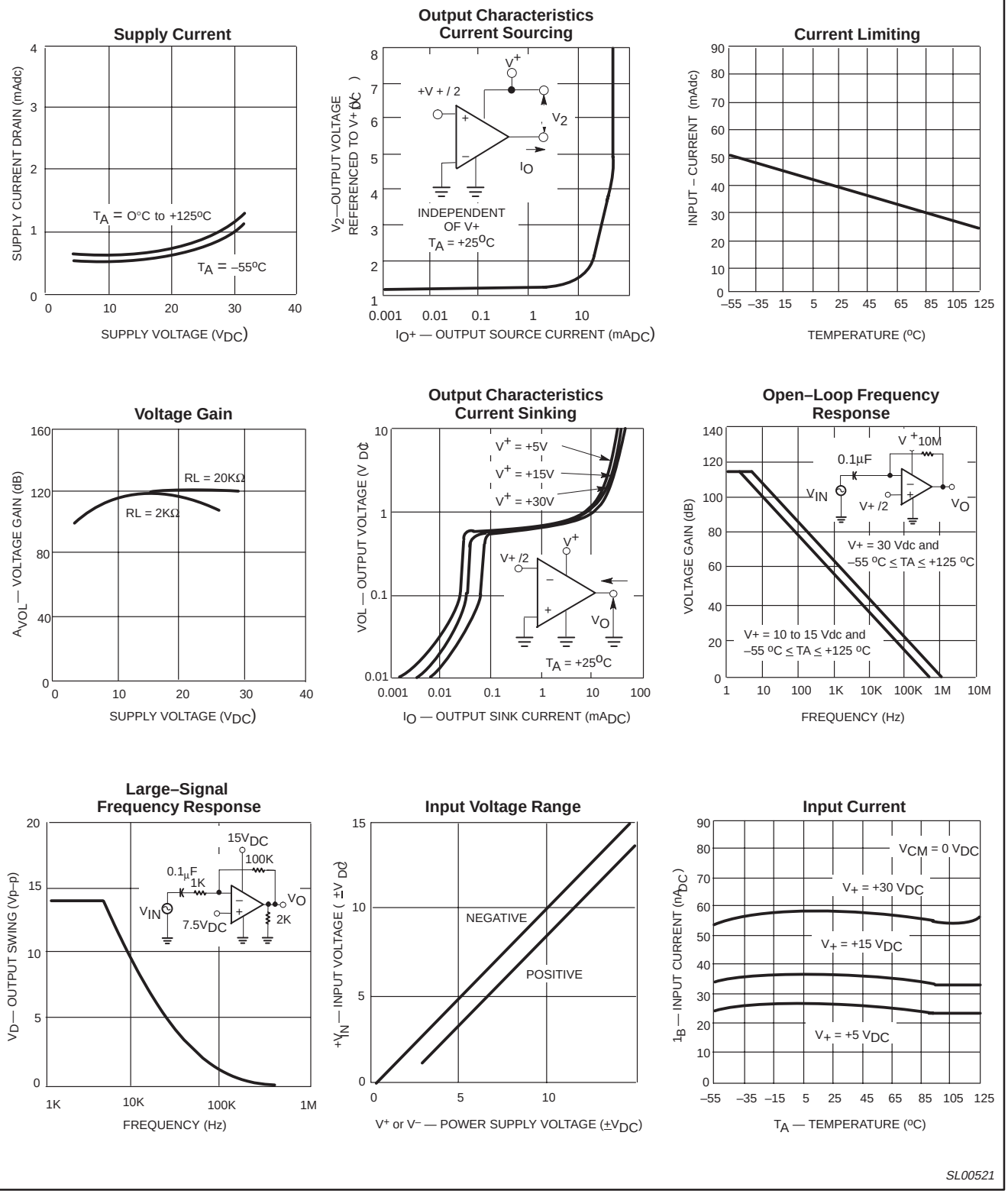


Figure 3. Typical Performance Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

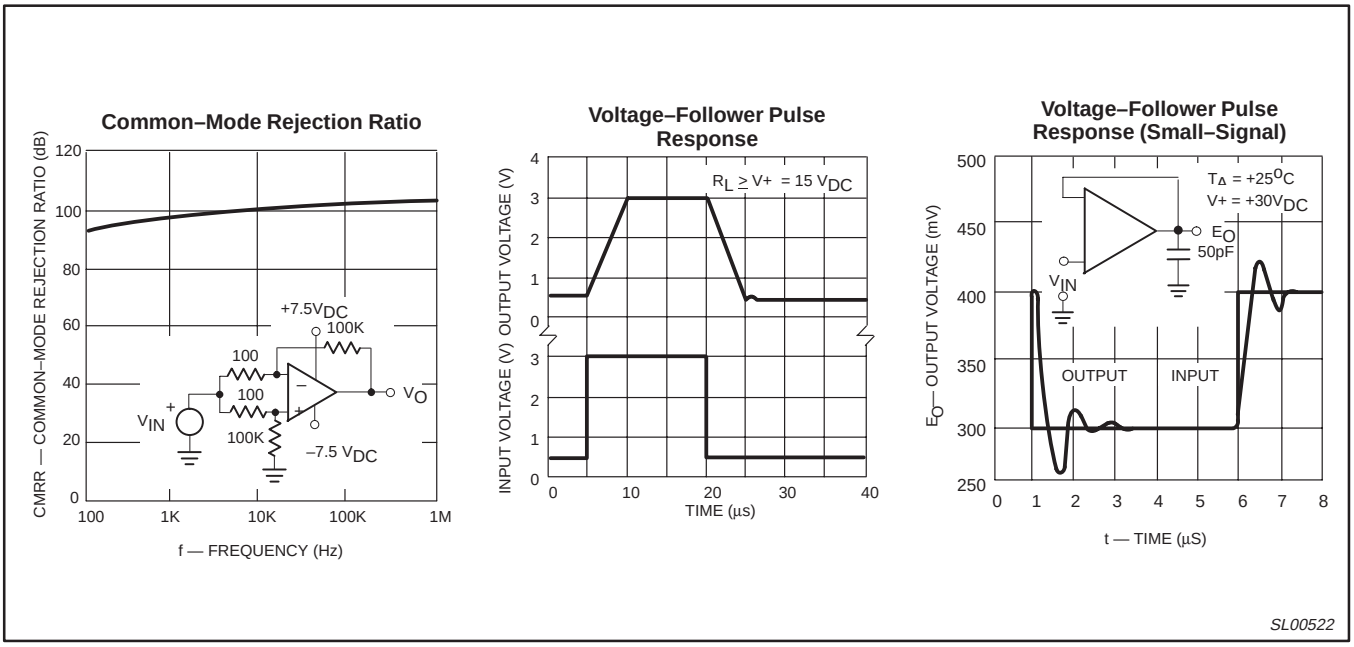


Figure 4. Typical Performance Characteristics (cont.)

TYPICAL APPLICATIONS

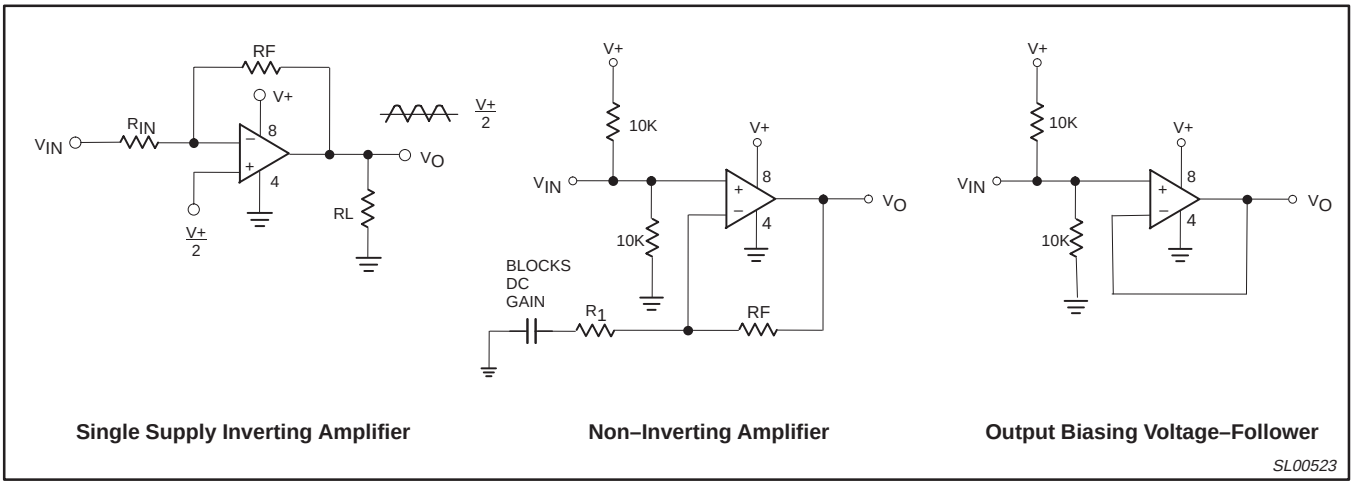
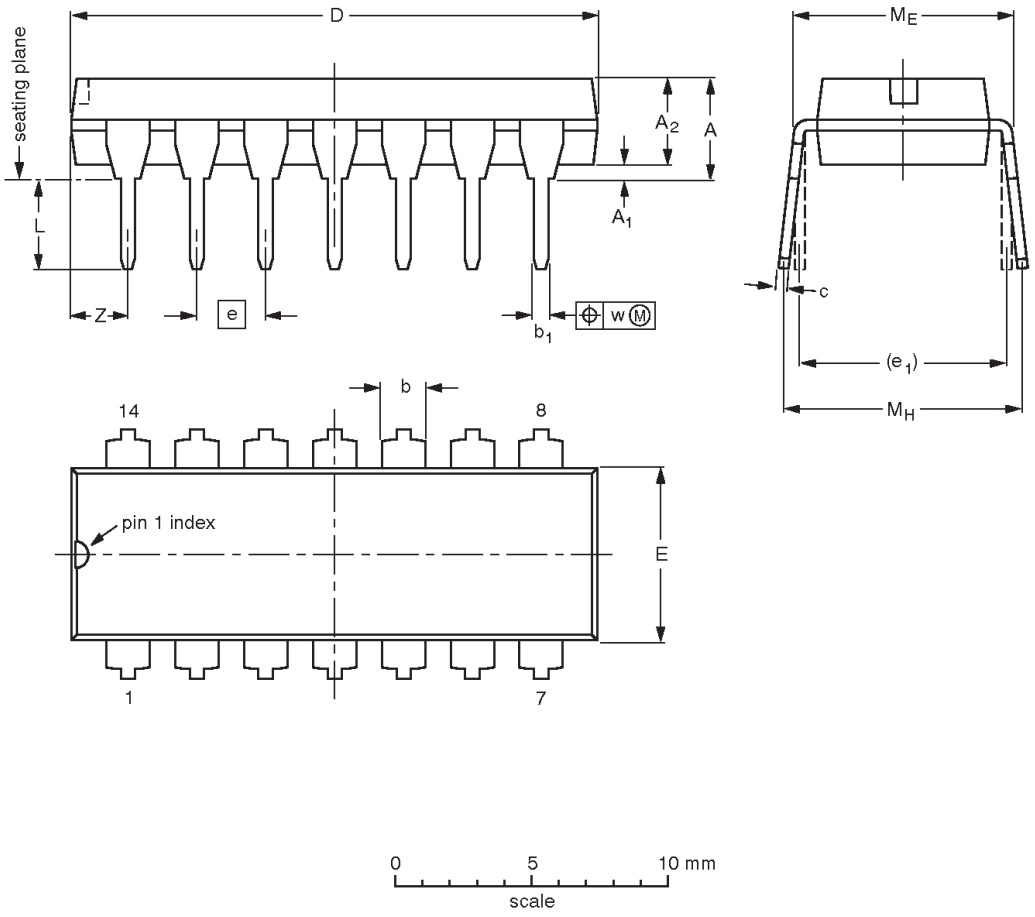


Figure 5. Typical Applications

DIP14: plastic dual in-line package; 14 leads (300 mil) **SOT27-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

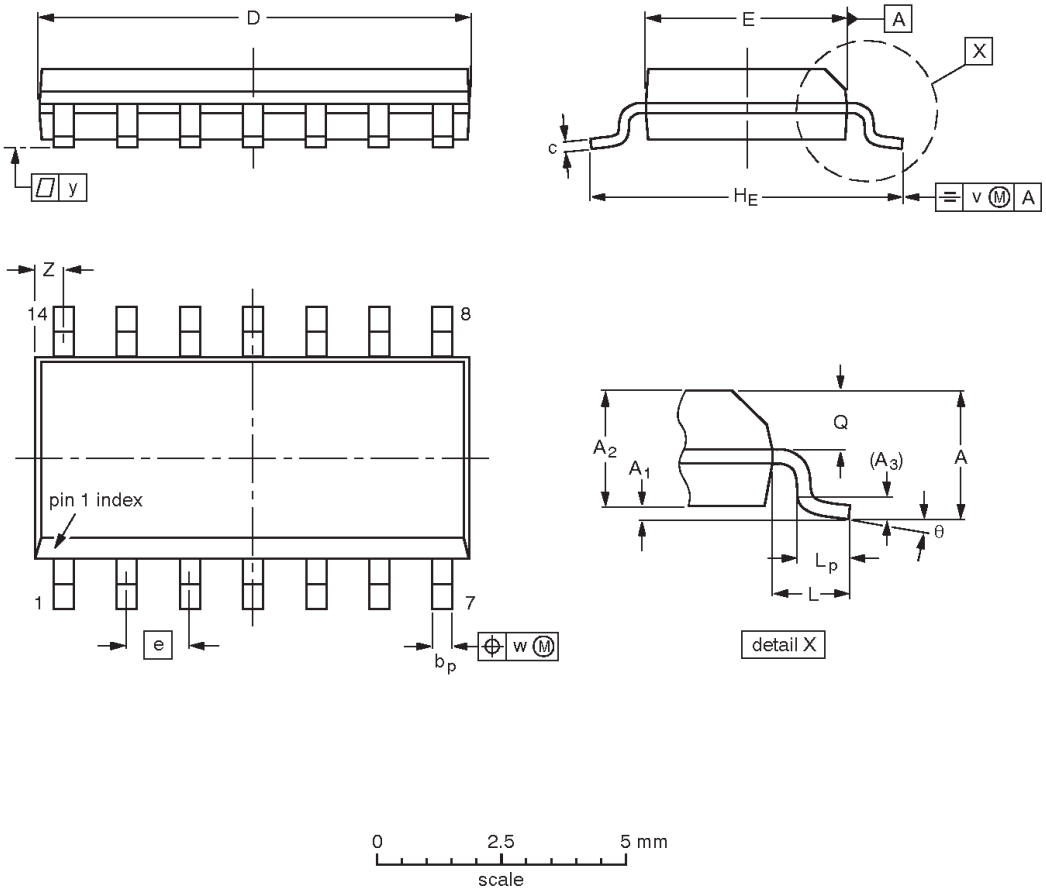
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001	SC-501-14			~~95-03-11~~ 99-12-27

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06	MS-012				~~97-05-22~~ 99-12-27

NOTES

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