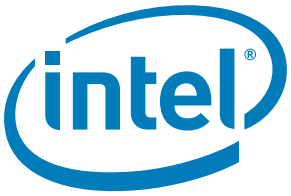


Intel® Atom™ Processor N400 & N500 Series

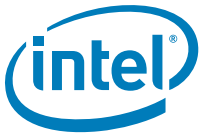
Datasheet - Volume 1

This is volume 1 of 2. Refer to Document Ref# 322848 for Volume 2.

June 2011

Revision 003

Document Number: 322847-003



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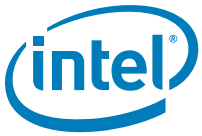

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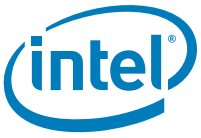
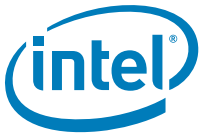
Tables





Revision History

Revision Number	Description	Revision Date
001	• Initial release	December 2009
002	• Updated Table 4-22: Added Icc data for Intel® Atom™ Processor N470 series as a new SKU • Updated Table 6-45: Added TDP data for Intel Atom Processor N470 as a new SKU	April 2010
003	• Inserted Intel® Atom™ N500 series information to Datasheet	June 2011

§

1 Introduction

The document provides DC electrical specifications, pinout and signal definitions, interface functional descriptions, and additional feature information pertinent to the implementation and operation of the processor on its respective platform.

Throughout this document, Intel® Atom™ Processor N400 Series is referred as the processor and Intel® NM10 Family Express Chipset is referred as the chipset.

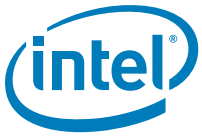
The processor is built on 45-nanometer Hi-K process technology. The processor is designed for a two-chip platform as opposed to the traditional three-chip platforms (processor, GMCH, and ICH). The two-chip platform consists of a processor and a chipset which enables better performance, lower cost, easier validation, and improved x-y footprint. The processor is offered in an BGA559 package.

Included in this family of processors is an integrated memory controller (IMC), integrated graphics processing unit (GPU) and integrated I/O (IIO) (such as DMI) on a single silicon die. This single die solution is known as a monolithic processor.

1.1 Processor Features

The following list provides some of the key features on this processor:

- On die, primary 32-kB instructions cache and 24-kB write-back data cache
- Intel® Hyper-Threading Technology (2 threads)
- On die 512-kB, 8-way L2 cache
- Support IA 32-bit and Intel® 64 architecture
- Intel® Streaming SIMD Extensions 2 and 3 (SSE2 and SSE3) and Supplemental Streaming SIMD Extensions 3 (SSSE3) support
- Micro-FCBGA8 packaging technologies
- Thermal management support via Intel® Thermal Monitor 1 (TM1) and Intel® Thermal Monitor 1 (TM2)
- Support C-state of C0/C1(E)/C2(E)/C4(E)
- Enhanced Intel® SpeedStep Technology (EIST)
- Support L2 dynamic cache sizing
- Execute Disable Bit support for enhanced security



1.2 Interfaces

1.2.1 System Memory Support

Support DDr2 SDRAMs (N450 and N470 support DDR2 only)

- One channel of DDR2 memory (consists of 64-bit of data lines):
  - — Maximum of two SO-DIMMs in Raw Card-A or Raw Card-C format
- Memory DDR2 data transfer rates of 667 MT/s
- I/O Voltage of 1.8 V for DDR2
- Non-ECC, unbuffered DDR2 SO-DIMMs only
- 512-Mb, 1-Gb and 2-Gb DDR2 DRAM technologies supported
- Maximum of 2-GB memory capacity supported
  - — Maximum 1-GB memory capacity on one SO-DIMM or Memory Down
- Memory organizations:
  - — Two SO-DIMMs
  - — One SO-DIMM only
  - — One SO-DIMM and One Memory Down (based on simulations only)
- Up to 32 simultaneous open pages (assuming 4 Ranks of 8 Bank Devices)
- Partial Writes to memory using Data Mask signals (DM)
- On-Die Termination (ODT)
- Intel® Fast Memory Access (Intel FMA)
  - — Just-in-Time Command Scheduling
  - — Command Overlap
  - — Out-of-Order Scheduling
  - — Opportunistic Writes
- Support memory thermal management scheme to selectively manage reads and/or writes. Memory thermal management can be triggered by either on-die thermal sensor, or by preset limits. Management limits are determined by weighted sum of various commands that are scheduled on the memory interface.
-

Support DDR3 SDRAMs:

- Support for DDR3 at data transfer rate of 667 MT/s
- One channel of DDR3 memory (consists of 64-bit of data lines): Maximum of two SO-DIMMs in Raw Card-A or Raw Card-B format
- I/O Voltage of 1.5 V for DDR3

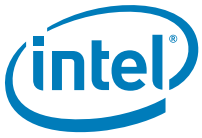
- Maximum of 2-GB system memory capacity supported on one SO-DIMM or two SO-DIMMs
- Memory organizations supported (refer to the Platform Design Guide for more details - DIMM populating rules and Clock/Control signals ordering):
  - Two SO-DIMMs
  - One SO-DIMM only

1.2.2 Direct Media Interface Features

- Compliant to Direct Media Interface (DMI)
- Support 2 lanes in each direction, point-to-point DMI interface to the chipset
- Raw bit-rate on the data pins of 2.5Gb/s, resulting in a real bandwidth per pair of 250MB/s given the 8b/10b encoding used to transmit data across this interface. Does not account for packet overhead and link maintenance
- Maximum theoretical bandwidth on interface of 500MB/s in each direction simultaneously, for an aggregate of 1GB/s for the interface
- 100-MHz reference clock
- 64-bit downstream address (only 36-bit addressable from the processor)
- APIC messaging support. Will send Intel-defined “End of Interrupt” broadcast message when initiated by the processor
- Message Signaled Interrupt (MSI) messages supported
- Power Management state change messages supported
- SMI, SCI and SERR error indication
- Legacy support for ISA regime protocol (PHOLD/PHOLDA) required for parallel port DMA, floppy drive, and LPC bus masters
- Hybrid AC-DC coupling solution between the processor and the chipset
- Polarity inversion supported

1.2.3 Integrated Graphics Controller

- The integrated graphics controller contains a refresh of the 3rd generation graphics core
- Intel® Dynamic Video Memory Technology 4.0
- Directx* 9 compliant Pixel Shader 2.0
- 200-MHz render clock frequency
- Two display ports: LVDS and RGB
  - Integrated single LVDS channel support resolution up to 1280*800 or 1366*768
  - Analog RGB display output up to resolution 1400x1050 @ 60Hz
- Intel® Clear Video Technology



— MPEG2 Hardware Acceleration

— ProcAmp

1.3 Clocking

- Differential Core clock of 166 MHz (BCLKP/BCLKN)
- Differential Host clock of 166 MHz (HPL_CLKINP/HPL_CLKINN)
- The differential DMI clock of 100 MHz (EXP_CLKINP/EXP_CLKINN)
- Display timings are generated from display PLLs that use a 96 MHz or 100 MHz differential clock as reference.
- All of the above clocks are capable of tolerating Spread Spectrum clocking.
- Memory clocks generated from internal Host PLLs
- Host, Memory, DMI, Display PLLs and all associated internal clocks are disabled until PWROK is asserted.

1.4 Power Management Support

- Processor Core:
  - Full support of ACPI C-states as implemented by the following processor C-states: C0/C1(E)/C2(E)/C4(E)
  - Enhanced Intel SpeedStep® Technology
- Thermal Management 1 (TM1) and Thermal Management 2 (TM2)
- System states: S0, S3, S4 and S5
- DMI: L0s and L1 ASPM power management capability

1.5 Package

- The processor is a Micro-FCBGA8 type of package at 22mmx22mm package size

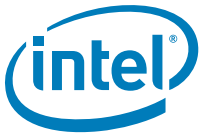
1.6 Terminology

(Sheet 1 of 3)

Term	Description
BGA	Ball Grid Array
BLT	Block Level Transfer
CRT	Cathode Ray Tube
DDR2	Second generation Double Data Rate SDRAM memory technology
DDR3	Third generation Double Data Rate SDRAM memory technology

(Sheet 2 of 3)

Term	Description
DMA	Direct Memory Access
DMI	Direct Media Interface
DTS	Digital Thermal Sensor
ECC	Error Correction Code
Enhanced Intel SpeedStep® Technology	Technology that provides power management capabilities to laptops.
Execute Disable Bit	The Execute Disable bit allows memory to be marked as executable or non-executable, when combined with a supporting operating system. If code attempts to run in non-executable memory the processor raises an error to the operating system. This feature can prevent some classes of viruses or worms that exploit buffer overrun vulnerabilities and can thus help improve the overall security of the system. See the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* for more detailed information.
Micro-FBGA	Micro Flip Chip Ball Grid Array
(G)MCH	Legacy component - Graphics Memory Controller Hub.
GPU	Graphics Processing Unit
ICH	The legacy I/O Controller Hub component that contains the main PCI interface, LPC interface, USB2, Serial ATA, and other I/O functions. It communicates with the legacy (G)MCH over a proprietary interconnect called DMI.
IMC	Integrated Memory Controller
Intel® 64 Technology	64-bit memory extensions to the IA-32 architecture.
LCD	Liquid Crystal Display
LVDS	Low Voltage Differential Signaling A high speed, low power data transmission standard used for display connections to LCD panels.
NCTF	Non-Critical to Function: NCTF locations are typically redundant ground or non-critical reserved, so the loss of the solder joint continuity at end of life conditions will not affect the overall product functionality.
Processor Core	The term “processor core” refers to Silicon die itself which may contain single or multiple execution cores.
Rank	A unit of DRAM corresponding four to eight devices in parallel, ignoring ECC. These devices are usually, but not always, mounted on a single side of a SO-DIMM.
SCI	System Control Interrupt. Used in ACPI protocol.
TDP	Thermal Design Power
TOM	Top of Memory
TTM	Time-To-Market
V_{CC}	Processor core power supply



(Sheet 3 of 3)

Term	Description
V_{SS}	Processor ground
V_{CCGFX}	Graphics core power supply
V_{CCSM}	DDR2/DDR3 power rail

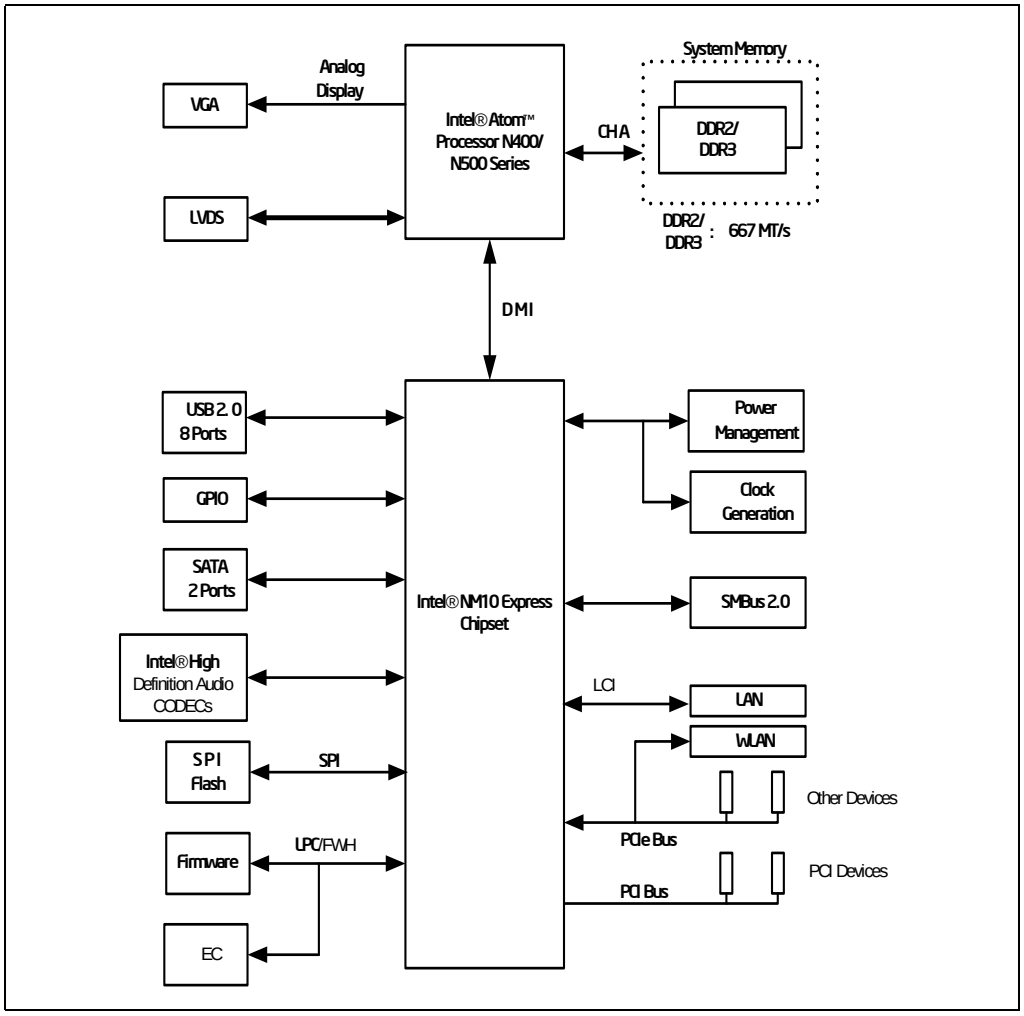
1.7 References

Please refer to the following documents which may be beneficial when reading this document or for additional information:

Document	Document Number
Intel® 64 and IA-32 Architectures Software Developer's Manuals Volume 1: Basic Architecture Volume 2A: Instruction Set Reference, A-M Volume 2B: Instruction Set Reference, N-Z Volume 3A: System Programming Guide Volume 3B: System Programming Guide	http://www.intel.com/products/processor/manuals/index.htm
AP-485, Intel® Processor Identification and CPUID Instruction Application Note	241618
Intel® Atom™ Processor N400 Series Datasheet - Volume 2	322848
Intel® Atom™ Processor N400 Series Specification Update	322849
Intel® NM10 Express Chipset Datasheet	322896

1.8 System Block Diagram

Figure 1-1. Platform Block Diagram



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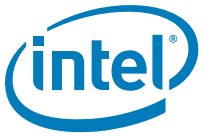


2 Signal Description

This chapter describes the processor signals. They are arranged in functional groups according to their associated interface or category. The following notations are used to describe the signal type.

Table 2-1. Signal Types

Notations	Signal Type
I	Input Pin
O	Output Pin
I/O	Bi-directional Input/Output Pin

The signal description also includes the type of buffer used for the particular signal.

Table 2-2. Signal Description Buffer Types

Signal	Description
CMOS	CMOS buffers. 1.05-V tolerant
DMI	Direct Media Interface signals. These signals are compatible with PCI Express* 1.0 signalling environment AC specifications but are DC coupled. The buffers are not 3.3-V tolerant.
HVCMOS	High Voltage buffers. 3.3-V tolerant
DDR2/DDR3	DDR2/DDR3 buffers: 1.8-V/1.5-V tolerant respectively
TAP	Test Access Port signal
Analog	Analog reference or output. May be used as a threshold voltage or for buffer compensation
Ref	Voltage reference signal
GTL+	Gunning Transceiver Logic signaling technology. Refer to GTL+ I/O Specification for complete details.
Asynch	This signal is asynchronous and has no timing relationship with any reference clock.
LVDS	Low Voltage Differential Signalling. A high speed, low power data transmission standard used for display connections to LCD panels.
SSTL - 1.8/ 1.5	Stub Series Termination Logic. These are 1.8-V (DDR2) or 1.5-V (DDR3) output capable buffers. 1.8-V or 1.5-V tolerant.

2.1 Processor Legacy Signals

Table 2-3. Processor Legacy Signals

Signal Name	Description	Direction	Type
A20M#	If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit-20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-MB boundary. Assertion of A20M# is only supported in real mode.	I	Core CMOS
BSEL[2:0]	BSEL[2:0] (Bus Select) are used to select the processor input clock frequency.	O	Core CMOS
CPUPWRGOOD	CPUPWRGOOD (Power Good) is a processor input. The processor requires this signal to be a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. CPUPWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of CPUPWRGOOD. It must also meet the minimum pulse width specification. The CPUPWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.	I	Core CMOS
DPRSTP#	DPRSTP#, when asserted on the platform causes the processor to transition from the Deep Sleep State to the Deeper Sleep state. In order to return to the Deep Sleep State, DPRSTP# must be deasserted. DPRSTP# is driven by the chipset.	I	Core CMOS
DPSLP#	DPRSLP#, when asserted on the platform causes the processor to transition from the Sleep State to the Deep Sleep state. In order to return to the Sleep State, DPSLP# must be deasserted. DPRSTP# is driven by the chipset.	I	Core CMOS
EXTBGREF	External Bandgap Reference.	I	Core Analog

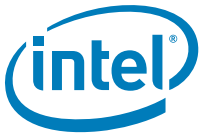
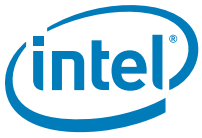


Table 2-3. Processor Legacy Signals

Signal Name	Description	Direction	Type
FERR#	FERR# (Floating-point Error) is a multiplexed signal and its meaning is qualified with STPCLK#. When STPCLK# is not asserted, FERR# indicates a floating point when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MSDOS*- type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR# indicates that the processor has a pending break event waiting for service. The assertion of FERR# indicates that the processor should be returned to the Normal state. When FERR# is asserted, indicating a break event, it will remain asserted until STPCLK# is deasserted. Assertion of PREQ# when STPCLK# is active will also cause an FERR# break event. For additional information on the pending break event functionality, including identification of support of the feature and enable/disable information, refer to Volume 3 of the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* and the *Intel® Processor Identification and CPUID Instruction Application Note*.	O	Core Open Drain
GTLREF	Reference voltage for BPM* pins.	I	Core Analog
IGNNE#	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute non-control floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a non-control floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set.	I	Core CMOS
INIT#	INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion.	I	Core CMOS

Table 2-3. Processor Legacy Signals

Signal Name	Description	Direction	Type
LINT0, LINT1	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a non-maskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT0/LINT1. Because the APIC is enabled by default after Reset, operation of these pins as LINT0/LINT1 is the default configuration.	I	Core CMOS
SMI#	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the deassertion of RESET# the processor will tristate its outputs.	I	Core CMOS
STPCLK#	Stop clock, when asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution.	I	Core CMOS
THERMDA_1 THERMDC_1	Thermal Diode - Anode & Cathode of the processor.	I O	Core Analog
THERMDA_2/RSVD THERMDC_2/RSVD	Reserved pins of Thermal Diode.	I O	Core Analog
BPM_1#[3:0] BPM_2#[3:0]/ RSVD	Breakpoint and Performance Monitor Signals: Output from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM_2#[3:0]/RSVD are reserved pins.	I/O	GTL+
PRDY#	PRDY# is a processor output used by debug tools to determine processor debug readiness.	O	Asynch GTL+
PREQ#	PREQ# is used by debug tools to request debug operation of the processor.	I	Asynch GTL+



2.2 System Memory Interface

Table 2-4. System Memory Interface

Signal Name	Description	Direction	Type
DDR_A_CK_[1:0]	**SDRAM Differential Clock:** SDRAM Differential clock signal pair.	O	SSTL-1.8
DDR_A_CK#_[1:0]	**SDRAM Inverted Differential Clock:** SDRAM Differential clock signal-pair complement.	O	SSTL-1.8
DDR_A_CK_[4:3]	**SDRAM Differential Clock:** SDRAM Differential clock signal pair.	O	SSTL-1.8
DDR_A_CK#_[4:3]	**SDRAM Inverted Differential Clock:** SDRAM Differential clock signal-pair complement.	O	SSTL-1.8
DDR_A_CS#_[3:0]	**Chip Select:** (1 per Rank) used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.	O	SSTL-1.8
DDR_A_CKE_[3:0]	**Clock Enable:** (1 per Rank) used to: • Initialize the SDRAM during power-up • Power-down SDRAM ranks • Place all SDRAM ranks into and out of self-refresh during STR	O	SSTL-1.8
DDR_A_MA_[14:0]	**Multiplexed Address:** These signals are used to provide the multiplexed row and column address to the SDRAM.	O	SSTL-1.8
DDR_A_BS_[2:0]	**Bank Select:** These signals define which banks are selected within each SDRAM rank.	O	SSTL-1.8
DDR_A_RAS#	**RAS Control Signal**: Used with DDR_A_CAS# and DDR_A_WE# (along with DDR_A_CS#) to define the SDRAM commands.	O	SSTL-1.8
DDR_A_CAS#	**CAS Control Signal:** Used with DDR_A_RAS# and DDR_A_WE# (along with DDR_A_CS#) to define the SDRAM commands.	O	SSTL-1.8
DDR_A_WE#	**Write Enable Control Signal:** Used with DDR_A_RAS# and DDR_A_CAS# (along with DDR_A_CS#) to define the SDRAM commands.	O	SSTL-1.8
DDR_A_DQ_[63:0]	**Data Bus:** Channel data signal interface to the SDRAM data bus	I/O	SSTL-1.8

Table 2-4. System Memory Interface

Signal Name	Description	Direction	Type
DDR_A_DM_[7:0]	**Data Mask:** These signals are used to mask individual bytes of data in the case of a partial write, and to interrupt burst writes. When activated during writes, the corresponding data groups in the SDRAM are masked. There is one DDR_A_DM_[7:0] for every data byte lane.	O	SSTL-1.8
DDR_A_DQS_[7:0]	**Data Strobes:** DDR_A_DQS_[7:0] and its complement signal group make up a differential strobe pair. The data is captured at the crossing point of DDR_A_DQS_[7:0] and its DDR_A_DQS#_[7:0] during read and write transactions.	I/O	SSTL-1.8
DDR_A_DQS#_[7:0]	**Data Strobe Complements:** These are the complementary strobe signals.	I/O	SSTL-1.8
DDR_A_ODT_[3:0]	**On-Die-Termination:** Active Termination Control	O	SSTL-1.8

Table 2-5. Memory Reference and Compensation

Signal Name	Description	Direction	Type
DDR_RPD	System Memory RCOMP signal.	I/O	Analog
DDR_RPU	System Memory RCOMP signal.	I/O	Analog
DDR_VREF	SDRAM Reference Voltage	I	Analog

2.3 Reset and Miscellaneous Signals

Table 2-6. Reset and Miscellaneous Signals (Sheet 1 of 2)

Signal Name	Description	Direction	Type
RSTIN#	**Reset In**: When asserted, this signal will asynchronously reset the CPU logic. The signal is connected to the PLTRST# output of the south bridge. This input should have a Schmitt trigger to avoid spurious resets. This signal is required to be 3.3-V tolerant.	I	HVCMOS
PWROK	**Power OK**: When asserted, PWROK is an indication to the processor that core power has been stable. This input should have a Schmitt trigger to avoid spurious resets. This signal is required to be 3.3-V tolerant.	I	HVCMOS

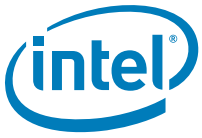


Table 2-6. Reset and Miscellaneous Signals (Sheet 2 of 2)

Signal Name	Description	Direction	Type
PM_EXTTS[1:0]#	**External Thermal Sensor Input:** If the system temperature reaches a dangerously high value then this signal can be used to trigger the start of system memory throttling. EXTTS1# can alternately be used to implement fast C4/C4E exit. See Section 5.3 for details. This functionality is not available on EXTTS0#.	I	HVCMOS
DDR3_DRAM_PWR OK	**DDR3 Power Good Monitor**. Driven by platform logic for DDR3. Reserved pin for DDR2 design.	I	CMOS-1.5
DDR3_DRAMRST#	**DDR3 DRAM Reset**. Reset signal from IMC to DRAM devices; one for all SO-DIMMs. Used only in DDR3 mode; reserved pin for DDR2 design.	O	SSTL-1.5
RSVD	**Reserved**. Must be left unconnected on the board. Intel does not recommend a test point on the board for this ball.	N/A	N/A
RSVD_NCTF	**Reserved/non-critical to function**. Pin for package mechanical reliability. A test point may be placed on the board for this ball.	N/A	N/A
RSVD_TP	**Reserved-test-point.** A test point may be placed on the board for this ball.	N/A	N/A
XDP_RSVD_[17:0]	**Reserved XDP debug signals.** Connect to XDP connector; or just left as Not-Connected except for XDP_RSVD_9 - pull this pin to low for normal operation.	N/A	N/A

2.4 DMI - Direct Media Interface

Table 2-7. DMI - Processor to Chipset Serial Interface

Signal Name	Description	Direction	Type
DMI_RXP[1:0] DMI_RXN[1:0]	DMI input from south bridge: Direct Media Interface receive differential pair.	I	DMI
DMI_TXP[1:0] DMI_TXN[1:0]	DMI output to south bridge: Direct Media Interface transmit differential pair.	O	DMI
EXP_ICOMPI	PCI-Express-G Input Current Compensation. Connect to EXP_RCOMPO and then to Ground via one 50 Ohm serial resistor.	I	Analog
EXP_RCOMPO	PCI-Express-G Resistance Compensation. Connect to EXP_ICOMPI and then to Ground via one 50 Ohm serial resistor.	I/O	Analog
EXP_RBIAS	PCI-Express CML Bias control: Connect to a 750 Ohm resistor to ground.	I/O	Analog

2.5 PLL Signals

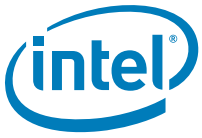
Table 2-8. PLL Signals

Signal Name	Description	Direction	Type
BCLKP[0] BCLKN[0]	Differential Core Clock In	I	Diff Clk CMOS
HPL_CLKINP HPL_CLKINN	Differential Host Clock In	I	Diff Clk CMOS
EXP_CLKINP EXP_CLKINN	Differential DMI Clock In	I	Diff Clk CMOS
REFCLKINN REFCLKINP	Differential PLL Clock In	I	Diff Clk CMOS
REFSSCLKINN REFSSCLKINP	Differential Spread Spectrum Clock In	I	Diff Clk CMOS

2.6 Analog Display Signals

Table 2-9. Analog Display Signals

Signal Name	Description	Direction	Type
CRT_RED	**RED Analog Video Output**: This signal is a CRT analog video output from the internal color palette DAC.	O	Analog
CRT_GREEN	**GREEN Analog Video Output**: This signal is a CRT analog video output from the internal color palette DAC.	O	Analog
CRT_BLUE	**BLUE Analog Video Output**: This signal is a CRT analog video output from the internal color palette DAC.	O	Analog
CRT_IRTN	Current return path. Shorted to ground	O	Analog
DAC_IREF	**Resistor Set**: Set point resistor for the internal color palette DAC. A 665-Ohm ±1% resistor is required between DAC_IREF and motherboard ground.	I/O	Analog
CRT_HSYNC	**CRT Horizontal Synchronization**: This signal is used as the vertical sync (polarity is programmable) or “sync interval”. 3.3-V output.	O	HVCMOS
CRT_VSYNC	**CRT Vertical Synchronization**: This signal is used as the vertical sync (polarity is programmable). 3.3-V output.	O	HVCMOS
CRT_DDC_CLK	CRT DDC Clock for monitor control	I/O	COD
CRT_DDC_DATA	CRT DDC Data for monitor control	I/O	COD



2.7 LVDS Signals

Table 2-10.LVDS Signals

Signal Name	Description	Direction	Type
LA_DATAP_[2:0]	Differential data output - positive	O	LVDS
LA_DATAN_[2:0]	Differential data output - negative	O	LVDS
LA_CLKP	Differential clock output - positive	O	LVDS
LA_CLKN	Differential clock output - negative	O	LVDS
LIBG	LVDS Reference Current. Need 2.37-KOhm pull-down resistor	I/O	Ref
LVBG	Reserved. No connect.	O	Analog
LVREFH	Reserved. Can be connected to V_{SS} or left as No Connect.	I	Ref
LVREFL	Reserved. Can be connected to V_{SS} or left as No Connect.	I	Ref
LVDD_EN	**LVDS Panel Power Enable**: Panel power control enable control.	O	HVCMOS
LBKLT_EN	**LVDS Backlight Enable**: Panel backlight enable control.	O	HVCMOS
LBKLT_CTL	**Panel Backlight Brightness Control**: Panel brightness control. The accuracy of the PWM duty cycle of LBKLT_CTL signal for any given value will be within ±20 ns.	O	HVCMOS
LCTLA_CLK	I2C based control signal (Clock) for External SSC clock chip control - optional	I/O	COD
LCTLB_DATA	I2C based control signal (Data) for External SSC clock chip control - optional	I/O	COD
LDDC_CLK	EDID support for flat panel display	I/O	COD
LDDC_DATA	EDID support for flat panel display	I/O	COD

2.8 TAP Signals

Table 2-11.TAP Signals (Sheet 1 of 2)

Signal Name	Description	Direction	Type
TCK	**TCK (Test Clock)** provides the clock input for the processor Test Bus (also known as the Test Access Port).	I	TAP OD
TDI	**TDI (Test Data In)** transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.	I	TAP OD

Table 2-11.TAP Signals (Sheet 2 of 2)

TDO	**TDO (Test Data Out)** transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.	O	TAP OD
TMS	**TMS (Test Mode Select)** is a JTAG specification support signal used by debug tools.	I	TAP OD
TRST#	**TRST# (Test Reset)** resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset.	I	TAP OD

2.9 Error and Thermal Protection

Table 2-12.Error and Thermal Protection

Signal Name	Description	Direction	Type
PROCHOT#	**Processor Hot#**: This will go active when the processor temperature monitoring sensor(s) detects that the processor has reached its maximum safe operation temperature Output: This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. Input: This signal can also be driven to the processor to activate the TCC.	I/O	I: CMOS O: OD
THERMTRIP#	**Thermal Trip**: The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 125°C. This is signaled to the system by the THERMTRIP# pin.	O	Open Drain

2.10 Processor Core Power Signals

Table 2-13.Processor Core Power Signals

Signal Name	Description	Direction	Type
VCC	Processor-core power supply. The voltage supplied to these pins is determined by the VID pins.		PWR
VCC_SENSE	VCC_SENSE and VSS_SENSE provide an isolated, low impedance connection to the processor core voltage and ground. They can be used to sense or measure voltage near the silicon.		Analog

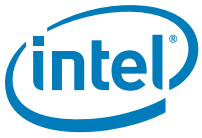


Table 2-13.Processor Core Power Signals

VID[6:0]	VID[6:0] (Voltage ID) are used to support automatic selection of power supply voltages (VCC).	I/O	CMOS
VSS_SENSE	VCC_SENSE and VSS_SENSE provide an isolated, low impedance connection to the processor core voltage and ground. They can be used to sense or measure voltage near the silicon.		Analog
VCCA	Processor PLL power supply.		PWR

2.11 Graphics, DMI and Memory Core Power Signals

Table 2-14.Power Signals

Signal Name	Description	Voltage Level (V)	Type
VCCP	LGI power supply	1.05	PWR
VCCGFX	Graphics core power supply	0.89	PWR
VCCSM	DDR2/DDR3 power supply	1.8/ 1.5	PWR
VCCA_DMI	DMI power supply	1.05	PWR
VCCACRTDAC	CRT DAC power supply	1.8	PWR
VCC_GIO	Graphics I/O power supply	3.3	PWR
VCC_LGI	LGIO VID power supply	1.05	PWR
VCCA_DDR	DDR2 power supply	1.05	PWR
VCCD_HMPLL	HMPLL power supply	1.05	PWR
VCCDLVDS	LVDS power supply	1.8	PWR
VCCSFR_DMIHMPLL	DMI, HPLL, MPLL power supply	1.8	PWR
VCCACK_DDR	DDR2 power supply	1.05	PWR
VCCD_AB_DPL	DPLL power supply	1.05	PWR
VCCSFR_AB_DPL	DPLL power supply	1.8	PWR
VCCRING_EAST	GIO, LVDS power supply	1.05	PWR
VCCRING_WEST	LGIO power supply	1.05	PWR
VCCCK_DDR	DDR2/DDR3 clock power supply	1.8/1.5	PWR

2.12 Ground

Table 2-15.Ground

Signal Name	Description	Direction	Type
VSS	VSS are the ground pins for the processor and should be connected to the system ground plane.		GND

§

3 Functional Description

3.1 Integrated Memory Controller

The integrated memory controller supports DDR2 or DDR3 protocols with one 64 bit wide channel accessing two SO-DIMMs. The controller supports a maximum of two un-buffered, non-ECC DDR2 or DDR3 SO-DIMMs; thus allowing up to four device ranks.

3.1.1 System Memory Organization Modes

The integrated memory controller supports only one memory organization mode: single channel. In this mode, all memory cycles are directed to a single channel.

3.1.2 System Memory Technology Supported

3.1.2.1 DDR2 Memory

The system memory controller supports the following DDR2 Data Transfer Rates, SO-DIMM Modules and DRAM Device Technologies:

- DDR2 Data Transfer Rate: 667MT/s (PC2-5300)
- DDR2 SO-DIMM Modules (unbuffered, non-ECC):
  - Raw Card A = 2 Ranks of x16 SDRAMs (Double-sided)
  - Raw Card C = 1 Rank of x16 SDRAMs (Single-sided)

“Single sided” above is a logical term referring to the number of Chip Selects attached to the SO-DIMM. A real SO-DIMM may put the components on both sides of the substrate, but be logically indistinguishable from single sided SO-DIMM if all components on the SO-DIMM are attached to the same Chip Select signal.

Note: x16 means that each SDRAM component has 16 data lines.

- DDR2 DRAM Device Technology:
  - Standard 512Mb, 1Gb and 2Gb technologies and addressing are supported for x16 devices. There is no support for SO-DIMMs with different technologies or capacities on opposite sides of the same SO-DIMM. If one side of a SO-DIMM is populated, the other side is either identical or empty.

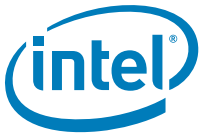


Table 3-16.Supported SO-DIMM Module Configurations

Raw Card Type	DIMM Capacity	DRAM Device Tech.	DRAM Organization	# of DRAM Devices	# of Ranks	Page Size
A	512MB	512Mb	32M x 16	8	2	8K
A	1GB	1Gb	64M x16	8	2	8K
C	256MB	512Mb	32M x 16	4	1	8K
C	512MB	1Gb	64M x 16	4	1	8K
C	1GB	2Gb	128M x 16	4	1	8K

3.1.2.2 DDR3 Memory

The system memory controller supports the following DDR3 Data Transfer Rates, SO-DIMM Modules and DRAM Device Technologies:

- DDR3 Data Transfer Rate: 667MT/s
- DDR3 SO-DIMM Modules (unbuffered, non-ECC):
  - — Raw Card A = 2 Ranks of x16 SDRAMs (Double-sided)
  - — Raw Card B = 1 Rank of x8 SDRAMs (Double-sided)

NOTE: x16/x8 means that each SDRAM component has 16/8 data lines.

- DDR3 DRAM Device Technology:
  - — Standard 1Gb and 2Gb technologies and addressing are supported for x16/x8 devices. There is no support for SO-DIMMs with different technologies or capacities on opposite sides of the same SO-DIMM. If one side of a SO-DIMM is populated, the other side is either identical or empty.

Table 3-17.Supported DDR3 S0-DIMM module Configurations

Raw Card Type	DIMM Capacity	DRAM Device Tech.	DRAM Organization	# of DRAM Devices	# of Ranks	Page Size
A	1GB	1Gb	64M x 16	8	2	8K
A	2GB	2Gb	128M x16	8	2	8K
B	1GB	1Gb	128M x 8	8	1	8K
B	2GB	2Gb	256M x 8	8	1	8K

3.1.3 Rules for populating SO-DIMM slots

The frequency of system memory will be the lowest frequency of all SO-DIMMs in the system, as determined through the SPD registers on the SO-DIMMs. Timing parameters [CAS latency (or CL + AL for DDR2), tRAS, tRCD, tRP] must be programmed to match within a channel.

To take advantage of enhanced addressing, it should be populating both SO-DIMM slots with the identical Raw Card type. If one SO-DIMM is used only, it should be populating the second slot (the further slot to the processor's Integrated Memory Controller) to get the best signal quality.

3.1.4 Intel® Fast Memory Access (Intel® FMA) Technology Enhancements

The following sections outline and explain the technology enhancements: Just-in-Time Command Scheduling, Command Overlap, Out-of-Order Scheduling and Opportunistic Writes.

3.1.4.1 Just-in-Time Command Scheduling

The memory controller has an advanced command scheduler where all pending requests are examined simultaneously to determine the most efficient request to be issued next. The most efficient request is picked from all pending requests and issued to system memory Just-in-Time to make optimal use of Command Overlapping. Thus, instead of having all memory access requests go individually through an arbitration mechanism forcing requests to be executed one at a time, they can be started without interfering with the current request allowing for concurrent issuing of requests. This allows for optimized bandwidth and reduced latency while maintaining appropriate command spacing to meet system memory protocol.

3.1.4.2 Command Overlap

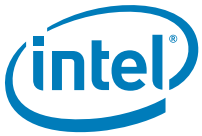
Command Overlap allows the insertion of the DRAM commands between the Activate, Precharge, and Read/Write commands normally used, as long as the inserted commands do not affect the currently executing command. Multiple commands can be issued in an overlapping manner, increasing the efficiency of system memory protocol.

3.1.4.3 Out-of-Order Scheduling

While leveraging the Just-in-Time Scheduling and Command Overlap enhancements, the IMC continuously monitors pending requests to system memory for the best use of bandwidth and reduction of latency. If there are multiple requests to the same open page, these requests would be launched in a back to back manner to make optimum use of the open memory page. This ability to reorder requests on the fly allows the IMC to further reduce latency and increase bandwidth efficiency.

3.1.4.4 Opportunistic Writes

Processor requests for memory reads usually are weighted more heavily than writes to memory to avoid cases of starving the processor of data to process while the writes are issued to system memory. Instead of having writes issued to a pending queue to be flushed to memory when certain watermarks are reached, which could starve the processor of data while it waits for the write flush to finish, the IMC monitors system memory requests and issues pending write requests to memory at times when they will



not impact memory read requests. This allows for an almost continuous flow of data to the processor for processing.

3.1.5 DRAM Clock Generation

Every supported SO-DIMM has two differential clock pairs. There are total of four clock pairs driven directly by the processor to two SO-DIMMs.

3.2 Integrated Graphics Controller

This section details the integrated graphics engines (3D, 2D and video), 3D pipeline, and the respective capabilities.

The processor's graphics processing unit (GPU) contains several types of components. The major components in the GPU are the engines, planes, pipes and ports. The GPU has a 3D/2D instruction processing unit to control the 3D and 2D engines respectively. The processor's 3D and 2D engines are fed with data through the memory controller. The outputs of the engines are surfaces sent to the memory, which are then retrieved and processed by the processor planes.

3.2.1 3D Graphics Pipeline

This GPU runs the graphics engine at 200 MHz and has two pixel pipelines.

The 3D graphics pipeline has a deep pipeline architecture in which each stage can simultaneously operate on different primitives or on different portions of the same primitive. The 3D graphics pipeline is broken up into four major stages: geometry processing, setup (vertex processing), texture application and rasterization.

The graphics is optimized by using the processor for advance software based transform and lighting (geometry processing) as defined by Microsoft DirectX*. The other three stages of 3D processing are handled on the GPU. The setup stage is responsible for vertex processing - converting vertices to pixels. The texture application stage applies textures to pixels. The rasterization engine takes textured pixels and applies lighting and other environment affects to produce the final pixel value. From the rasterization stage, the final pixel value is written to the frame buffer in memory so it can be displayed.

3.2.1.1 3D Engine

The 3D engine on the GPU has been designed with a deep pipeline architecture, where performance is maximized by allowing each stage of the pipeline to simultaneously operate on different primitive or portions of the same primitive. The GPU supports Perspective-Correct Texture Mapping, Multitextures, Bump-Mapping, Cubic Environment Maps, Bilinear, Trilinear and Anisotropic MIP mapped filtering, Gouraud shading, Alpha-blending, Vertex and Per Pixel Fog and Z/W Buffering.

The 3D pipeline subsystem performs the 3D rendering acceleration. The main blocks of the pipeline are the setup engine, scan converter, texture pipeline, and raster pipeline. A typical programming sequence would be to send instructions to set the state of the pipeline followed by rending instructions containing 3D primitive vertex data.

The engines' performance is dependent on the memory bandwidth available. Systems that have more bandwidth available will outperform systems with less bandwidth. The engines' performance is also dependent on the core clock frequency. The higher the frequency, the more data is processed.

3.2.1.2 Texture Engine

The GPU allows an image, pattern, or video to be placed on the surface of the 3D polygon. The texture processor receives the texture coordinate information from the setup engine and the texture blend information from the scan converter. The texture processor performs texture color or ChromaKey matching, texture filtering (anisotropic, trilinear, bilinear interoplation), and YUV-to-RGB conversions.

3.2.2 Video Engine

The Video Engine handles the non-3D (media/video) applications. It includes support for VLD and MPEG2 decode in Hardware. The CGPU engine includes a number of encompassments over the previous generation capabilities, which have been listed above.

3.2.2.1 Hardware Motion Compensation

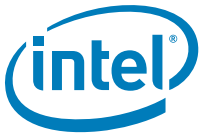
The Motion Compensation (MC) process consists of reconstructing a new picture by predicting (either forward, backward or bidirectionally) the resulting pixel colors from one or more reference pictures. The GPU receives the video stream and implements Motion Compensation and subsequent steps in hardware. Performing Motion Compensation in hardware reduces the processor demand of software-based MPEG-2 decoding, and thus improves system performance.

The Motion Compensation functionality is overloaded onto the texture cache and texture filter. The texture cache is used to typically access the data in the reconstruction of the frames and the filter is used in the actual motion compensation process. To support this overloaded functionality the texture cache additionally supports the following input format: YUV420 planar.

3.2.2.2 Sub-Picture Support

Sub-picture is used for two purposes, one is subtitles for movie captions, etc. (which are superimposed on a main picture), and “menus” used to provide some visual operation environments the user of a content player.

DVD allows movie subtitles to be recorded as Sub-pictures. On a DVD disc, it is called “subtitle” because it has been prepared for storing captions. Since the disc can have a maximum of 32 tracks for subtitles, they can be used for various applications, for example, as subtitles in different languages or other information to be displayed.



There are two kinds of Menus, the System Menus and other In-Title Menus. First, the System Menus are displayed and operated at startup of or during the playback of the disc or from the stop state. Second, In-Title menus can be programmed as a combination of Sub-picture and Highlight commands to be displayed during playback of the disc.

The GMCH supports sub-picture for DVD and DBS by mixing the two video streams via alpha blending. Unlike color keying, alpha blending provides a softer effect and each pixel that is displayed is a composite between the two video stream pixels. The GPU can utilize four methods when dealing with sub-pictures. The flexibility enables the GPU to work with all sub-picture formats.

3.2.3 2D Engine

3.2.3.1 VGA Registers

The 2D registers are a combination of registers defined for the original Video Graphics Array (VGA) and others that Intel has added to support graphics modes that have color depths, resolutions, and hardware acceleration features that go beyond the original VGA standard.

3.2.3.2 Logical 128-Bit Fixed BLT and 256 Fill Engine

Use of this BLT engine accelerates the Graphical User Interface (GUI) of Microsoft Windows* operating systems. The 128-bit BLT Engine provides hardware acceleration of block transfers of pixel data for many common Windows operations. The term BLT refers to a block transfer of pixel data between memory locations. The BLT engine can be used for the following:

- Move rectangular blocks of data between memory locations
- Data Alignment
- Perform logical operations (raster ops)

The rectangular block of data does not change as it is transferred between memory locations. The allowable memory transfers are between: cacheable system memory and frame buffer memory, frame buffer memory and frame buffer memory, and within system memory. Data to be transferred can consist of regions of memory, patterns, or solid color fills. A pattern will always be 8x8 pixels wide and may be 8, 16, or 32 bits per pixel.

The BLT engine has the ability to expand monochrome data into a color depth of 8, 16, or 32 bits. BLTs can be either opaque or transparent. Opaque transfers move the data specified to the destination. Transparent transfers compare destination color to source color and write according to the mode of transparency selected.

Data is horizontally and vertically aligned at the destination. If the destination for the BLT overlaps with the source memory location, the graphics controller can specify which area in memory to begin the BLT transfer. Hardware is included for all 256 raster operations (Source, Pattern, and Destination) defined by Microsoft, including transparent BLT.

The graphics controller has instructions to invoke BLT and stretch BLT operations, permitting software to set up instruction buffers and use batch processing. The graphics controller can perform hardware clipping during BLTs.

3.2.4 Display Pipes

The display consists of two pipes:

- Display Pipe A (VGA)
- Display Pipe B (VGA or LVDS)

A pipe consists of a set of combined planes and a timing generator. The timing generators provide the basic timing information for each of the display pipes. The GPU has two display pipes, allowing for support of two independent display streams. A port is the destination for the result of the pipe.

3.2.4.1 Clock Generator Units (DPLLs)

The clock generator units provide a stable frequency for driving display devices. It operates by converting an input reference frequency into an output frequency. The timing generators take their input from internal DPLL devices that are programmable to generate pixel clocks in the range of 20 MHz–200 MHz. Accuracy for VESA timing modes is required to be within ±0.5%.

The DPLL can take a reference frequency from the external reference inputs (REFCLKINN/P, REFSSCLKINN/P).

3.2.5 Display Ports

Display ports are the destination for the display pipes. These are the places where the data finally appears to devices outside the graphics device. the GPU has one CRT display port (Analog) and one dedicated LVDS port (Digital).

3.2.5.1 Analog Display Port Characteristics

The analog display port provides a RGB signal output along with a HSYNC and VSYNC signal. There is an associated DDC signal pair that is implemented using GPIO pins dedicated to the analog port. The intended target device is for a CRT based monitor with a VGA connector. Display devices such as LCD panels with analog inputs may work satisfactory but no functionality added to the signals to enhance that capability.

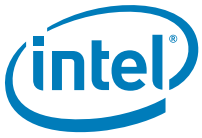


Table 3-18.Analog Port Characteristics

Signal	Port Characteristics	Support
RGB	Voltage Range	0.7 Vp-p only
	Monitor Sense	Analog Compare
	Analog Copy Protection	No
	Sync on Green	No
HSYNC VSYNC	Voltage	3.3V
	Enable/Disable	Port control
	Polarity Adjust	VGA or port control
	Composite Sync Support	No
	Special Flat Panel Sync	No
	Stereo Sync	No
DDC	Voltage	External buffered to 5V
	Control	Through GPIO interface

3.2.5.1.1 Integrated RAMDAC

The display function contains a RAM-based Digital-to-Analog Converter (RAMDAC) that transforms the digital data from the graphics and video subsystems to analog data for the CRT monitor. GPU's integrated RAMDAC supports resolutions up to 1400 x 1050 @ 60 Hz. Three 8-bit DACs provide the R, G, and B signals to the monitor.

3.2.5.1.2 Sync Signals

HSYNC and VSYNC signals are digital and conform to TTL signal levels at the connector. These signals can be polarity adjusted and individually disabled in one of the two possible states. The sync signals should power up disabled in the high state. No composite sync or special flat panel sync support will be included.

3.2.5.2 Single Channel LVDS Port

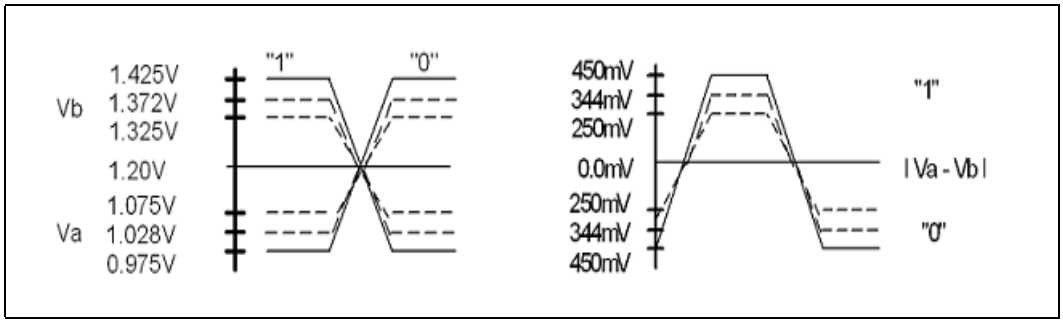
The processor has an integrated single channel LVDS (Low Voltage Differential Signaling) port that supports 1x18 data format. There is one LVDS transmitter channel in the LVDS port; this channel consists of 3 data pairs and a clock pair. The channel supports transmit clock frequency ranges from 25 MHz to 112 MHz which provides a throughput of up to 784Mbps on each data output and up to 112 MP/s on the input.

3.2.5.2.1 LVDS Data Pairs and Clock Pairs

The LVDS data and clock pairs are identical buffers and differ only in the use defined for that pair. The LVDS data pair is used to transfer pixel data as well as the LCD timing control signals. A single clock pair is used to transfer clocking information to the LVDS receiver. A serial pattern of 1100011 represents one cycle of the clock.

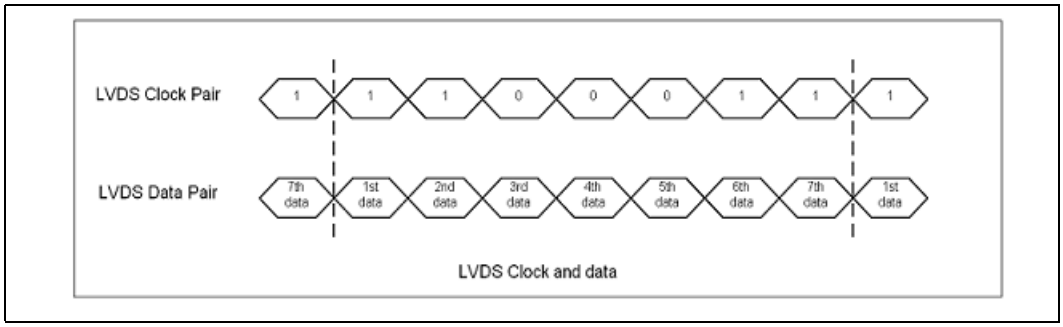
There is one LVDS transmitter channel in the LVDS interface. It contains 1-clock pair and 3-data pair of low voltage differential swing signals. Figure 3-2 shows a pair of LVDS signals and swing voltage.

Figure 3-2. LVDS Signals and Swing Voltage



1's and 0's are represented the differential voltage between the pair of signals.

Figure 3-3. LVDS Clock and Data Relationship



3.2.5.2.2 LVDS Pair States

The LVDS pairs can be put into one of five states, powered down tri-state, powered down 0 V, common mode, send 0's, or active. When in powered down state, the circuit enters a low power state and drives out 0 V or tri-states on both the output pins for the entire channel. The common mode tri-state is both pins of the pair set to the common mode voltage. When in the send 0's state, the circuit is powered up but sends only 0 for the pixel color data regardless what the actual data is with the clock lines and timing signals sending the normal clock and timing data.

3.2.5.2.3 Panel Power Sequencing

This section provides details for the power sequence timing relationship of the panel power, the backlight enable and the LVDS data timing delivery. In order to meet the panel power timing specification requirements, two signals, LVDD_EN and BKLT_EN are provided to control the timing sequencing function of the panel and the backlight power supplies.

Panel Power Sequence States

A defined power sequence is recommended when enabling the panel or disabling the panel. The set of timing parameters can vary from panel to panel vendor, provided that they stay within a predefined range of values. The panel VDD power, the backlight on/off state and the LVDS clock and data lines are all managed by an internal power sequencer.

A requested power-up sequence is only allowed to begin after the power cycle delay time requirement T4 is met.

Figure 3-4. Panel Power Sequencing

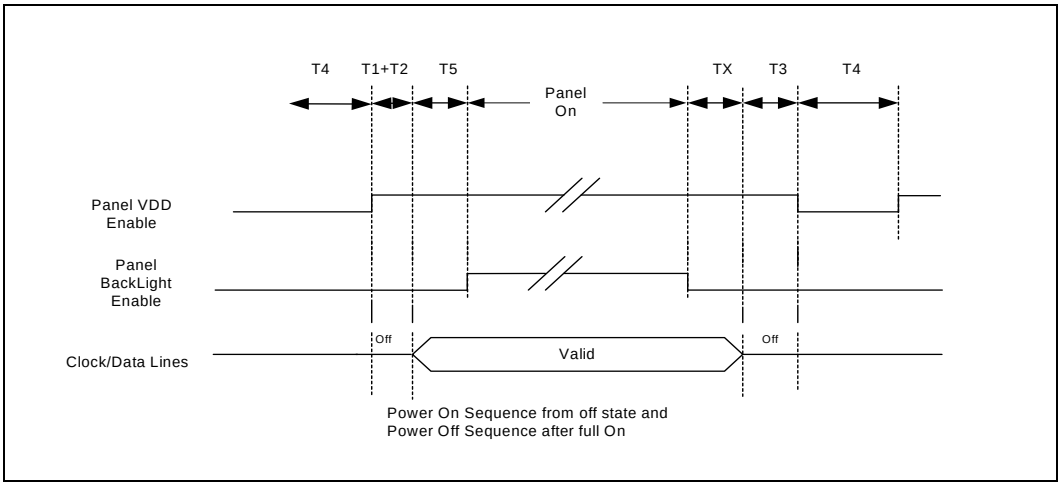


Table 3-19. Panel Power Sequencing Timing Parameters

Panel Power Sequence Timing Parameters			Min	Max	Name	Units
Spec Name	From	To				
Vdd On	0.1 Vdd	0.9 Vdd	0	10	T1	ms
LVDS Active	Vdd Stable On	LVDS Active	0	50	T2	ms
Backlight	LVDS Active	Backlight on	200		T5	ms
Backlight State	Backlight Off	LVDS off	X	X	TX	ms
LVDS State	LVDS Off	Start power off	0	50	T3	ms
Power cycle Delay	Power Off	Power On Sequence Start	0	400	T4	ms

3.2.6 VESA / VGA Mode

VESA/VGA mode provides compatibility for pre-existing software that set the display mode using the VGA CRTC registers. Timings are generated based on the VGA register values and the timing generator registers are not used.

3.2.6.1 DDC (Display Data Channel)

DDC is a standard defined by VESA. Its purpose is to allow communication between the host system and display. Both configuration and control information can be exchanged allowing plug-and-play systems to be realized. Support for DDC 1 and DDC 2 is implemented. The GPU uses the CRT_DDC_CLK and CRT_DDC_DATA signals to communicate with the analog monitor. The GPU will generate these signals at 3.3V. External pull-up resistors and level shifting circuitry should be implemented on the board.

The GPU implements a hardware GMBus controller that can be used to control these signals allowing for transactions speeds up to 100 kHz.

3.2.7 Multiple Display Configurations

Since the GPU has two display ports available for its two pipes, it can support up to two different images on different display devices. The GPU integrated in this processor supports two display modes: Dual Display Clone and Extended Desktop (LVDS + VGA).

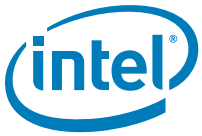
3.3 Thermal Sensor

There are several registers that need to be configured to support the uncore thermal sensor functionality and SMI# generation. Customers must enable the Catastrophic Trip Point as protection for the processor. If the Catastrophic Trip Point is crossed, then the processor will instantly turn off all clocks inside the device. Customers may optionally enable the Hot Trip Point to generate SMI#. Customers will be required to then write their own SMI# handler in BIOS that will speed up the processor (or system) fan to cool the part.

3.3.1 PCI Device 0, Function 0

The SMICMD register requires that a bit be set to generate an SMI# when the Hot Trip point is crossed. The ERRSTS register can be inspected for the SMI alert.

Address	Register Symbol	Register Name	Default Value	Access
C8-C9	ERRST	Error Status	0000h	RWC/S, RO
CC-CDh	SMICMD	SMI Command	0000h	RO, R/W



3.4 Power Management

The processor has many permutations of possibly concurrently operating modes. Care should be taken (Hardware and Software) to disable unused sections of the silicon when this can be done with sufficiently low performance impact. Refer to Chapter 5 and the *ACPI Specification, Rev3.0* for more details.

3.5 Intel® Hyper-Threading Technology

The processor supports Intel® Hyper-Threading Technology (Intel® HT Technology), which allows an execution core to function as two logical processors. While some execution resources such as caches, execution units, and buses are shared, each logical processor has its own architectural state with its own set of general-purpose registers and control registers. This feature must be enabled via the BIOS and requires operating system support.

Intel recommends enabling Hyper-Threading Technology with Microsoft Windows Vista*, Microsoft Windows* XP Professional/Windows* XP Home, and disabling Hyper-Threading Technology via the BIOS for all previous versions of Windows operating systems. For more information on Hyper-Threading Technology, see http://www.intel.com/products/ht/hyperthreading_more.htm.

§

4 Electrical Specifications

This chapter contains signal group descriptions, absolute maximum ratings, voltage identification and power sequencing. The chapter also includes DC specifications.

Please note that all data or specifications for processors supporting DDR3 and/or Dual core processors in this chapter are based on pre-silicon estimates and simulations or empirical data; these specifications will be updated with characterized data from silicon measurements at a later date.

4.1 Power and Ground Balls

The processor has V_{CC} and V_{SS} (ground) inputs for on-chip power distribution. All power balls must be connected to their respective processor power planes, while all V_{SS} balls must be connected to the system ground plane. Use of multiple power and ground planes is recommended to reduce I*R drop. The V_{CC} balls must be supplied with the voltage determined by the processor Voltage IDentification (VID) signals.

4.2 Decoupling Guidelines

Due to large number of transistors and high internal clock speeds, the processor is capable of generating large current swings between low- and full-power states. This may cause voltages on power planes to sag below their minimum values, if bulk decoupling is not adequate. Larger bulk storage (C_{BULK}), such as electrolytic capacitors, supply current during longer lasting changes in current demand (for example, coming out of an idle condition). Similarly, capacitors act as a storage well for current when entering an idle condition from a running condition. To keep voltages within specification, output decoupling must be properly designed.

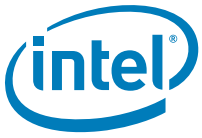
Caution: Design the board to ensure that the voltage provided to the processor remains within the specifications. Failure to do so can result in timing violations or reduced lifetime of the processor.

4.2.1 Voltage Rail Decoupling

The voltage regulator solution needs to provide:

- Bulk capacitance with low effective series resistance (ESR).
- A low path impedance from the regulator to the processor.
- Bulk decoupling to compensate for large current swings generated during power-on, or low-power idle state entry/exit.

The power delivery solution must ensure that the voltage and current specifications are met, as defined in Table 4-23.



4.3 Processor Clocking

BCLKP, BCLKN, HPL_CLKINP, HPL_CLKINN, EXP_CLKINP, EXP_CLKINN, REFCLKINP, REFCLKINN

The processor utilizes differential clocks to generate the processor core(s) and memory controller frequency, and other internal clocks. The processor core frequency is determined by multiplying the processor core ratio by 166MHz. Clock multiplying within the processor is provided by an internal phase locked loop (PLL), which requires a constant frequency input, with exceptions for Spread Spectrum Clocking (SSC).

4.3.1 PLL Power Supply

An on-die PLL filter solution is implemented on the processor. Refer to Table 4-23 for DC specifications.

4.4 Voltage Identification (VID)

The processor uses seven voltage identification signals, VID[6:0], to support automatic selection of voltages. Table 4-20 specifies the voltage level corresponding to the state of VID[6:0]. A '1' in this table refers to a high voltage level and a '0' refers to a low voltage level. If the processor is not soldered on board (VID[6:0] = 1111111), or the voltage regulation circuit cannot supply the voltage that is requested, the voltage regulator must disable itself.

VID signals are CMOS push/pull drivers. Refer to Table 4-25 for the DC specifications for these signals. Individual processor VID values may be set during manufacturing so that two devices at the same core frequency may have different VID settings.

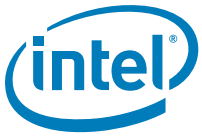
The VR utilized must be capable of regulating its output to the value defined by the VID values issued. DC specifications are included in Table 4-25 and Table 4-26.

Table 4-20.Voltage Identification Definition

VID6	VID5	VID4	VID3	VID2	VID1	VID0	VCC (V)
0	0	1	1	0	0	0	1.2000
0	0	1	1	0	0	1	1.1875
0	0	1	1	0	1	0	1.1750
0	0	1	1	0	1	1	1.1625
0	0	1	1	1	0	0	1.1500
0	0	1	1	1	0	1	1.1375
0	0	1	1	1	1	0	1.1250
0	0	1	1	1	1	1	1.1125
0	1	0	0	0	0	0	1.1000
0	1	0	0	0	0	1	1.0875
0	1	0	0	0	1	0	1.0750
0	1	0	0	0	1	1	1.0625

Table 4-20.Voltage Identification Definition

VID6	VID5	VID4	VID3	VID2	VID1	VID0	VCC (V)
0	1	0	0	1	0	0	1.0500
0	1	0	0	1	0	1	1.0375
0	1	0	0	1	1	0	1.0250
0	1	0	0	1	1	1	1.0125
0	1	0	1	0	0	0	1.0000
0	1	0	1	0	0	1	0.9875
0	1	0	1	0	1	0	0.9750
0	1	0	1	0	1	1	0.9625
0	1	0	1	1	0	0	0.9500
0	1	0	1	1	0	1	0.9375
0	1	0	1	1	1	0	0.9250
0	1	0	1	1	1	1	0.9125
0	1	1	0	0	0	0	0.9000
0	1	1	0	0	0	1	0.8875
0	1	1	0	0	1	0	0.8750
0	1	1	0	0	1	1	0.8625
0	1	1	0	1	0	0	0.8500
0	1	1	0	1	0	1	0.8375
0	1	1	0	1	1	0	0.8250
0	1	1	0	1	1	1	0.8125
0	1	1	1	0	0	0	0.8000
0	1	1	1	0	0	1	0.7875
0	1	1	1	0	1	0	0.7750
0	1	1	1	0	1	1	0.7625
0	1	1	1	1	0	0	0.7500
0	1	1	1	1	0	1	0.7375
0	1	1	1	1	1	0	0.7250
0	1	1	1	1	1	1	0.7125
1	0	0	0	0	0	0	0.7000



4.5 Catastrophic Thermal Protection

The processor supports the THERMTRIP# signal for catastrophic thermal protection. An external thermal sensor should also be used to protect the processor and the system against excessive temperatures. Even with the activation of THERMTRIP#, which halts all processor internal clocks and activity, leakage current can be high enough such that the processor cannot be protected in all conditions without the removal of power to the processor. If the external thermal sensor detects a catastrophic processor temperature of 125°C (maximum), or if the THERMTRIP# signal is asserted, the V_{CC} supply to the processor must be turned off within 500 ms to prevent permanent silicon damage due to thermal runaway of the processor. THERMTRIP# functionality is not ensured if the PWRGOOD signal is not asserted.

4.6 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD - these signals should not be connected
- RSVD_TP - these signals should be routed to a test point
- RSVD_NCTF - these signals are non-critical to function and may be left un-connected

Arbitrary connection of these signals to V_{CC}*, V_{SS}*, or to any other signal (including each other) may result in component malfunction. See Chapter 5 for a land listing of the processor and the location of all reserved signals.

For reliable operation, always connect unused inputs or bi-directional signals to an appropriate signal level. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Unused outputs maybe left unconnected; however, this may interfere with some Test Access Port (TAP) functions, complicate debug probing, and prevent boundary scan testing. A resistor must be used when tying bi-directional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability. Resistor values should be within ±20% of the impedance of the baseboard trace.

4.7 Signal Groups

Signals are grouped by buffer type and similar characteristics as listed in Chapter 2. The buffer type indicates which signaling technology and specifications apply to the signals. All the differential signals, and selected DDR2 and Control Sideband signals have On-Die Termination (ODT) resistors. There are some signals that do not have ODT and need to be terminated on the board.

All Control Sideband Asynchronous signals are required to be asserted/deasserted for at least eight BCLKs in order for the processor to recognize the proper signal state. See Section 4.10 for the DC and AC specifications.

4.8 Test Access Port (TAP) Connection

Due to the voltage levels supported by other components in the Test Access Port (TAP) logic, Intel recommends the processor be first in the TAP chain, followed by any other components within the system. A translation buffer should be used to connect to the rest of the chain unless one of the other components is capable of accepting an input of the appropriate voltage. Two copies of each signal may be required with each driving a different voltage level.

4.9 Absolute Maximum and Minimum Ratings

Table 4-21 specifies absolute maximum and minimum ratings. At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits (but within the absolute maximum and minimum ratings) the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

Although the processor contains protective circuitry to resist damage from Electro-Static Discharge (ESD), precautions should always be taken to avoid high static voltages or electric fields

Table 4-21.Processor Absolute Minimum and Maximum Ratings (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Unit	Notes[1, 2]
V_{CC}, V_{CCP}	Processor Core, LGI voltages with respect to V_{SS}	-0.3	1.45	V	6
V_{CCSM}, V_{CCCK_DDR}	Processor DDR voltage with respect to V_{SS}	-0.3	2.25	V	
V_{CCA}	Processor PLL voltage with respect to V_{SS}	-0.3	2.25	V	
V_{CCGFX}	Processor GFX voltage with respect to V_{SS}	-0.3	1.55	V	
V_{CCLVDS}	Processor LVDS voltage with respect to V_{SS}	-0.3	2.25	V	
V_{CCA_DDR}, V_{CCACK_DDR}	Processor DDR PLL voltage with respect to V_{SS}	-0.3	1.45	V	
V_{CCRING_EAST}, V_{CCRING_WEST}, $V_{CC\_LGI\_VID}$,	Processor DAC, LGIO, LVDS, & LGIO voltage with respect to V_{SS}	-0.3	1.45	V	
$V_{CCD\_AB\_DPL}$, V_{CCD_HMPLL}	Processor DPLL, & HMPLL voltage with respect to V_{SS}	-0.3	1.45	V	
$V_{CCSFR\_AB\_DPL}$,	Processor SFR DPLL voltage with respect to V_{SS}	-0.3	2.25	V	
$V_{CCACRTDAC}$	Processor CRT DAC voltage with respect to V_{SS}	-0.3	2.25	V	

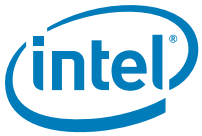


Table 4-21.Processor Absolute Minimum and Maximum Ratings (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Unit	Notes[1, 2]
$V_{CCSFR\_DMIHMPLL}$	Processor DMI SFR voltage with respect to V_{SS}	-0.3	2.25	V	
V_{CC_GIO}	Processor GIO voltage with respect to V_{SS}	3.135	3.465	V	
$T_{STORAGE}$	Storage temperature	-40	85	°C	3, 4, 5
VinLGIO	LGIO Buffer DC Input Voltage with Respect to $V_{SS,}$	-0.1	1.45	V	
VinAsynch_CMOS	CMOS Buffer DC Input Voltage with Respect to V_{SS}	-0.1	1.45	V	

NOTES:
1. For functional operation, all processor electrical, signal quality, mechanical and thermal specifications must be satisfied.
2. Excessive overshoot or undershoot on any signal will likely result in permanent damage to the processor.
3. Storage temperature is applicable to storage conditions only. In this scenario, the processor must not receive a clock, and no lands can be connected to a voltage bias. Storage within these limits will not affect the long-term reliability of the device. For functional operation, please refer to the processor case temperature specifications.
4. This rating applies to the processor and does not include any tray or packaging.
5. Failure to adhere to this specification can affect the long-term reliability of the processor.
6. V_{CC} is a VID based rail.

Possible damage to the processor may occur if the processor temperature exceeds 150 °C. Intel does not ensure functionality for parts that have exceeded temperature above 150 °C due to specification violation.

4.10 DC Specifications

Section 4.10 lists the DC specifications for the processor and are valid only while meeting the thermal specifications, clock frequency, and input voltages.

4.10.1 Voltage and Current Specifications

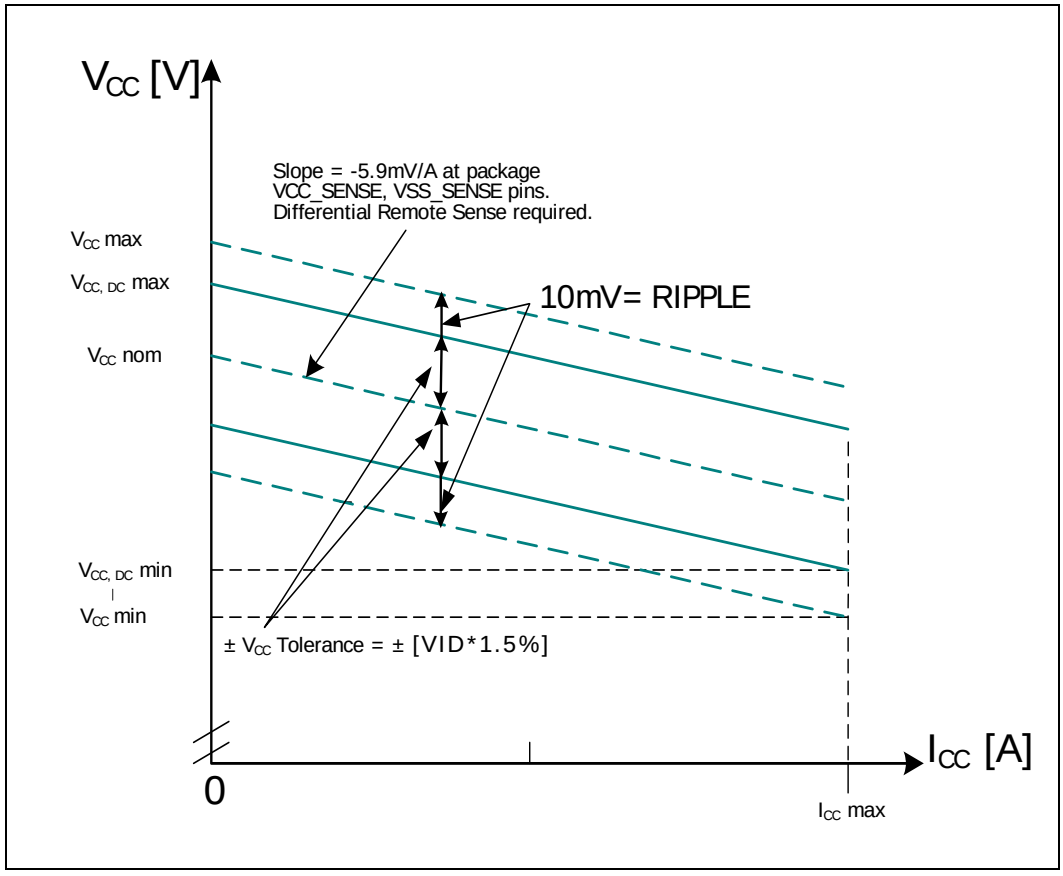
Table 4-23 and Table 4-23 list the DC specifications for the processor core and I/O buffer; they are valid only while meeting specifications for junction temperature, clock frequency, and input voltages. The Highest Frequency Mode (HFM) and Lowest Frequency Mode (LFM) refer to the highest and lowest core operating frequencies supported on the processor. Active mode load line specifications apply in all states except in the Deeper Sleep state. $V_{CC,BOOT}$ is the default voltage driven by the voltage regulator at power up in order to set the VID values. Unless specified otherwise, all specifications for the processor are at T_J = 100°C. Care should be taken to read all notes associated with each parameter.

Table 4-22.Processor Core Active and Idle Mode DC Voltage and Current Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Note[1]
VID	VID Range	0.8		1.175	V	
V_{CC_HFM}	V_{CC} at Highest Frequency Mode (HFM)	0.9625		1.175	V	2, 3
V_{CC_LFM}	V_{CC} at Lowest Frequency Mode (LFM)	0.8		0.95	V	2, 3
$V_{CCDPRSLP}$	V_{CC} at Deeper Sleep (C4)	0.8		0.95	V	
$V_{CC,BOOT}$	Default V_{CC} voltage for initial power up	1.045	1.20	1.26	V	
I_{CC}	I_{CC} for processor core — N450/N455 — N470/N475 — N550 — N570			 5.77 6.04 11.54 11.54	A	
I_{AH}	I_{CC} Auto-Halt — N400 series — N500 series			 3.06 6.12	A	
I_{SGNT}	I_{CC} Stop-Grant — N400 series — N500 series			 3.03 6.06	A	
I_{DPRSLP}	I_{CC} Deeper Sleep (C4) — N400 series — N500 series			 2.04 4.08	A	
$SLOPE_{LL}$	Processor Core Supply Loadline		-5.9		mΩ	Figure 4-5

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Each processor is programmed with voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Please note this differs from the VID employed by the processor during a power management event.
3. The voltage specifications are assumed to be measured across VCC_SENSE and VSS_SENSE pins at socket with a 100-MHz bandwidth oscilloscope, 1.5-pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.

Figure 4-5. V_{CC} and I_{CC} Processor Loadline



The I/O buffer supply voltage should be measured at the processor package pins. The tolerances shown in Table 4-23 are inclusive of all noise from DC up to 20 MHz. The voltage rails should be measured with a bandwidth limited oscilloscope with a roll-off of 3 dB/decade above 20 MHz under all operating conditions. Table 4-23 indicates which supplies are connected directly to a voltage regulator or to a filtered voltage rail. For voltage rails that are connected to a filter, they should be measured at the input of the filter. If the recommended platform decoupling guidelines cannot be met, the system designer will have to make trade-offs between the voltage regulator out DC tolerance and the decoupling performances of the capacitor network to stay within the voltage tolerances listed below.

Table 4-23.Processor I/O Buffer Supply DC Voltage and Current Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{CCA}	Processor Core analog supply voltage (DC + AC specification)	1.425	1.5	1.575	V	
I_{CCA}	Processor Core analog supply current			0.080	A	
V_{CCGFX}	GFX supply voltage	0.8455	0.89	0.9345	V	
I_{CCGFX}	GFX supply current			2.64	A	
$V_{CCALVDS}$, $V_{CCDLVDS}$, $V_{CCACRTDAC}$	LVDS supply voltage CRT DAC supply voltage	1.71	1.8	1.89	V	
$I_{CCALVDS}$, $I_{CCDLVDS}$, $I_{CCACRTDAC}$	LVDS and CRT DAC supply current			0.15	A	
$V_{CCSFR\_DMIHMPLL}$, $V_{CCSFR\_AB\_DPL}$	DMIHMPLL supply voltage and Display PLL supply voltage	1.71	1.8	1.89	V	
$I_{CCSFR\_DMIHMPLL}$, $I_{CCSFR\_AB\_DPL}$	DMIHMPLL supply current and Display PLL supply current			0.18	A	
V_{CCSM}, V_{CCCK_DDR}	DDR I/O supply voltage and DDR Clock power supply voltage DDR2 DDR3	 1.71 1.425	 1.8 1.5	 1.89 1.575	V	
I_{CCSM}, I_{CCCK_DDR}	DDR I/O supply current (DDR2/DDR3) DDR Clock power supply current (DDR2/ DDR3)			2.00 0.27	A A	
V_{CCA_DMI}, V_{CCD_HMPLL}	DMI analog supply voltage and PLL supply voltage	0.9975	1.05	1.1025	V	
I_{CCA_DMI}, I_{CCD_HMPLL}	DMI analog supply current and PLL supply current			0.54	A	
$V_{CCD\_AB\_DPL}$, V_{CC_LGI}	Display PLL supply voltage and LGI supply voltage	0.9975	1.05	1.1025	V	
$I_{CCD\_AB\_DPL}$, I_{CC_LGI}	Display PLL supply current and LGI supply current			0.06	A	
V_{CCA_DDR}, V_{CCACK_DDR}	DDR analog supply voltage	0.9975	1.05	1.1025	V	
I_{CCA_DDR}, I_{CCACK_DDR}	DDR analog supply current DDR2 DDR3			 1.32 1.882	A	
V_{CCP}	Legacy I/O supply voltage	0.9975	1.05	1.1025	V	
I_{CCP}	Legacy I/O supply current			0.42	A	
V_{CCRING_EAST}, V_{CCRING_WEST}	DAC, GIO, LVDS supply voltage and LGIO supply voltage	0.9975	1.05	1.1025	V	

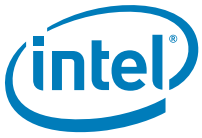


Table 4-23.Processor I/O Buffer Supply DC Voltage and Current Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Note
I_{CCRING_EAST}, I_{CCRING_WEST}	DAC, GIO, LVDS supply voltage and LGIO supply current			0.19	A	
V_{CC_GIO}	GIO supply voltage	3.135	3.3	3.465	V	
I_{CC_GIO}	GIO supply current			0.01	A	

4.10.2 Interface DC Specifications

Platform reference voltages at the top of Table 4-23 are specified at DC only. V_{REF} measurements should be made with respect to the supply voltage.

4.10.2.1 Input Clock DC Specification

Table 4-24.Input Clocks (BCLK, HPL_CLKIN, REFCLKIN, EXP_CLKIN) Differential Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
V_{IL}	Input Low Voltage	-0.30	0		V	
V_{IH}	Input High Voltage			1.15	V	
V_{CROSS}	Absolute crossing voltage	0.3		0.550	V	2
dV_{CROSS}	Range of crossing points			0.14	V	
C_{IN}	Input Capacitance	1.0		3.0	pF	

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Crossing voltage defined as instantaneous voltage when rising edge of CLKN equalise CLKP. The crossing point must meet the absolute and relative crossing point specification simultaneously.

4.10.2.2 DDR2/DDR3 DC Specifications

Table 4-25.DDR2/DDR3 Signal Group DC Specifications

Symbol	Parameter	Min (V)	Typ (V)	Max (V)	Units	Notes[1]
V_{IL}(DC)	Input Low Voltage			DDR_VREF - 0.2	V	2,4,9
V_{IH}(DC)	Input High Voltage	DDR_VREF + 0.2			V	3,9
V_{IL}(AC)	Input Low Voltage			DDR_VREF - 0.25	V	2,4,9
V_{IH}(AC)	Input High Voltage	DDR_VREF + 0.25			V	3,9

Table 4-25.DDR2/DDR3 Signal Group DC Specifications

Symbol	Parameter	Min (V)	Typ (V)	Max (V)	Units	Notes[1]
V_{OL}	Output Low Voltage DDR2 DDR3			 0.27 0.20		5
V_{OH}	Output High Voltage DDR2 DDR3	 1.47 1.22			V	4,5
I_{LI}	Input Leakage Current			10	µA	
V_{REF}	DDR Reference Voltage		V_{CCSM} / 2			7
$C_{I/O}$	DQ/DQS/DQS# DDR2 I/O Pin Capacitance	3.5	3.5	3.6	pF	

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4. V_{IH} and V_{OH} may experience excursions above V_{CCSM}. However, input signal drivers must comply with the signal quality specifications.
5. Measured at VCCSM(MIN).
6. The minimum and maximum values for these signals are programmable by BIOS
7. V_{CCSM} varies with typical/min/max cases. Refer Table 4-23 for details.
8. 2x Buffer Strength Settings is equal to a 20Ohm buffer setting.
9. DDR_VREF could either be from external or internal reference voltage.

4.10.2.3 LGIO Signal DC Specification

Table 4-26.GTL Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
V_{CCP}	I/O Voltage	1	1.05	1.1	V	
GTLREF	GTL Reference Voltage	2/3 V_{CCP}		2/3 V_{CCP}	V	6
R_{ODT}	On Die Termination		55		Ohm	10
V_{IH}	Input High Voltage	GTLREF + 0.1		V_{CCP} + 0.1	V	3,6
V_{IL}	Input Low Voltage	-0.1		GTLREF - 0.1	V	2,4
V_{OH}	Output High Voltage	V_{CCP} - 0.1		V_{CCP}	V	6

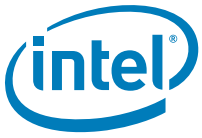


Table 4-26.GTL Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
R_{TT}	Termination Resistance	20	55	70	Ohm	7
R_{ON}	Buffer on Resistance	14	25	40	Ω	5
I_{LI}	Input Leakage Current	-100		100	µA	8
C_{PAD}	Pad Capacitance	2.35	2.5	2.6	pF	9

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. VIL is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. VIH is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical high value.
4. VIH and VOH may experience excursions above V_{CCP}. However, input signal drivers must comply with the signal quality specifications.
5. This is the pull-down driver resistance. Measured at 0.31 * V_{CCP}. R_{ON}(min) = 0.4 * R_{TT}, R_{ON}(typ) = 0.455 * R_{TT}, R_{ON}(max) = 0.51 * R_{TT}. R_{TT} typical value of 55 Ohm is used for R_{ON} typ/min/max calculations.
6. GTLREF is the on-die termination resistance measured at VOL of the output driver. Measured at 0.31 * V_{CCP}. The V_{CCP} referred to in these specifications is the instantaneous V_{CCP}.
7. R_{TT} is the on-die termination resistance measured at VOL of the output driver. Measured at 0.31 * V_{CCP}. R_{TT} is connected to V_{CCP} on die.
8. Specified with on-die R_{ON} and R_{TT} are turned off. Vin between 0 and V_{CCP}.
9. C_{PAD} includes die capacitance only. No package parasitic are included.
10. On die termination resistance, measured at 0.33 * V_{CCP}.

Table 4-27.Legacy CMOS Signal Group DC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
V_{CCP}	I/O Voltage	1.00	1.05	1.10	V	
V_{IH}	Input High Voltage	0.7 * V_{CCP}		V_{CCP} + 0.1	V	2
V_{IL}	Input Low Voltage	-0.1	0	0.3 * V_{CCP}	V	2, 3
V_{OH}	Output High Voltage	0.9 * V_{CCP}	V_{CCP}	V_{CCP} + 0.1	V	2, 4
V_{OL}	Output Low Voltage	-0.1		0.1 * V_{CCP}	V	2, 5
I_{LI}	Input Leakage Current	-100		100	uA	6
C_{PAD1}	Pad Capacitance	2.35	2.5	2.6	pF	7
C_{PAD2}	Pad Capacitance for CMOS Input	0.85	1.0	1.05	pF	8

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The V_{CCP} referred to in these specifications is the instantaneous V_{CCP}.
3. Refer to the processor I/O Buffer Models for I/V characteristics.
4. Measured at Iout = -1.1 mA.

5. Measured at Iout = 1.1 mA.
6. For V_{IN} between 0V and V_{CCP}. Measured when driver is tri-stated.
7. C_{PAD1} includes die capacitance only for CPUPWRGOOD. No package parasitic are included.
8. C_{PAD2} includes die capacitance for all other CMOS input signals. No package parasitics are included.

Table 4-28.Open Drain Signal Group DC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
V_{OH}	Output High Voltage	V_{CCP} - 5%		V_{CCP} + 5%	V	3
V_{OL}	Output Low Voltage	--		0.20	V	
I_{OL}	Output Low Current	16		60	mA	2
I_{LI}	Input Leakage Current	-200		200	uA	4
C_{PAD}	Pad Capacitance	1.8	2.1	2.6	pF	5

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Measured at 0.2V
3. VOH is determined by value of the external pull-up resistor to V_{CCP}.
4. For V_{IN} between 0V and V_{CCP}.
5. C_{PAD} includes die capacitance only. No package parasitic are included.

Table 4-29.PWROK and RSTIN# DC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes[1,2]
V_{IL}	Input Low Voltage	-0.3		0.8	V	2
V_{IH}	Input High Voltage	2.7		$VCC_{3.3}$*(1+ 5%)	V	2
L_I	Input Leakage Current			100	uA	
C_{PAD1}	Pad Capacitance			1.5	pF	

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IH} may experience excursions above V_{CCP}. However, input signal drivers must comply with the signal quality specifications.

Table 4-30.CPUPWRGOOD DC Specification

Symbol	Parameter	Min	Max	Units	Notes[1]
V_{IL}	Input Low Voltage	-0.1	0.3 * V_{CCP}	V	
V_{IH}	Input High Voltage	0.7 * V_{CCP}	V_{CCP} + 0.1	V	2
V_{HYS}	Hysteresis of Schmitt Trigger Inputs	100	--	mV	
L_I	Input Current of Each I/O Pin	-10	10	uA	
C_I	Capacitance of Each I/O Pin	--	1.5	pF	

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IH} may experience excursions above V_{CCP}. However, input signal drivers must comply with the signal quality specifications.

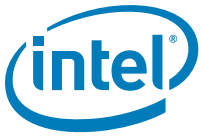


Table 4-31.DDR3_DRAM_PWROK DC Specification

Symbol	Parameter	Min	Max	Units	Notes[1]
V_{IL}	Input Low Voltage		0.29	V	
V_{IH}	Input High Voltage	1.25_P		V	2
I_{IL}	Inputs leakage current		20	uA	

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.

2. V_{IH} may experience excursions above V_{CCSM}. However, input signal drivers must comply with the signal quality specifications.

4.10.2.4 JTAG DC Specification

Table 4-32.TAP Signal Group DC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
RPD_{GTL}	GTL mode pull-down impedance (JTAG mode)		25		Ohm	
V_{T-}	Input fall transition threshold voltage	0.54* V_{CCP}	-	0.66* V_{CCP}	V	
V_{T+}	Input rise transition threshold voltage	0.74* V_{CCP}	-	0.86* V_{CCP}	V	
I_{LI}	Input Leakage Current			50	uA	

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.

4.10.2.5 Display DC Specification

The Analog Video Signal DC Specifications are referred to the VESA Video Signal Standard Version 1, Revision 2.

Table 4-33.CRT_DDC_DATA. CRT_DDC_CLK DC, LDDC_DATA, LDDC_CLK, LCTLA_CLK, and LCTLB_DATA Specification

Symbol	Parameter	Standard mode 100 kbits/s		Units	Notes[1]
		Min	Max		
V_{IL}	Input Low Voltage	-0.5	0.3 V_{CC_GIO}	V	
V_{IH}	Input High Voltage	0.7 V_{CC_GIO}	0.5 + V_{CC_GIO}	V	
V_{OL1}	Output Low Voltage - 1	0	0.4	V	2
L_I	Input Leakage Current	-50	50	uA	3
C_I	Capacitance	--	10	pF	

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. 3mA sink current.
3. 0.1 V_{CC_GIO} < V_{IN} < 0.9 $V_{CC\_GIO(MAX)}$

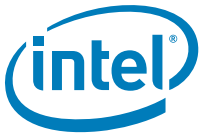


Table 4-34.CRT_HSYNC and CRT_VSYNC DC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
V_{OH}	Output High Voltage	2.4	--	V_{CC_GIO}	V	
V_{OL}	Output Low Voltage	0	--	0.5	V	
I_{OH}	Output High Current	--	--	8	mA	
I_{OL}	Output Low Current	--	--	8	mA	

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.

Table 4-35.LVDS Interface DC Specification (functional operating range, V_{CCLVDS} = 1.8V +/- 5%)

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
V_{OD}	Differential Output Voltage	250	350	450	mV	2
ΔV_{OD}	Change in V_{OD} between Complementary Output States			50	mV	2
V_{OS}	Offset Voltage	1.125	1.25	1.375	V	2
ΔV_{OS}	Change in V_{OS} between Complementary Output States			50	mV	2
I_{OS}	Output Short Circuit Current		-3.5	-10	mA	2
I_{OZ}	Output TRI-STATE Current		±1	±10	uA	2

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. All LVDS active lanes must be terminated with 100 Ohm resistor for correct V_{OS} performance and measurement.

Table 4-36.LVDD_EN, LBLKLT_EN and LBKLT_CTL DC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
V_{OL}	Output Low Voltage	0	--	0.4	V	2
V_{OH}	Output High Voltage	V_{CC_GIO} - 0.5	--	V_{CC_GIO}	V	2
I_L	Input Leakage	-50	--	50	uA	3

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. I_{CL}=6mA, I_{OH}=2mA
3. For power and unpowered devices.

§

5 Power Management

This chapter provides information on power management capabilities of the processor:

- ACPI States
- Processor Core States
- IGD (Integrated Graphics Devices) States
- IMC (Integrated Memory Controller) States
- DMI (Direct Media Interface) States

5.1 ACPI States Supported

The ACPI states supported by the processor are described in this section.

5.1.1 System States

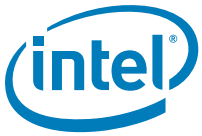
Table 5-37.System States

State	Description
G0/S0	Full On
G1/S3-Cold	Suspend-to-RAM (STR). Context saved to memory.
G1/S4	Suspend-to-Disk (STD). All power lost (except wakeup on chipset)
G2/S5	Soft off. All power lost (except wakeup on chipset)
G3	Mechanical/hard off. All power (AC and battery) removed from system

5.1.2 Processor Idle States

Table 5-38.Processor Core/Package States Support

State	Description
C0	Active mode, processor executing code
C1	AutoHALT state
C2	Stop Clock. Clock to processor is still running. Clock stopped to processor core
C4	Deeper Sleep. Clock to processor stopped with reduced voltage on the processor
C1E, C2E, C4E	Extended C-states; C1/C2/C4 states work together with Enhanced Intel® SpeedStep Technology



5.1.3 Integrated Graphics Display States

Table 5-39.Integrated Graphics Display Device Control

State	Description
D0	Display active
D3	Display power off

5.1.4 Integrated Memory Controller States

Table 5-40.Main Memory States

States	Description
Power-up	CKE asserted. Active mode
Precharge Powerdown	CKE de-asserted (not self-refresh) with all banks closed
Active Powerdown	CKE de-asserted (not self-refresh) with at least one bank active
Self-Refresh	CKE de-asserted using device self-refresh

5.1.5 DMI States

Table 5-41.DMI States

States	Description
L0	Full on – Active transfer state
L0s	First Active Power Management low power state – Low exit latency
L1	Lowest Active Power Management - Longer exit latency

5.1.6 Interface State Combinations

Table 5-42.G, S and C State combinations

Global (G) State	Sleep (S) State	Processor Core (C) State	Processor State	System Clocks	Description
G0	S0	C0	Full On	On	Full On
G0	S0	C1/C1E	Auto-Halt	On	Auto-Halt
G0	S0	C2/C2E	Stop-Grant	On	Stop-Grant
G0	S0	C4/C4E	Deeper Sleep	On	Deeper Sleep
G1	S3	Power off		Off except RTC	Suspend to RAM

Table 5-42.G, S and C State combinations

Global (G) State	Sleep (S) State	Processor Core (C) State	Processor State	System Clocks	Description
G1	S4	Power off	Power off	Off except RTC	Suspend to Disk
G2	S5	Power off	Power off	Off except RTC	Soft Off
G3	NA	Power Off	Power off	Power off	Hard Off

Table 5-43.D, S and C state Combinations

Graphics Adapter (D) State	Sleep (S) State	Package (C) State	Description
D0	S0	C0	Full On, Displaying
D0	S0	C1	Auto-Halt, Displaying
D0	S0	C2/C4	Stop Grant/Deeper Sleep, Displaying
D3	S0	Any	Not Displaying
D3	S3	---	Not Displaying, host core power off.
D3	S4	---	Not Displaying Suspend to disk Host core power off

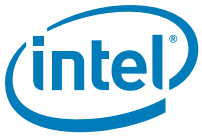
5.2 Processor Core Power Management

While executing code, Enhanced Intel® SpeedStep Technology optimizes the processor's frequency and core voltage based on workload. Each frequency and voltage operating point is defined by ACPI as a P-state. When the processor is not executing code, it is idle. A low-power idle state is defined by ACPI as a C-state. In general, lower power C-states have longer entry and exit latencies.

5.2.1 Enhanced Intel SpeedStep® Technology

The following are the key features of Enhanced Intel SpeedStep Technology:

- Multiple frequency and voltage points for optimal performance and power efficiency. These operating points are known as P-states.
- Frequency selection is software controlled by writing to processor MSRs. The voltage is optimized based on the selected frequency:
  - If the target frequency is higher than the current frequency, V_{CC} is ramped up in steps to an optimized voltage. This voltage is signaled by the VID pins to the voltage regulator. Once the voltage is established, the PLL locks on to the target frequency.
  - If the target frequency is lower than the current frequency, the PLL locks to the target frequency, then transitions to a lower voltage by signaling the target voltage on the VID pins.



— Software-requested transitions are accepted at any time. If a previous transition is in progress, the new transition is deferred until the previous transition is completed.

- The processor controls voltage ramp rates internally to ensure glitch-free transitions.
- Because there is low transition latency between P-states, a significant number of transitions per second are possible.
- Improved Thermal Monitor mode.
  - — When the on-die thermal sensor indicates that the die temperature is too high, the processor can automatically perform a transition to a lower frequency and voltage specified in a software programmable MSR.
  - — The processor waits for a fixed time period. If the die temperature is down to acceptable levels, an up transition to the previous frequency and voltage point occurs.
  - — An interrupt is generated for the up and down Intel Thermal Monitor transitions enabling better system level thermal management.

5.2.2 Dynamic Cache Sizing

Dynamic Cache Sizing allows the processor to flush and disable a programmable number of L2 cache ways upon each Deeper Sleep entry under the following condition:

- The C0 timer that tracks continuous residency in the Normal package state, has not expired. This timer is cleared during the first entry into Deeper Sleep to allow consecutive Deeper Sleep entries to shrink the L2 cache as needed.
- The predefined L2 shrink threshold is triggered.

The number of L2 cache ways disabled upon each Deeper Sleep entry is configured in the BBL_CR_CTL3 MSR. The C0 timer is referenced through the CLOCK_CORE_CST_CONTROL_STT MSR. The shrink threshold under which the L2 cache size is reduced is configured in the PMG_CST_CONFIG_CONTROL MSR. If the ratio is zero, then the ratio will not be taken into account for Dynamic Cache Sizing decisions.

5.2.3 Low-Power Idle States

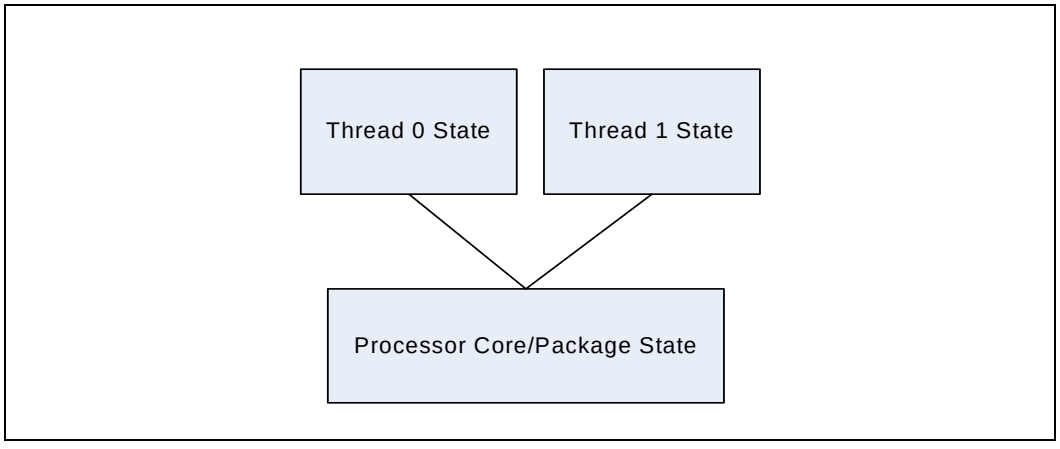
When the processor core is idle, low-power idle states (C-states) are used to save power. More power savings actions are taken for numerically higher C-states. However, higher C-states have longer exit and entry latencies. Resolution of C-states occur at the thread, processor core, and processor core package level. Thread level C-states are available if Hyper-Threading Technology is enabled.

5.2.3.1 Clock Control and Low-Power States

The processor core supports low power states at the thread level and core/package level. Thread states (TCx) loosely correspond to ACPI processor core power states (Cx). A thread may independently enter TC1/AutoHALT, TC1/MWAIT, TC2, TC3 and TC4 lower power states, but this does not always cause a power state transition. Only when both threads request a low-power state (TCx) greater than the current processor core state will a transition occur. The central power management logic ensures the entire processor core enters the new common processor core power state. For processor core power states higher than C1, this would be done by initiating a P_LVLx (P_LVL2, P_LVL3, P_LVL4) I/O read to both threads. Package states are states that require external intervention and typically map back to processor core power states. Package states for processor core include Normal (C0, C1), and Stop Grant, Stop Grant Snoop (C2), and Deeper Sleep (C4).

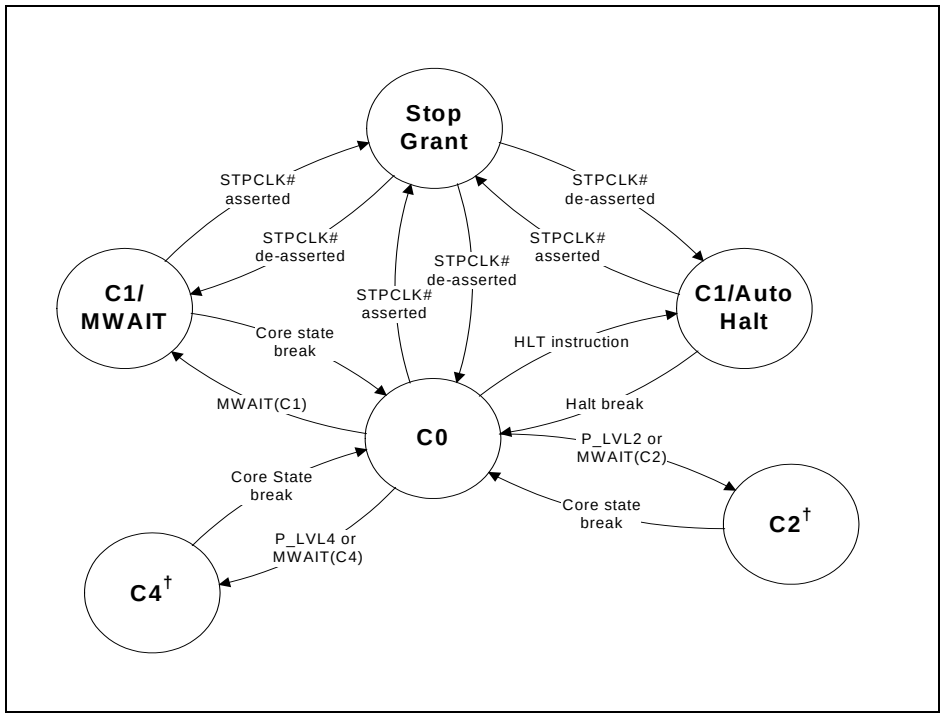
The processor core implements two software interfaces for requesting low power states: MWAIT instruction extensions with sub-state hints and P_LVLx reads to the ACPI P_BLK register block mapped in the processor core's I/O address space. The P_LVLx I/O reads are converted to equivalent MWAIT C-state requests inside the processor core and do not directly result in I/O reads on the processor core bus. The monitor address does not need to be setup before using the P_LVLx I/O read interface. The sub-state hints used for each P_LVLx read can be configured in a software programmable MSR by BIOS. If a thread encounters a chipset break even while STPCLK# is asserted, then it asserts the PBE# output signal. Assertion of PBE# (multifunction of FERR#) when STPCLK# is asserted indicates to system logic that individual threads should return to the C0 state and the processor core should return to the Normal state.

Figure 5-6. Idle Power Management Breakdown of the Processor Thread



Entry and exit of C-states at the thread and core level are show in Figure 5-7

Figure 5-7. Thread C-state



NOTES:

1. halt break = A20M# transition, INIT#, INTR, NMI, PREQ#, SMI# or APIC interrupt.
2. core state break = (halt break OR Monitor event) AND STPCLK# high (not asserted)
3. STPCLK# assertion and de-assertion have no effect if a thread is in C2 state.

Figure 5-8. Processor Core Low-power States

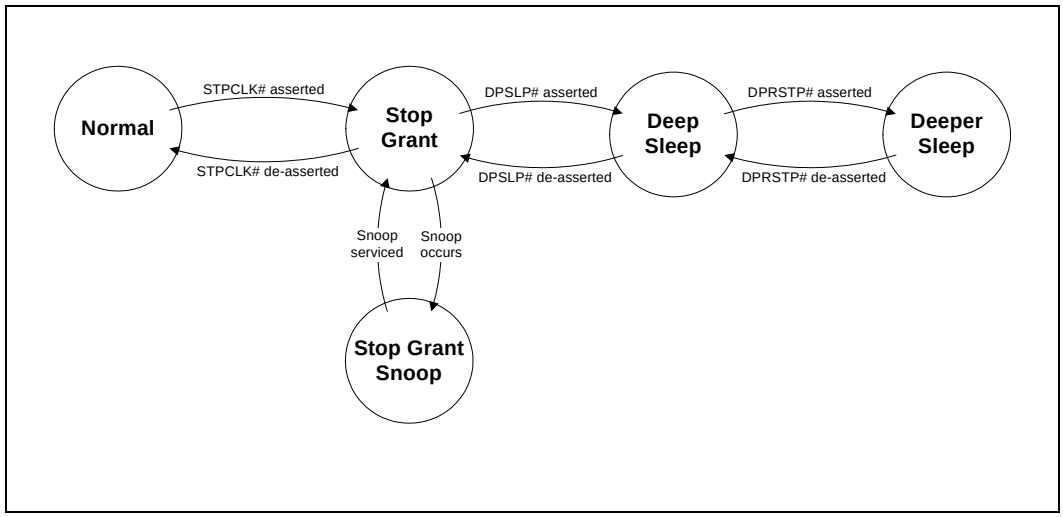


Table 5-44. Coordination of Thread Low-power States at the Package/Core Level

Processor Core C-State		Thread 1			
		C0	C1	C2	C4
Thread 0	C0	C0	C0	C0	C0
	C1	C0	C1[1]	C1[1]	C1[1]
	C2	C0	C1[1]	C2	C2
	C4	C0	C1[1]	C2	C4

NOTES:
1. AutoHALT or MWAIT/C1
2. To enter a package state, both threads must be in a common low power state. If the threads are not in a common low power state, the package state will resolve to the highest power C state.

5.2.4 Thread C-states Description

5.2.4.1 Thread C0 State

This is the normal operating state for threads in the processor core.

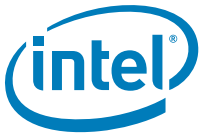
5.2.4.2 Thread C1/AutoHALT Powerdown State

C1/AutoHALT is a low-power state entered when one thread executes the HALT instruction while the other is in the TC1 or greater thread state. The processor core will transition to the C0 state upon occurrence of SMI#, INIT#, LINT00/LINT10 (NMI, INTR), or internal bus interrupt messages. RSTINB will cause the processor core to immediately initialize itself.

A System Management Interrupt (SMI) handler will return execution to either Normal state or the AutoHALT power down state. See the *Intel® 64 and IA-32 Architectures Software Developer's Manuals, Volume 3A/3B: System Programmer's Guide* for more information.

The system can generate STPCLK# while the processor core is in the AutoHALT power down state. When the system de-asserts the STPCLK# interrupt, the processor core will return to the HALT state.

While in AutoHalt power down state, the processor core will process bus snoops. The processor core will enter an internal snoopable sub-state to process the snoop and then return to the AutoHALT power down state.



5.2.4.3 Thread C1 / MWAIT Power-down State

C1/MWAIT is a low-power state entered when one thread executes the MWAIT (C1) instruction while the other thread is in the TC1 or greater thread state. processor core behavior in the MWAIT state is identical to the AutoHALT state except that Monitor events can cause the processor core to return to the C0 state. See the *Intel® 64 and IA-32 Architectures Software Developer's Manuals, Volume 2A: Instruction Set Reference, A-M and Volume 2B: Instruction Set Reference, N-Z,* for more information.

5.2.4.4 Thread C2 State

Individual threads of the dual-threaded processor can enter the C2 state by initiating a P_LVL2 I/O read to the P_BLK or an MWAIT(C2) instruction, but the processor will not issue a Stop-Grant Acknowledge special bus cycle unless the STPCLK# pin is also asserted.

While in the C2 state, the processor will process bus snoops and snoops from the other thread. The processor thread will enter a snoopable sub-state to process the snoop and then return to the C2 state.

5.2.4.5 Thread C4 State

Individual threads of the processor can enter the C4 state by initiating a P_LVL4 I/O read to the P_BLK or an MWAIT(C4) instruction. If both processor threads are in C4, the central power management logic will request that the entire processor enter the Deeper Sleep package low-power state.

To enable the package level Intel Enhanced Deeper Sleep state, Dynamic Cache Sizing and Intel Enhanced Deeper Sleep state fields must be configured in the PMG_CST_CONFIG_CONTROL MSR.

5.2.5 Processor Core / Package C-states Description

The following state descriptions assume that both threads are in a common low power state. For cases when only one thread is in a low power state, no change in Core/ Package power state will occur (see Section 5.2.3).

5.2.5.1 Normal State (C0, C1)

This is the normal operating state for the processor core. The processor core remains in the Normal state when the processor core is in the C0, C1/AutoHALT, or C1/MWAIT state. C0 is the active execution state.

5.2.5.2 C2 State

Individual threads of the dual-threaded processor core can enter TC2 state by initiating a P_LVL2 I/O read to the P_BLK or an MWAIT (C2) instruction. Once both threads have C2 as a common state, the processor core will transition to the C2 state; however, the processor core will not issue a Stop-Grant Acknowledge special bus cycle unless the STPCLK# pin is also asserted by the chipset.

While in the C2 state, the processor core will process bus snoops. The processor core will enter a snoopable sub-state described in the following section (and shown in Figure 31), to process the snoop and return to the C2 state.

5.2.5.2.1 Stop-Grant State

When STPCLK# pin is asserted, each thread of the processor cores enter the Stop-Grant state within 1384 bus clocks after the response phase of the processor-issued Stop-Grant Acknowledge special bus cycle. When the STPCLK# pin is deasserted, the core returns to its previous low-power state.

RSTIN# causes the processor core to immediately initialize itself, but the processor core will stay in Stop-Grant state. When RSTIN# is asserted by the system, the STPCLK#, DPSLP#, and DPRSTP# pins must be de-asserted prior to RSTIN# de-assertion.

While in Stop-Grant state, the processor core will service snoops and latch interrupts delivered on the internal bus. The processor core will latch SMI#, INIT# and LINT[1:0] interrupts and will service only one of each upon return to the Normal state.

The PBE# (FERR#) signal may be driven when the processor core is in Stop-Grant state. PBE# will be asserted if there is any pending interrupt or Monitor event latched within the processor core. Pending interrupts that are blocked by the EFLAGS. IF bit being clear will still cause assertion of PBE#. Assertion of PBE# indicates to system logic that the entire processor core should return to the Normal state.

A transition to the Stop-Grant Snoop state occurs when the processor core detects a snoop on the internal bus.

5.2.5.2.2 Stop-Grant Snoop State

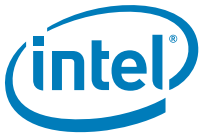
The processor core responds to snoop or interrupt transactions on the internal bus while in Stop-Grant state by entering the Stop-Grant Snoop state. The processor core will stay in this state until the snoop on the internal bus has been serviced (whether by the processor core or another agent on the internal bus) or the interrupt has been latched. The processor core returns to the Stop-Grant state once the snoop has been serviced or the interrupt has been latched.

5.2.5.3 Deep Sleep State

The Deep Sleep state is entered through assertion of the DPSLP# pin while in the Sleep state. BCLK may be stopped during the Deep Sleep state for additional platform level power savings. Deep Sleep State is mapped into the Deeper Sleep State for this processor.

BCLK stop/restart timings on appropriate chipset-based platforms with the clock chip are as follows:

- **Deep Sleep entry:** the system clock chip may stop/tri-state BCLK within 2 BCLKs of DPSLP# assertion. It is permissible to leave BCLK running during Deep Sleep.



- **Deep Sleep exit**: the system clock chip must start toggling BCLK within 10 BCLK periods within DPSLP# de-assertion.

5.2.5.4 Deeper Sleep State

The Deeper Sleep state is similar to the Deep Sleep state but further reduces core voltage levels. One of the potential lower core voltage levels is achieved by entering the base Deeper Sleep state. The Deeper Sleep state is entered through assertion of the DPRSTP# pin while in the Deep Sleep state.

In response to entering Deeper Sleep, the processor drives the VID code corresponding to the Deeper Sleep core voltage on the VID [6:0] pins.

Exit from Deeper Sleep is initiated by DPRSTP# de-assertion when the core requests a package state other than C4 or the core requests a processor performance state other than the lowest operating point.

5.2.5.5 Extended Low-Power States

Extended low-power states (C1E, C2E, C4E) optimize for power by forcibly reducing the performance state of the processor when it enters a package low-power state. Instead of directly transitioning into the package low-power state, the extended low-power state first reduces the performance state of the processor by performing an Enhanced Intel® SpeedStep Technology transition down to the lowest operating point. Upon receiving a break event from the package low-power state, control will be returned to software while an Enhanced Intel® SpeedStep Technology transition up to the initial operating point occurs. The advantage of this feature is that it significantly reduces leakage while in the package low power states. **Also, long-term reliability may not be assured if the Extended Low-Power States are not enabled.**

The processor implements two software interfaces for requesting extended package low-power states: MWAIT instruction extensions with sub-state hints and via BIOS by configuring IA32_MISC_ENABLES MSR bits to automatically promote package low-power states to extended package low-power states.

Extended Stop-Grant and Extended Deeper Sleep must be enabled via the BIOS for the processor to remain within specification. Not complying to this guideline may affect the long-term reliability of the processor.

Enhanced Intel® SpeedStep Technology transitions are multi-step processes that require clocked control. These transitions cannot occur when the processor is in the Sleep or Deep Sleep package low-power states since processor clocks are not active in these states. Extended Deeper Sleep is an exception to this rule when the Hard C4E configuration is enabled in the IA32_MISC_ENABLES MSR. This Extended Deeper Sleep state configuration will lower core voltage to the Deeper Sleep level while in Deeper Sleep and, upon exit, will automatically transition to the lowest operating voltage and frequency to reduce snoop service latency.

The transition to the lowest operating point or back to the original software requested point may not be instantaneous. Furthermore, upon very frequent transitions between active and idle states, the transitions may lag behind the idle state entry resulting in the processor either executing for a longer time at the lowest operating point or running idle at a high operating point. Observations and analyses show this behavior should not significantly impact total power savings or performance score while providing power benefits in most other cases.

5.3 External Thermal Sensor PM_EXTTS1#: Implementation for Fast C4/C4E Exit

Being used as DPRSLPVR is an alternate functionality for the PM_EXTTS1# signal. This implementation enables power savings by speeding up the C4 exit latency. To enable power savings, the PM_EXTTS1#/DPRSLPVR of the processor and the DPSLPVR signal of the chipset should be connected as shown in Figure 5-9 below. The DPRSLPVR signal of the chipset needs to be connected to the DPRSLPVR signal of the IMVP6 via a 500ohm series isolation resistor. The pull-up on the PM_EXTTS1# signal should be removed in this particular implementation.

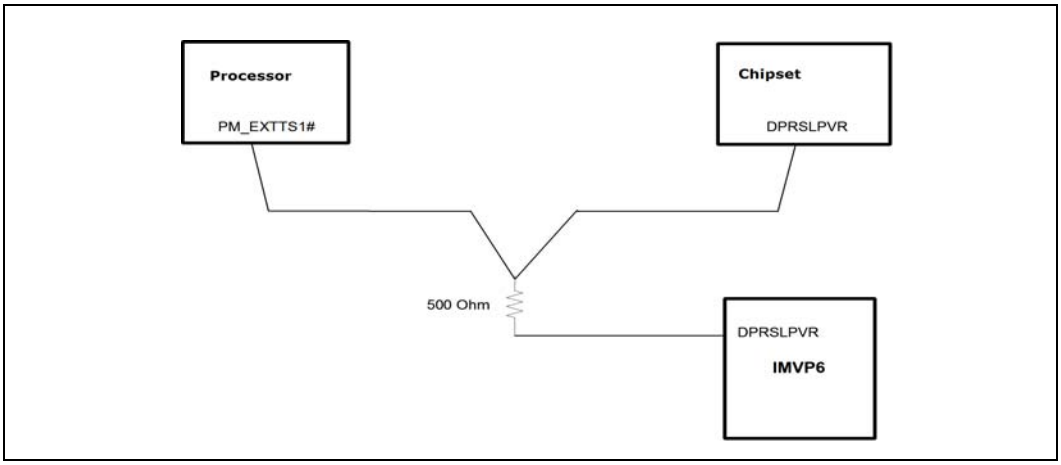
This implementation enables power-savings by increasing average C-state residency of the processor (The probability of the CPU going into C4/C4E state increases if the exit latency is reduced).

With this implementation, PM_EXTTS1# **cannot** be used for thermal throttling of Memory. If this implementation is chosen, system designers shall need to ensure that the memory Auto-refresh rate programmed on their systems is the most appropriate for their thermal solution and choice of memory.

Intel strongly recommends the implementation described above, to enable greater power savings on the processor. For details of the recommended routing topologies and guidelines, please contact your Intel Field Representative.

Note: PM_EXTTS0# cannot be used in this manner.

Figure 5-9. PM_EXTTS1# / DPSLPVR Implementation for Fast C4 / C4E Exit



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6 Thermal Specifications and Design Considerations

The processor requires a thermal solution to maintain temperatures within operating limits as set forth in Section Thermal Specifications. Any attempt to operate the processor outside these operating limits may result in permanent damage to the processor and potentially other components in the system. As processor technology changes, thermal management becomes increasingly crucial when building computer systems. Maintaining the proper thermal environment is key to reliable, long-term system operation.

A complete thermal solution includes both component and system level thermal management features. Component level thermal solutions include active or passive heatsink attached to the exposed processor die. The solution should make firm contact to the die while maintaining processor mechanical specifications such as pressure. A typical system level thermal solution may consist of a system fan used to evacuate or pull air through the system. Alternatively, the processor may be in a fan-less system, but would likely still use a multi-component heat spreader. Note that trading of thermal solutions also involves trading performance.

6.1 Thermal Specifications

To allow for the optimal operation and long-term reliability of Intel processor-based systems, the system/processor thermal solution should be designed such that the processor remains within the minimum and maximum junction temperature (Tj) specifications at the corresponding thermal design power (TDP) value listed in Table 6-45. Thermal solutions not designed to provide this level of thermal capability may affect the long-term reliability of the processor and system.

The maximum junction temperature is defined by an activation of the processor Thermal Monitor. Refer to Section 6.1.2 for more details. Analysis indicates that real applications are unlikely to cause the processor to consume the theoretical maximum power dissipation for sustained time periods. Intel recommends that complete thermal solution designs target the TDP indicated in Table 6-45 instead of the maximum processor power consumption. The Intel Thermal Monitor feature is designed to help protect the processor in the unlikely event that an application exceeds the TDP recommendation for a sustained period of time. For more details on the usage of this feature, refer to Section Section 6.1.2. In all cases the Intel Thermal Monitor feature must be enabled for the processor to remain within specification.

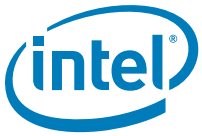


Table 6-45.Power Specifications for the Processor

Symbol	Processor Number	Core Frequency	Thermal Design Power			Unit	Notes
TDP	N450/N455 N470/N475	1.66 GHz 1.83 GHz	5.5/6.5 6.5			W	1, 2, 3
	N550 N570	1.5 GHz 1.66 GHz		6.5 6.5			
Symbol	**Parameter**		**Min**	**Typ**	**Max**	**Unit**	
Tj			0		100	(°C)	

NOTES:
1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
3. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.

The processor incorporates 3 methods of monitoring die temperature: Digital Thermal Sensor, Intel Thermal Monitor, and the Thermal Diode. The Intel Thermal Monitor (detailed in Section Section 6.1.2) must be used to determine when the maximum specified processor junction temperature has been reached.

6.1.1 Thermal Diode

The processor incorporates an on-die PNP transistor whose base emitter junction is used as a thermal “diode”, with its collector shorted to ground. The thermal diode can be read by an off-die analog/digital converter (a thermal sensor) located on the motherboard or a stand-alone measurement kit. The thermal diode may be used to monitor the die temperature of the processor for thermal management or instrumentation purposes but is not a reliable indication that the maximum operating temperature of the processor has been reached. See Section 6.1.2 for more details and thermal diode usage recommendation when the PROCHOT# signal is not asserted.

The reading of the external thermal sensor (on the motherboard) connected to the processor thermal diode signals will not necessarily reflect the temperature of the hottest location on the die. This is due to inaccuracies in the external thermal sensor, on-die temperature gradients between the location of the thermal diode and the hottest location on the die, and time based variations in the die temperature measurement. Time based variations can occur when the sampling rate of the thermal diode (by the thermal sensor) is slower than the rate at which the T_J temperature can change.

Offset between the thermal diode based temperature reading and the Intel Thermal Monitor reading may be characterized using the Intel Thermal Monitor's Automatic mode activation of the thermal control circuit. This temperature offset must be taken into account when using the processor thermal diode to implement power management events.

Table 6-46 and Table 6-47 provide the diode interface and specifications. Transistor model parameters shown in Table 6-47 providing more accurate temperature measurements when the diode ideality factor is closer to the maximum or minimum limits. Contact your external sensor supplier for their recommendation. The thermal diode is separate from the Thermal Monitor's thermal sensor and cannot be used to predict the behavior of the Thermal Monitor.

Table 6-46.Thermal Diode Interface

Signal Name	Pin/Ball Number	Signal Description
THRMDA_1	D30	Thermal diode anode
THRMDC_1	E30	Thermal diode cathode

Table 6-47.Thermal Diode Parameters using Transistor Model

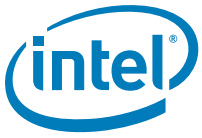
Symbol	Parameter	Min	Typ	Max	Unit	Notes
IFW	Forward Bias Current	5		200	µA	1
IE	Emitter Current	5		200	µA	1
nQ	Transistor Ideality	0.997	1.001	1.015		2,3,4
Beta		0.25		0.65		2,3
RT	Series Resistance	2.79	4.52	6.24	Ω	2,5

NOTES:
1. Intel does not support or recommend operation of the thermal diode under reverse bias.
2. Characterized across a temperature range of 50–100°C.
3. Not 100% tested. Specified by design characterization.
4. The ideality factor, nQ, represents the deviation from ideal transistor model behavior as exemplified by the equation for the collector current:

$$I_C = I_S * (e^{qV_{BE}/n_QkT} - 1)$$

   where I_S = saturation current, q = electronic charge, V_{BE} = voltage across the transistor base emitter junction (same nodes as VD), k = Boltzmann Constant, and T = absolute temperature (Kelvin).
5. The series resistance, R_T, provided in the Diode Model Table (Table 6-47) can be used for more accurate readings as needed.

When calculating a temperature based on the thermal diode measurements, a number of parameters must be either measured or assumed. Most devices measure the diode ideality and assume a series resistance and ideality trim value, although are capable of also measuring the series resistance. Calculating the temperature is then accomplished using the equations listed under Table 6-47. In most sensing devices, an expected value for the diode ideality is designed-in to the temperature calculation equation. If the designer of the temperature sensing device assumes a perfect diode, the ideality



value (also called n_{trim}) will be 1.000. Given that most diodes are not perfect, the designers usually select an n_{trim} value that more closely matches the behavior of the diodes in the processor. If the processor diode ideality deviates from that of the n_{trim}, each calculated temperature will be offset by a fixed amount. This temperature offset can be calculated with the equation:

$$T_{error(nf)} = T_{measured} * (1 - n_{actual}/n_{trim})$$

where $T_{error(nf)}$ is the offset in degrees C, $T_{measured}$ is in Kelvin, n_{actual} is the measured ideality of the diode, and n_{trim} is the diode ideality assumed by the temperature sensing device.

6.1.2 Intel® Thermal Monitor

The Intel Thermal Monitor helps control the processor temperature by activating the TCC (Thermal Control Circuit) when the processor silicon reaches its maximum operating temperature. The temperature at which the Intel Thermal Monitor activates the TCC is not user configurable. Bus traffic is snooped in the normal manner and interrupt requests are latched (and serviced during the time that the clocks are on) while the TCC is active.

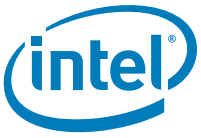
With a properly designed and characterized thermal solution, it is anticipated that the TCC would only be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be minor and hence not detectable. An under-designed thermal solution that is not able to prevent excessive activation of the TCC in the anticipated ambient environment may cause a noticeable performance loss and may affect the long-term reliability of the processor. In addition, a thermal solution that is significantly under designed may not be capable of cooling the processor even when the TCC is active continuously.

The Intel Thermal Monitor controls the processor temperature by modulating (starting and stopping) the processor core clocks when the processor silicon reaches its maximum operating temperature. The Intel Thermal Monitor uses two modes to activate the TCC: automatic mode and on-demand mode. If both modes are activated, automatic mode takes precedence.

There are two automatic modes called Intel Thermal Monitor-1 and Intel Thermal Monitor-2. These modes are selected by writing values to the MSRs of the processor. After automatic mode is enabled, the TCC will activate only when the internal die temperature reaches the maximum allowed value for operation.

The Intel Thermal Monitor automatic mode must be enabled through BIOS for the processor to be operating within specifications. Intel recommends TM1 and TM2 be enabled on the processors.

When TM1 is enabled and a high temperature situation exists, the clocks will be modulated by alternately turning the clocks off and on at a 50% duty cycle. Cycle times are processor speed dependent and will decrease linearly as processor core frequencies increase. Once the temperature has returned to a non-critical level, modulation ceases



and TCC goes inactive. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near the trip point. The duty cycle is factory configured and cannot be modified. Also, automatic mode does not require any additional hardware, software drivers, or interrupt handling routines. Processor performance will be decreased by the same amount as the duty cycle when the TCC is active.

When Intel Thermal Monitor-2 is enabled and a high temperature situation exists, the processor will perform an Enhanced Intel® SpeedStep Technology transition to the LFM. When the processor temperature drops below the critical level, the processor will make an Enhanced Intel® SpeedStep Technology transition to the last requested operating point.

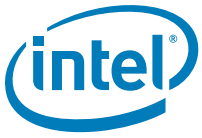
Intel Thermal Monitor-1 and Intel Thermal Monitor-2 can co-exist within the processor. If both Intel Thermal Monitor-1 and Intel Thermal Monitor-2 bits are enabled in the auto-throttle MSR, Intel Thermal Monitor-2 will take precedence over Intel Thermal Monitor-1.

However, if Force Intel Thermal Monitor-1 over Intel Thermal Monitor-2 is enabled in MSRs via BIOS and Intel Thermal Monitor-2 is not sufficient to cool the processor below the maximum operating temperature, then Intel Thermal Monitor-1 will also activate to help cool down the processor. If a processor load based Enhanced Intel® SpeedStep Technology transition (through MSR write) is initiated when a Intel Thermal Monitor-2 period is active, there are two possible results:

- If the processor load based Enhanced Intel® SpeedStep technology transition target frequency is **higher** than the Intel Thermal Monitor-2 transition based target frequency, the processor load-based transition will be deferred until the Intel Thermal Monitor-2 event has been completed.
- If the processor load-based Enhanced Intel® SpeedStep technology transition target frequency is **lower** than the Intel Thermal Monitor-2 transition based target frequency, the processor will transition to the processor load-based Enhanced Intel® SpeedStep technology target frequency point.

The TCC may also be activated via on-demand mode. If bit 4 of the ACPI Intel Thermal Monitor control register is written to a 1, the TCC will be activated immediately independent of the processor temperature. When using on-demand mode to activate the TCC, the duty cycle of the clock modulation is programmable via bits 3:1 of the same ACPI Intel Thermal Monitor control register. In automatic mode, the duty cycle is fixed at 50% on, 50% off, however in on-demand mode, the duty cycle can be programmed from 12.5% on/ 87.5% off, to 87.5% on/12.5% off in 12.5% increments. On-demand mode may be used at the same time automatic mode is enabled, however, if the system tries to enable the TCC via on-demand mode at the same time automatic mode is enabled and a high temperature condition exists, automatic mode will take precedence.

An external signal, PROCHOT# (processor hot) is asserted when the processor detects that its temperature is above the thermal trip point. Bus snooping and interrupt latching are also active while the TCC is active.



Besides the thermal sensor and thermal control circuit, the Intel Thermal Monitor also includes one ACPI register, one performance counter register, three MSR, and one I/O pin (PROCHOT#). All are available to monitor and control the state of the Intel Thermal Monitor feature. The Intel Thermal Monitor can be configured to generate an interrupt upon the assertion or deassertion of PROCHOT#.

PROCHOT# will not be asserted when the processor is in the low power states like Stop Grant and Deeper Sleep; hence, the thermal diode reading must be used as a safeguard to maintain the processor junction temperature within maximum specification. If the platform thermal solution is not able to maintain the processor junction temperature within the maximum specification, the system must initiate an orderly shutdown to prevent damage. If the processor enters one of the above power states with PROCHOT# already asserted, PROCHOT# will remain asserted until the processor exits the low power state and the processor junction temperature drops below the thermal trip point.

If Intel Thermal Monitor automatic mode is disabled, the processor will be operating out of specification. Regardless of enabling the automatic or on-demand modes, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached a temperature of approximately 125°C. At this point the THERMTRIP# signal will go active. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles. When THERMTRIP# is asserted, the processor core voltage must be shut down within the time specified.

6.1.3 Digital Thermal Sensor

The processor also contains an on die Digital Thermal Sensor (DTS) that can be read via an MSR (no I/O interface). The DTS is only valid while the processor is in the normal operating state (the Normal package level low power state).

Unlike traditional thermal devices, the DTS will output a temperature relative to the maximum supported operating temperature of the processor (T_{J_max}). It is the responsibility of software to convert the relative temperature to an absolute temperature. The temperature returned by the DTS will always be at or below T_{J_max}. Catastrophic temperature conditions are detectable via an Out Of Spec status bit. This bit is also part of the DTS MSR. When this bit is set, the processor is operating out of specification and immediate shutdown of the system should occur. The processor operation and code execution is not ensured once the activation of the Out of Spec status bit is set.

The DTS-relative temperature readout corresponds to the Thermal Monitor 1(TM1) and Thermal Monitor 2 (TM2) trigger points. When the DTS indicates maximum processor core temperature has been reached, the TM1 or TM2 hardware thermal control mechanism will activate. The DTS and TM1/TM2 temperature may not correspond to the thermal diode reading since the thermal diode is located in a separate portion of the die and thermal gradient between the DTS. Additionally, the thermal gradient from DTS to thermal diode can vary substantially due to changes in processor power,

mechanical and thermal attach, and software application. The system designer is required to use the DTS to ensure proper operation of the processor within its temperature operating specifications.

Changes to the temperature can be detected via two programmable thresholds located in the processor MSRs. These thresholds have the capability of generating interrupts via the core's local APIC. Refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* for specific register and programming details.

6.1.4 Out of Specification Detection

Overheat detection is performed by monitoring the processor temperature and temperature gradient. This feature is intended for graceful shut down before the THERMTRIP# is activated. If the processor's TM1 is triggered and the temperature remains high, an "Out Of Spec" status and sticky bit are latched in the status MSR register and generates thermal interrupt.

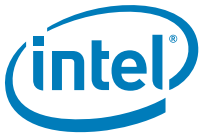
6.1.5 PROCHOT# Signal Pin

An external signal, PROCHOT# (processor hot), is asserted when the processor die temperature has reached its maximum operating temperature. If TM1 is enabled, then the TCC will be active when PROCHOT# is asserted. The processor can be configured to generate an interrupt upon the assertion or deassertion of PROCHOT#.

The processor implements a bi-directional PROCHOT# capability to allow system designs to protect various components from overheating situations. The PROCHOT# signal is bi-directional in that it can either signal when the processor has reached its maximum operating temperature or be driven from an external source to activate the TCC. The ability to activate the TCC via PROCHOT# can provide a means for thermal protection of system components.

Only a single PROCHOT# pin exists at a package level of the processor. When the core's thermal sensor trips, PROCHOT# signal will be driven by the processor package. If TM1 is enabled, PROCHOT# will be asserted and only the core that is above TCC temperature trip point will have its core clock modulated. If TM2 is enabled and the core is above TCC temperature trip point, it will enter the lowest programmed TM2 performance state. It is important to note that Intel recommends both TM1 and TM2 to be enabled.

When PROCHOT# is driven by an external agent and if only TM1 is enabled on the core, then the processor core will have the clocks modulated. If TM2 is enabled, then the processor core will enter the lowest programmed Intel Thermal Monitor-2 performance state. It should be noted that Force TM1 on TM2, enabled via BIOS, does not have any effect on external PROCHOT#. If PROCHOT# is driven by an external agent when TM1, TM2, and Force TM1 on TM2 are all enabled, then the processor will still apply only TM2.



PROCHOT# may be used for thermal protection of voltage regulators (VR). System designers can create a circuit to monitor the VR temperature and activate the TCC when the temperature limit of the VR is reached. By asserting PROCHOT# (pulled-low) and activating the TCC, the VR will cool down as a result of reduced processor power consumption. Bi-directional PROCHOT# can allow VR thermal designs to target maximum sustained current instead of maximum current. Systems should still provide proper cooling for the VR and rely on bi-directional PROCHOT# only as a backup in case of system cooling failure. The system thermal design should allow the power delivery circuitry to operate within its temperature specification even while the processor is operating at its TDP. With a properly designed and characterized thermal solution, it is anticipated that bi-directional PROCHOT# would only be asserted for very short periods of time when running the most power intensive applications.

An under-designed thermal solution that is not able to prevent excessive assertion of PROCHOT# in the anticipated ambient environment may cause a noticeable performance loss.

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7 Package Mechanical Specifications and Ball Information

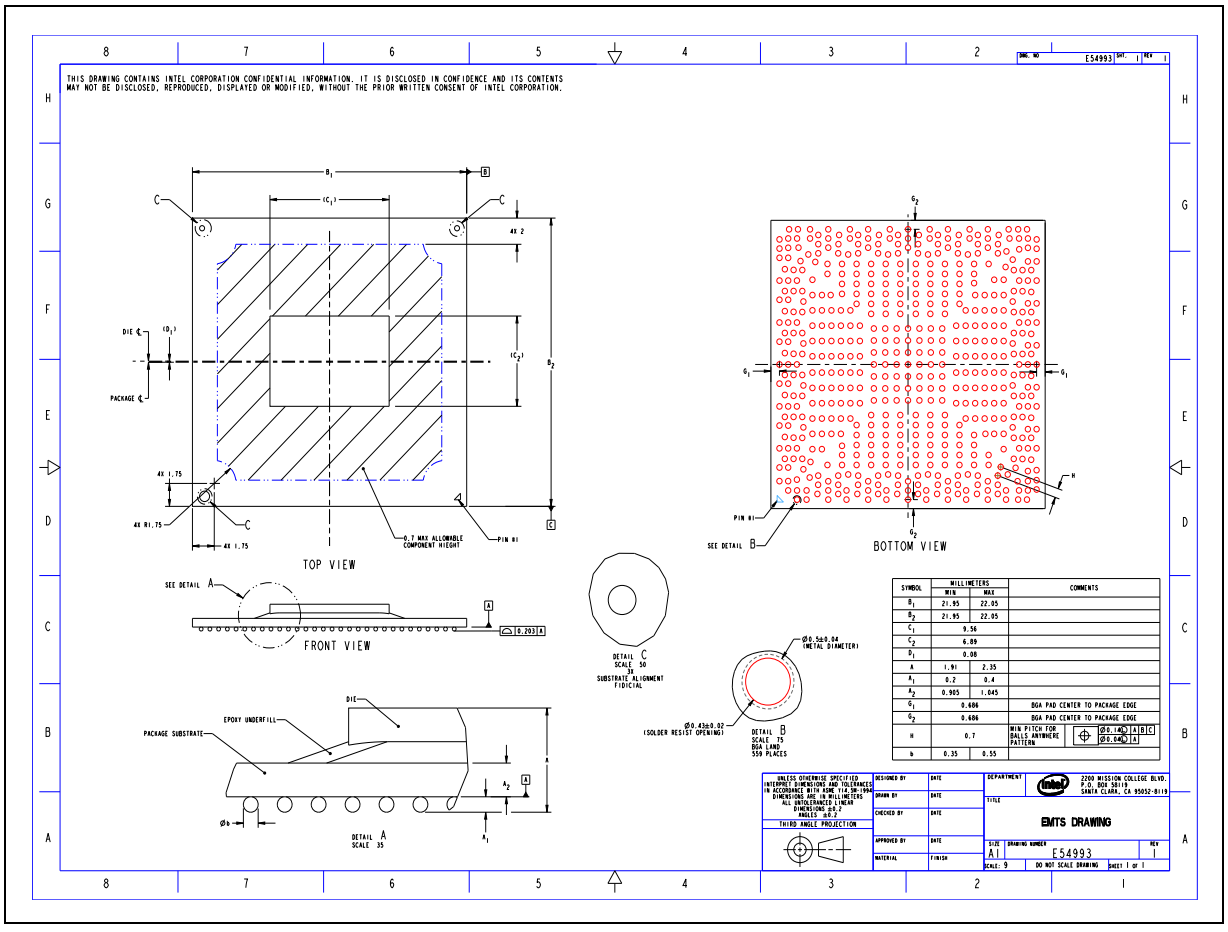
This chapter provides the package specifications, and ballout assignments.

7.1 Package Mechanical Specifications

The processor is available with 559 pins micro-FCBGA8 package. The package dimensions are shown in Figure 7-10.

7.1.1 Package Mechanical Drawings

Figure 7-10.Package Mechanical Drawings



7.1.2 Package Loading Specifications

Package loading is 15lb max static compressive.

7.2 Processor Ballout Assignment

Figure 7-10 to Figure 7-14 are graphic representations of the processor ballout assignments. Table 7-48 lists the ballout by signal name.

Figure 7-11.Package Pinmap (Top View, Upper-Left Quadrant)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	---	---	RSVD_NCTF	RSVD_NCTF	---	---	XDP_RSVD_1	---	XDP_RSVD_8	---	VSS	---	GTLREF	---	---	VSS
B	---	VCCRING_WEST	VCCP	VCCP	VSS	---	XDP_RSVD_7	XDP_RSVD_11	VSS	XDP_RSVD_15	XDP_RSVD_14	XDP_RSVD_16	VSS	TCK	---	VSS
C	RSVD_NCTF	VCCRING_WEST	VCCRING_WEST	---	XDP_RSVD_3	XDP_RSVD_5	XDP_RSVD_4	XDP_RSVD_10	---	XDP_RSVD_12	XDP_RSVD_17	VSS	---	TMS	---	TRST#
D	---	---	---	VCCP	---	XDP_RSVD_2	---	XDP_RSVD_6	XDP_RSVD_9	XDP_RSVD_13	---	XDP_RSVD_0	TDO	TDI	---	---
E	RSVD_NCTF	VCCP	---	---	IGNNE#	---	SMI#	VSS	---	VSS	PRDY#	---	THERMTRIP#	---	BPM_1_1#	---
F	---	DMI_RXN_0	DMI_RXP_0	VSS	---	---	---	STPCLK#	---	LINT0	LINT1	---	BPM_1_3#	---	PREQ#	---
G	DMI_TXN_0	DMI_TXP_0	DMI_RXN_1	---	RSVD	DPRSTP#	---	INIT#	---	DPSLP#	BPM_1_0#	---	BPM_1_2#	---	VSS	---
H	---	VSS	DMI_TXP_1	DMI_RXP_1	BSEL_1	FERR#	A20M#	VSS	---	BCLKN	VSS	---	RSVD	---	VSS	---
J	RSVD	DMI_TXN_1	---	VSS	---	---	---	---	---	BCLKP	VSS	---	VSS	---	VSS	---
K	---	RSVD	RSVD	VSS	BSEL_0	BSEL_2	EXTBGREF	VSS	RSVD_TP	---	VSS	---	VSS	---	VCC	---
L	VSS	RSVD	RSVD	---	PWROK	RSVD	RSVD	EXP_RBIAS	EXP_ICOMPI	EXP_RCOMPO	RSVD	---	VSS	VCC	---	VCC
M	---	RSVD	VSS	RSVD	---	---	---	---	---	---	---	---	---	---	---	---
N	VSS	RSVD	---	VSS	VSS	EXP_CLKINP	EXP_CLKINN	VSS	RSVD	RSVD	RSVD_TP	---	VSS	VCC	---	VCC
P	---	RSVD	VSS	VSS	---	---	---	---	---	---	RSVD_TP	---	VSS	VSS	---	VSS
R	---	---	---	---	RSVD_TP	RSVD_TP	VSS	VSS	RSVD	RSVD	---	---	---	---	---	---

Figure 7-12.Package Pinmap (Top View, Upper-Right Quadrant)

17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
---	---	VSS	---	VCC_LGI	---	VCC	---	VCC	---	VCC	---	RSVD_NCTF	RSVD_NCTF	---	A
---	BPM_2_0#/RSVD	VSS	BPM_2_1#/RSVD	BPM_2_3#/RSVD	VSS	VCC	VCC	VCC	VCC	VCC	---	VSSSENSE	RSVD_NCTF	RSVD_NCTF	B
---	PROCHOT#	---	BPM_2_2#/RSVD	VSS	VSS	---	VCC	VSS	VCC	---	---	VCCSENSE	THRMDA_2/RSVD	RSVD_NCTF	C
---	RSVD	RSVD_TP	RSVD	---	VSS	VCC	VCC	---	VCC	---	VCC	---	THRMDA_1	THRMDC_2/RSVD	D
RSVD	---	VSS	---	VSS	VCC	---	VCC	VSS	---	VCC	---	VID_6	THRMDC_1	---	E
VSS	---	VSS	---	VCC	VCC	---	VSS	VCC	---	---	VSS	VID_5	---	---	F
VSS	---	VCC	---	VCC	VSS	---	VCC	---	---	VSS	---	VID_4	VID_3	VSS	G
VCC	---	VCC	---	VSS	VCC	---	VCC	VSS	LVDD_EN	VSS	VID_2	VID_1	VID_0	---	H
VCC	---	VCC	---	VCC	VCC	---	---	---	---	---	LVBG	---	PM_EXTTS#_0	VCCRING_EAST	J
VCC	---	VSS	---	VCC	---	LDDC_CLK	LDDC_DATA	LCTLB_DATA	VSS	VSS	VSS	PM_EXTTS#_1/DPRSLPVR	VSS	---	K
---	VSS	VCC	---	VCC	VSS	LCTLA_CLK	VSS	VSS	LBKLT_CTL	LBKLT_EN	---	VSS	CRT_DDC_CLK	CRT_DDC_DATA	L
---	---	---	---	---	---	---	---	---	---	---	VSS	CRT_VSYNC	CRT_HSYNC	---	M
---	VSS	VCC	---	VCC	LVREFH	LVREFL	VSS	VSS	LA_DATAN_1	LA_DATAP_1	VSS	---	CRT_IRTN	CRT_RED	N
---	VSS	VSS	---	VSS	---	---	---	---	---	---	DAC_IREF	CRT_BLUE	CRT_GREEN	---	P
---	---	---	---	---	LIBG	LA_DATAN_0	LA_DATAP_0	VSS	LA_DATAN_2	LA_DATAP_2	---	---	---	---	R

Figure 7-13.Package Pinmap (Top View, Lower-Left Quadrant)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
T	VCCA_DMI	VCCA_DMI	VCCA_DMI	---	---	---	---	---	---	---	VSS	---	VCCGFX	VCCGFX	---	VCCGFX
U	---	---	---	---	VCCA_DDR	VCCA_DDR	VCCA_DDR	VCCA_DDR	VCCA_DDR	VCCA_DDR	---	---	---	---	---	---
V	---	VCCA_DDR	VCCA_DDR	VCCA_DDR	---	---	---	---	---	---	VCCD_HMPLL	---	VCCGFX	VSS	---	VSS
W	CPUPWRGOOD	VSS	---	VSS	VSS	VSS	VSS	HPL_CLKINN	HPL_CLKINP	VCCA_DDR	VCCA_DDR	---	VSS	VCCGFX	---	VCCGFX
Y	---	VCCA	VSS	VSS	---	---	---	---	---	---	---	---	---	---	---	---
AA	VCCSFR_DMIHMPLL	VSS	RSTIN#	---	DDR_A_DQ_12	RSVD_TP	RSVD_TP	VSS	DDR_A_DM_1	VCCACK_DDR	VCCACK_DDR	---	VSS	VSS	---	VSS
AB	---	DDR_A_DQ_4	DDR_A_DQ_5	DDR3_DRAM_PWROK	DDR_A_DQ_13	DDR_A_DQ_8	DDR_A_DQ_9	DDR_A_DQS_1	DDR_A_DQ_14	---	RSVD_TP	---	RSVD_TP	---	RSVD	---
AC	DDR_A_DQ_1	VSS	---	DDR_A_DQ_0	---	---	---	---	---	VSS	VSS	---	DDR_A_CK#_1	---	DDR_A_CK_3	---
AD	---	DDR_A_DQS#_0	DDR_A_DQS_0	DDR_A_DM_0	VSS	DDR_A_DQ_15	DDR_A_DQS#_1	DDR_A_DQS_2	---	DDR_A_DQS#_2	DDR_A_DQ_22	---	DDR_A_CK_1	---	DDR_A_CK#_3	---
AE	VSS	DDR_A_DQ_6	DDR_A_DQ_7	---	DDR_A_DQ_10	---	---	DDR_A_DM_2	---	DDR_A_DQ_23	VSS	---	VSS	---	VSS	---
AF	---	---	DDR_A_DQ_28	DDR_A_DQ_2	---	---	DDR_A_DQ_20	DDR_A_DQ_21	---	DDR_A_DQ_18	VSS	---	DDR_A_CK_4	---	DDR_A_CK#_0	---
AG	---	DDR_A_DQ_3	VSS	---	DDR_A_DQ_11	---	DDR_A_DQ_17	DDR_A_DQ_16	---	VSS	DDR_A_DQ_19	---	DDR_A_CK#_4	---	DDR_A_CK_0	---
AH	DDR_A_DQ_24	DDR_A_DQ_29	---	VSS	---	VSS	---	VSS	DDR_A_CKE_1	DDR_A_CKE_0	---	DDR_A_MA_11	DDR_A_MA_8	DDR_A_MA_5	---	---
AJ	RSVD_NCTF	DDR_A_DQ_25	DDR_A_DM_3	---	---	DDR_A_DQ_31	DDR_A_DQ_27	DDR_A_CKE_3	---	DDR_A_MA_14	DDR_A_MA_12	DDR_A_MA_7	---	DDR_A_MA_4	---	VSS
AK	RSVD_NCTF	RSVD_NCTF	DDR_A_DQS#_3	---	DDR_A_DQS_3	DDR_A_DQ_26	VCCCK_DDR	DDR3_DRAMRST#	VCCSM	DDR_A_CKE_2	DDR_A_BS_2	DDR_A_MA_9	VCCSM	DDR_A_MA_6	---	DDR_A_MA_3
AL	---	RSVD_NCTF	RSVD_NCTF	---	DDR_A_DQ_30	---	VCCCK_DDR	---	VSS	---	VCCSM	---	VSS	---	---	VCCSM

Figure 7-14.Package Pinmap (Top View, Lower-Right Quadrant)

---	VCCGFX	VCCGFX	---	RSVD_TP	---	---	---	---	---	---	---	VSS	VCCACRTDAC	VCC_GIO	T
---	---	---	---	---	VSS	VSS	VSS	LA_CLKN	LA_CLKP	VSS	---	---	---	---	U
---	VSS	VCCGFX	---	RSVD_TP	---	---	---	---	---	---	VSS	VSS	VCCALVDS	---	V
---	VCCGFX	VCCGFX	---	RSVD_TP	DDR_A_DQ_59	VSS	DDR_A_DQ_58	VSS	VSS	DDR_A_DQ_63	VSS	---	VSS	VCCDLVDS	W
---	---	---	---	---	---	---	---	---	---	---	VSS	REFCLKINN	REFCLKINP	---	Y
---	VSS	VCCD_AB_DPL	---	RSVD_TP	VSS	DDR_A_DQ_62	DDR_A_DQ_56	VSS	VSS	DDR_A_DQS#_7	---	VSS	REFSSCLKINP	REFSSCLKINN	AA
RSVD	---	VSS	---	VSS	---	DDR_A_DQ_61	DDR_A_DQ_60	DDR_A_DQ_57	DDR_A_DM_7	DDR_A_DQS_7	VSS	VSS	VSS	---	AB
RSVD	---	VSS	---	VSS	DDR_A_DQ_44	---	---	---	---	---	VSS	---	VSS	VCCSFR_AB_DPL	AC
RSVD	---	DDR_A_DM_4	---	DDR_A_DQ_39	DDR_A_DQ_35	---	DDR_A_DQ_43	DDR_A_DQ_42	VSS	DDR_A_DQ_46	DDR_A_DQ_55	DDR_A_DQ_51	DDR_A_DQ_50	---	AD
VSS	---	DDR_A_DQ_32	---	DDR_A_DQ_38	VSS	---	DDR_A_DQ_40	---	DDR_A_DQS_5	DDR_A_DQ_47	---	DDR_A_DQ_54	DDR_A_DQS_6	VSS	AE
VSS	---	DDR_A_DQ_37	---	VSS	DDR_A_DQ_34	---	VSS	---	---	---	VSS	DDR_A_DQS#_6	DDR_A_DM_6	---	AF
DDR_A_DQ_36	---	DDR_A_DQ_33	---	DDR_A_DQS#_4	DDR_A_DQS_4	---	DDR_A_DQ_45	DDR_A_DQ_41	---	DDR_A_DQS#_5	---	---	DDR_A_DQ_49	DDR_A_DQ_48	AG
---	VSS	DDR_A_MA_0	DDR_A_BS_1	---	DDR_A_CS#_0	VSS	DDR_A_ODT_2	---	DDR_A_ODT_1	---	VSS	---	---	---	AH
---	DDR_A_MA_1	---	DDR_A_BS_0	DDR_A_CS#_2	DDR_A_CAS#	---	DDR_A_MA_13	DDR_A_CS#_3	DDR_RPU	DDR_A_DM_5	---	DDR_A_DQ_53	DDR_A_DQ_52	RSVD_NCTF	AJ
---	DDR_A_MA_2	VCCSM	DDR_A_MA_10	DDR_A_RAS#	DDR_A_WE#	VSS	DDR_A_ODT_0	DDR_A_CS#_1	---	DDR_A_ODT_3	DDR_RPD	RSVD	RSVD_NCTF	RSVD_NCTF	AK
---	---	VSS	---	VCCSM	---	VSS	---	VCCSM	---	---	DDR_VREF	RSVD_NCTF	RSVD_NCTF	---	AL
17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	

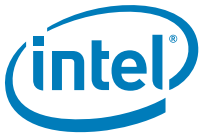


Table 7-48.Processor Ball List by Ball Name (Sheet 1 of 9)

Pin Name	Pin Number	Type	Dir.
A20M#	H7	CPU legacy	I/O
BCLKN	H10	CPU legacy	I
BCLKP	J10	CPU legacy	I
BPM_1_0#	G11	CPU legacy	I/O
BPM_1_1#	E15	CPU legacy	I/O
BPM_1_2#	G13	CPU legacy	I/O
BPM_1_3#	F13	CPU legacy	I/O
BPM_2_0#/ RSVD	B18	CPU legacy	I/O
BPM_2_1#/ RSVD	B20	CPU legacy	I/O
BPM_2_2#/ RSVD	C20	CPU legacy	I/O
BPM_2_3#/ RSVD	B21	CPU legacy	I/O
BSEL_0	K5	CPU legacy	I/O
BSEL_1	H5	CPU legacy	I/O
BSEL_2	K6	CPU legacy	I/O
CPUPWRGOOD	W1	CPU legacy	I
CRT_BLUE	P29	CRTDAC	O
CRT_DDC_CLK	L30	CRTDAC	I/O
CRT_DDC_DAT A	L31	CRTDAC	I/O
CRT_GREEN	P30	CRTDAC	O
CRT_HSYNC	M30	CRTDAC	O
CRT_IRTN	N30	CRTDAC	O
CRT_RED	N31	CRTDAC	O
CRT_VSYNC	M29	CRTDAC	O
DAC_IREF	P28	CRTDAC	I/O
DDR_A_BS_0	AJ20	MEM_Cntl_A	O
DDR_A_BS_1	AH20	MEM_Cntl_A	O
DDR_A_BS_2	AK11	MEM_Cntl_A	O
DDR_A_CAS#	AJ22	MEM_Cntl_A	O
DDR_A_CK_0	AG15	MEM_Clk_A	O
DDR_A_CK_1	AD13	MEM_Clk_A	O
RSVD	AD17	N/A	N/A
DDR_A_CK_3	AC15	MEM_Clk_A	O

Pin Name	Pin Number	Type	Dir.
RSVD	AB17	N/A	N/A
DDR_A_CKE_0	AH10	MEM_Cntl_A	O
DDR_A_CKE_1	AH9	MEM_Cntl_A	O
DDR_A_CKE_2	AK10	MEM_Cntl_A	O
DDR_A_CKE_3	AJ8	MEM_Cntl_A	O
DDR_A_CS#_0	AH22	MEM_Cntl_A	O
DDR_A_CS#_1	AK25	MEM_Cntl_A	O
DDR_A_CS#_2	AJ21	MEM_Cntl_A	O
DDR_A_CS#_3	AJ25	MEM_Cntl_A	O
DDR_A_DM_0	AD4	MEM_Ad	O
DDR_A_DM_1	AA9	MEM_Ad	O
DDR_A_DM_2	AE8	MEM_Ad	O
DDR_A_DM_3	AJ3	MEM_Ad	O
DDR_A_DM_4	AD19	MEM_Ad	O
DDR_A_DM_5	AJ27	MEM_Ad	O
DDR_A_DM_6	AF30	MEM_Ad	O
DDR_A_DM_7	AB26	MEM_Ad	O
DDR_A_DQ_0	AC4	MEM_Ad	I/O
DDR_A_DQ_1	AC1	MEM_Ad	I/O
DDR_A_DQ_10	AE5	MEM_Ad	I/O
DDR_A_DQ_11	AG5	MEM_Ad	I/O
DDR_A_DQ_12	AA5	MEM_Ad	I/O
DDR_A_DQ_13	AB5	MEM_Ad	I/O
DDR_A_DQ_14	AB9	MEM_Ad	I/O
DDR_A_DQ_15	AD6	MEM_Ad	I/O
DDR_A_DQ_16	AG8	MEM_Ad	I/O
DDR_A_DQ_17	AG7	MEM_Ad	I/O
DDR_A_DQ_18	AF10	MEM_Ad	I/O
DDR_A_DQ_19	AG11	MEM_Ad	I/O
DDR_A_DQ_2	AF4	MEM_Ad	I/O
DDR_A_DQ_20	AF7	MEM_Ad	I/O
DDR_A_DQ_21	AF8	MEM_Ad	I/O

Table 7-48.Processor Ball List by Ball Name (Sheet 2 of 9)

Pin Name	Pin Number	Type	Dir.	Pin Name	Pin Number	Type	Dir.
DDR_A_CK_4	AF13	MEM_Clk_A	O	DDR_A_DQ_22	AD11	MEM_Ad	I/O
RSVD	AB15	N/A	N/A	DDR_A_DQ_23	AE10	MEM_Ad	I/O
DDR_A_CK_0#	AF15	MEM_Clk_A	O	DDR_A_DQ_24	AH1	MEM_Ad	I/O
DDR_A_CK_1#	AC13	MEM_Clk_A	O	DDR_A_DQ_25	AJ2	MEM_Ad	I/O
RSVD	AC17	N/A	N/A	DDR_A_DQ_26	AK6	MEM_Ad	I/O
DDR_A_CK_3#	AD15	MEM_Clk_A	O	DDR_A_DQ_27	AJ7	MEM_Ad	I/O
DDR_A_CK_4#	AG13	MEM_Clk_A	O	DDR_A_DQ_28	AF3	MEM_Ad	I/O
DDR_A_DQ_29	AH2	MEM_Ad	I/O	DDR_A_DQ_8	AB6	MEM_Ad	I/O
DDR_A_DQ_3	AG2	MEM_Ad	I/O	DDR_A_DQ_9	AB7	MEM_Ad	I/O
DDR_A_DQ_30	AL5	MEM_Ad	I/O	DDR_A_DQS_0	AD3	MEM_Ad	O
DDR_A_DQ_31	AJ6	MEM_Ad	I/O	DDR_A_DQS_1	AB8	MEM_Ad	O
DDR_A_DQ_32	AE19	MEM_Ad	I/O	DDR_A_DQS_2	AD8	MEM_Ad	O
DDR_A_DQ_33	AG19	MEM_Ad	I/O	DDR_A_DQS_3	AK5	MEM_Ad	O
DDR_A_DQ_34	AF22	MEM_Ad	I/O	DDR_A_DQS_4	AG22	MEM_Ad	O
DDR_A_DQ_35	AD22	MEM_Ad	I/O	DDR_A_DQS_5	AE26	MEM_Ad	O
DDR_A_DQ_36	AG17	MEM_Ad	I/O	DDR_A_DQS_6	AE30	MEM_Ad	O
DDR_A_DQ_37	AF19	MEM_Ad	I/O	DDR_A_DQS_7	AB27	MEM_Ad	O
DDR_A_DQ_38	AE21	MEM_Ad	I/O	DDR_A_DQS#_0	AD2	MEM_Ad	O
DDR_A_DQ_39	AD21	MEM_Ad	I/O	DDR_A_DQS#_1	AD7	MEM_Ad	O
DDR_A_DQ_4	AB2	MEM_Ad	I/O	DDR_A_DQS#_2	AD10	MEM_Ad	O
DDR_A_DQ_40	AE24	MEM_Ad	I/O	DDR_A_DQS#_3	AK3	MEM_Ad	O
DDR_A_DQ_41	AG25	MEM_Ad	I/O	DDR_A_DQS#_4	AG21	MEM_Ad	O
DDR_A_DQ_42	AD25	MEM_Ad	I/O	DDR_A_DQS#_5	AG27	MEM_Ad	O
DDR_A_DQ_43	AD24	MEM_Ad	I/O	DDR_A_DQS#_6	AF29	MEM_Ad	O
DDR_A_DQ_44	AC22	MEM_Ad	I/O	DDR_A_DQS#_7	AA27	MEM_Ad	O
DDR_A_DQ_45	AG24	MEM_Ad	I/O	DDR_A_MA_0	AH19	MEM_Cntl_A	O
DDR_A_DQ_46	AD27	MEM_Ad	I/O	DDR_A_MA_1	AJ18	MEM_Cntl_A	O
DDR_A_DQ_47	AE27	MEM_Ad	I/O	DDR_A_MA_10	AK20	MEM_Cntl_A	O
DDR_A_DQ_48	AG31	MEM_Ad	I/O	DDR_A_MA_11	AH12	MEM_Cntl_A	O
DDR_A_DQ_49	AG30	MEM_Ad	I/O	DDR_A_MA_12	AJ11	MEM_Cntl_A	O
DDR_A_DQ_5	AB3	MEM_Ad	I/O	DDR_A_MA_13	AJ24	MEM_Cntl_A	O
DDR_A_DQ_50	AD30	MEM_Ad	I/O	DDR_A_MA_14	AJ10	MEM_Cntl_A	O
DDR_A_DQ_51	AD29	MEM_Ad	I/O	DDR_A_MA_2	AK18	MEM_Cntl_A	O
DDR_A_DQ_52	AJ30	MEM_Ad	I/O	DDR_A_MA_3	AK16	MEM_Cntl_A	O
DDR_A_DQ_53	AJ29	MEM_Ad	I/O	DDR_A_MA_4	AJ14	MEM_Cntl_A	O
DDR_A_DQ_54	AE29	MEM_Ad	I/O	DDR_A_MA_5	AH14	MEM_Cntl_A	O

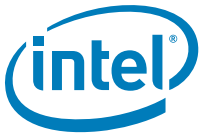


Table 7-48.Processor Ball List by Ball Name (Sheet 3 of 9)

Pin Name	Pin Number	Type	Dir.
DDR_A_DQ_55	AD28	MEM_Ad	I/O
DDR_A_DQ_56	AA24	MEM_Ad	I/O
DDR_A_DQ_57	AB25	MEM_Ad	I/O
DDR_A_DQ_58	W24	MEM_Ad	I/O
DDR_A_DQ_59	W22	MEM_Ad	I/O
DDR_A_DQ_6	AE2	MEM_Ad	I/O
DDR_A_DQ_60	AB24	MEM_Ad	I/O
DDR_A_DQ_61	AB23	MEM_Ad	I/O
DDR_A_DQ_62	AA23	MEM_Ad	I/O
DDR_A_WE#	AK22	MEM_Cntl_A	O
DDR_RPD	AK28	MEM_Ana	I/O
DDR_A_DQ_63	W27	MEM_Ad	I/O
DDR_A_DQ_7	AE3	MEM_Ad	I/O
DDR_RPU	AJ26	MEM_Ana	I/O
RSVD	AK29	N/A	N/A
DDR_VREF	AL28	MEM_Ana	I
DMI_RXN_0	F2	3GIO_CTC_rx	I
DMI_RXN_1	G3	3GIO_CTC_rx	I
RSVD	J1	N/A	N/A
RSVD	L3	N/A	N/A
DMI_RXP_0	F3	3GIO_CTC_rx	I
DMI_RXP_1	H4	3GIO_CTC_rx	I
RSVD	K2	N/A	N/A
RSVD	M4	N/A	N/A
DMI_TXN_0	G1	3GIO_CTC_tx	O
DMI_TXN_1	J2	3GIO_CTC_tx	O
RSVD	L2	N/A	N/A
RSVD	N2	N/A	N/A
DMI_TXP_0	G2	3GIO_CTC_tx	O
DMI_TXP_1	H3	3GIO_CTC_tx	O
RSVD	K3	N/A	N/A
RSVD	M2	N/A	N/A
REFCLKINN	Y29	Display PLL	I
REFCLKINP	Y30	Display PLL	I
DPRSTP#	G6	CPU_sideband	I

Pin Name	Pin Number	Type	Dir.
DDR_A_MA_6	AK14	MEM_Cntl_A	O
DDR_A_MA_8	AH13	MEM_Cntl_A	O
DDR_A_MA_9	AK12	MEM_Cntl_A	O
DDR_A_ODT_0	AK24	MEM_Cntl_A	O
DDR_A_ODT_1	AH26	MEM_Cntl_A	O
DDR_A_ODT_2	AH24	MEM_Cntl_A	O
DDR_A_ODT_3	AK27	MEM_Cntl_A	O
DDR_A_RAS#	AK21	MEM_Cntl_A	O
INIT#	G8	CPU_sideband	I/O
LBKLT_CTL	L26	LVDS	O
LBKLT_EN	L27	LVDS	O
LCTLA_CLK	L23	LVDS	I/O
LCTLB_DATA	K25	LVDS	I/O
LDDC_CLK	K23	LVDS	I/O
LDDC_DATA	K24	LVDS	I/O
LINT0	F10	CPU_sideband	I
LINT1	F11	CPU_sideband	I
LA_CLKN	U25	LVDS	O
LA_CLKP	U26	LVDS	O
LA_DATAN_0	R23	LVDS	O
LA_DATAN_1	N26	LVDS	O
LA_DATAN_2	R26	LVDS	O
LA_DATAP_0	R24	LVDS	O
LA_DATAP_1	N27	LVDS	O
LA_DATAP_2	R27	LVDS	O
LIBG	R22	LVDS	I/O
LVBG	J28	LVDS	O
LVREFH	N22	LVDS	I
LVREFL	N23	LVDS	I
LVDD_EN	H26	LVDS	O
PM_EXTTS#_0	J30	HVCMOS	I
PM_EXTTS#_1/ DPRSLPVR	K29	HVCMOS	I/O
PRDY#	E11	CPU_sideband	I/O
PREQ#	F15	CPU_sideband	I/O
PROCHOT#	C18	CPU_legacy	I/O

Table 7-48.Processor Ball List by Ball Name (Sheet 4 of 9)

Pin Name	Pin Number	Type	Dir.
DPSLP#	G10	CPU_sideband	I
DDR_A_MA_7	AJ12	MEM_Cntl_A	O
EXP_CLKINP	N6	3GIO_GFX_clk	I
EXP_ICOMPI	L9	3GIO_GFX_ana	I
EXP_RBIAS	L8	3GIO_GFX_ana	I/O
EXP_RCOMPO	L10	3GIO_GFX_ana	I
RSVD	R10	N/A	N/A
RSVD	R9	N/A	N/A
EXTBGREF	K7	CPU_legacy	I
FERR#	H6	CPU_sideband	O
GTLREF	A13	CPU_legacy	I
HPL_CLKINN	W8	Host PLL	I
HPL_CLKINP	W9	Host PLL	I
IGNNE#	E5	CPU_sideband	I/O
RSVD_TP	N11	N/A	N/A
RSVD_TP	P11	N/A	N/A
RSVD_TP	AA6	N/A	N/A
RSVD_TP	AA7	N/A	N/A
RSVD_TP	R6	N/A	N/A
RSVD_TP	R5	N/A	N/A
RSVD	H13	N/A	N/A
RSVD	D18	N/A	N/A
RSVD	L7	N/A	N/A
RSVD	D20	N/A	N/A
RSVD	L6	N/A	N/A
RSVD	E17	N/A	N/A
DDR3_DRAM_PWROK	AB4	CMOS-1.5	I
RSVD_TP	K9	N/A	N/A
RSVD_TP	D19	N/A	N/A
SMI#	E7	CPU_sideband	I/O
STPCLK#	F8	CPU_sideband	I
TCK	B14	CPU_legacy	I/O
TDI	D14	CPU_legacy	I/O
TDO	D13	CPU_legacy	I/O
RSVD	G5	N/A	N/A

Pin Name	Pin Number	Type	Dir.
PWROK	L5	HVCMOS	I
EXP_CLKINN	N7	3GIO_GFX_clk	I
RSVD_TP	AB11	N/A	N/A
RSVD_TP	AB13	N/A	N/A
DDR3_DRAMRST#	AK8	SSTL-1.5	O
RSVD_TP	AA21	N/A	N/A
RSVD_TP	W21	N/A	N/A
RSVD_TP	T21	N/A	N/A
RSVD_TP	V21	N/A	N/A
REFSSCLKINN	AA31	Clock	I
REFSSCLKINP	AA30	Clock	I
RSVD	L11	N/A	N/A
RSVD	N10	N/A	N/A
RSVD	N9	N/A	N/A
VCC	D24	PWR	
VCC	D26	PWR	
VCC	D28	PWR	
VCC	E22	PWR	
VCC	E24	PWR	
VCC	E27	PWR	
VCC	F21	PWR	
VCC	F22	PWR	
VCC	F25	PWR	
VCC	G19	PWR	
VCC	G21	PWR	
VCC	G24	PWR	
VCC	H17	PWR	
VCC	H19	PWR	
VCC	H22	PWR	
VCC	H24	PWR	
VCC	J17	PWR	
VCC	J19	PWR	
VCC	J21	PWR	
VCC	J22	PWR	
VCC	K15	PWR	

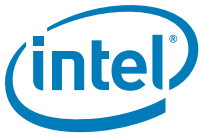


Table 7-48.Processor Ball List by Ball Name (Sheet 5 of 9)

Pin Name	Pin Number	Type	Dir.
THERMTRIP#	E13	CPU_sideband	O
THRMDA_1	D30	CPU_legacy	I
RSTIN#	AA3	HVCMOS	I
THRMDC_1	E30	CPU_legacy	O
THRMDC_2/ RSVD	D31	CPU_legacy	O
TMS	C14	CPU_legacy	I/O
TRST#	C16	CPU_legacy	I/O
VCC	A23	PWR	
VCC	A25	PWR	
VCC	A27	PWR	
VCC	B23	PWR	
VCC	B24	PWR	
VCC	B25	PWR	
VCC	B26	PWR	
VCC	B27	PWR	
VCC	C24	PWR	
VCC	C26	PWR	
VCC	D23	PWR	
VCCSM	AK13	PWR	
VCCSM	AK19	PWR	
VCCSM	AK9	PWR	
VCCSM	AL11	PWR	
VCCSM	AL16	PWR	
VCCSM	AL21	PWR	
VCCSM	AL25	PWR	
VCC_GIO	T31	PWR	
VCC_LGI	A21	PWR	
VCCA	Y2	PWR	
VCCA_DDR	U10	PWR	
VCCA_DDR	U5	PWR	
VCCA_DDR	U6	PWR	
VCCA_DDR	U7	PWR	
VCCA_DDR	U8	PWR	
VCCA_DDR	U9	PWR	

Pin Name	Pin Number	Type	Dir.
VCC	K17	PWR	
VCC	K21	PWR	
THRMDA_2/RSVD	C30	CPU_legacy	I
VCC	L19	PWR	
VCC	L21	PWR	
VCC	N14	PWR	
VCC	N16	PWR	
VCC	N19	PWR	
VCC	N21	PWR	
VCCP	B3	PWR	
VCCP	B4	PWR	
VCCP	E2	PWR	
VCCP	D4	PWR	
VCCRING_EAST	J31	PWR	
VCCRING_WEST	B2	PWR	
VCCRING_WEST	C2	PWR	
VCCRING_WEST	C3	PWR	
VCCGFX	W14	PWR	
VCCGFX	W16	PWR	
VCCGFX	W18	PWR	
VCCGFX	W19	PWR	
VCCSENSE	C29	PWR	
VCCSFR_AB_DPL	AC31	PWR	
VCCSFR_DMIHMP LL	AA1	PWR	
VID_0	H30	CPU_legacy	O
VID_1	H29	CPU_legacy	O
VID_2	H28	CPU_legacy	O
VID_3	G30	CPU_legacy	O
VID_4	G29	CPU_legacy	O
VID_5	F29	CPU_legacy	O
VID_6	E29	CPU_legacy	O
VSS	H27	VSS	
VSS	A11	VSS	

Table 7-48.Processor Ball List by Ball Name (Sheet 6 of 9)

Pin Name	Pin Number	Type	Dir.
VCCA_DDR	V2	PWR	
VCCA_DDR	V3	PWR	
VCCA_DDR	V4	PWR	
VCC	L14	PWR	
VCC	L16	PWR	
VCCA_DMI	T1	PWR	
VCCA_DMI	T2	PWR	
VCCA_DMI	T3	PWR	
VCCALVDS	V30	PWR	
VCCACK_DDR	AA10	PWR	
VCCACK_DDR	AA11	PWR	
VCCACRTDAC	T30	PWR	
RSVD	P2	N/A	N/A
VCCCK_DDR	AK7	PWR	
VCCCK_DDR	AL7	PWR	
VCCD_AB_DPL	AA19	PWR	
VCCD_HMPLL	V11	PWR	
VCCDLVDS	W31	PWR	
VCCGFX	T13	PWR	
VCCGFX	T14	PWR	
VCCGFX	T16	PWR	
VCCGFX	T18	PWR	
VCCGFX	T19	PWR	
VCCGFX	V13	PWR	
VCCGFX	V19	PWR	
VSS	AC21	VSS	
VSS	AC28	VSS	
VSS	AC30	VSS	
VSS	AD26	VSS	
VSS	AD5	VSS	
VSS	AE1	VSS	
VSS	AE11	VSS	
VSS	AE13	VSS	
VSS	AE15	VSS	
VSS	AE17	VSS	
VSS	AE22	VSS	

Pin Name	Pin Number	Type	Dir.
VSS	A16	VSS	
VSS	A19	VSS	
RSVD_NCTF	A29	VSS	
VCCA_DDR	W10	PWR	
VCCA_DDR	W11	PWR	
RSVD_NCTF	A4	VSS	
VSS	AA13	VSS	
VSS	AA14	VSS	
VSS	AA16	VSS	
VSS	AA18	VSS	
VSS	AA2	VSS	
VSS	AA22	VSS	
VSS	AA25	VSS	
VSS	AA26	VSS	
VSS	AA29	VSS	
VSS	AA8	VSS	
VSS	AB19	VSS	
VSS	AB21	VSS	
VSS	AB28	VSS	
VSS	AB29	VSS	
VSS	AB30	VSS	
VSS	AC10	VSS	
VSS	AC11	VSS	
VSS	AC19	VSS	
VSS	AC2	VSS	
VSS	AL9	VSS	
VSS	B13	VSS	
VSS	B16	VSS	
VSS	B19	VSS	
VSS	B22	VSS	
RSVD_NCTF	B30	VSS	
RSVD_NCTF	B31	VSS	
VSS	B5	VSS	
VSS	B9	VSS	
RSVD_NCTF	C1	VSS	
VSS	C12	VSS	

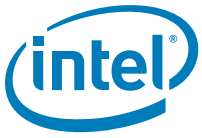


Table 7-48.Processor Ball List by Ball Name (Sheet 7 of 9)

Pin Name	Pin Number	Type	Dir.	Pin Name	Pin Number	Type	Dir.
VSS	AE31	VSS		VSS	C21	VSS	
VSS	AF11	VSS		VSS	C22	VSS	
VSS	AF17	VSS		VSS	C25	VSS	
VSS	AF21	VSS		RSVD_NCTF	C31	VSS	
RSVD_NCTF	A3	VSS		VSS	AF24	VSS	
RSVD_NCTF	A30	VSS		VSS	AF28	VSS	
VSS	AG10	VSS		VSS	E10	VSS	
VSS	AG3	VSS		VSS	E19	VSS	
VSS	AH18	VSS		VSS	E21	VSS	
VSS	AH23	VSS		VSS	E25	VSS	
VSS	AH28	VSS		VSS	E8	VSS	
VSS	AH4	VSS		VSS	F17	VSS	
VSS	AH6	VSS		VSS	F19	VSS	
VSS	AH8	VSS		VSS	F24	VSS	
RSVD_NCTF	AJ1	VSS		VSS	F28	VSS	
VSS	AJ16	VSS		VSS	F4	VSS	
VSS	AJ31	VSS		VSS	G15	VSS	
RSVD_NCTF	AK1	VSS		VSS	G17	VSS	
RSVD_NCTF	AK2	VSS		VSS	G22	VSS	
VSS	AK23	VSS		VSS	G27	VSS	
RSVD_NCTF	AK30	VSS		VSS	G31	VSS	
RSVD_NCTF	AK31	VSS		VSS	H11	VSS	
VSS	AL13	VSS		VSS	H15	VSS	
VSS	AL19	VSS		VSS	H2	VSS	
RSVD_NCTF	AL2	VSS		VSS	H21	VSS	
VSS	AL23	VSS		VSS	H25	VSS	
RSVD_NCTF	AL29	VSS		VSS	H8	VSS	
RSVD_NCTF	AL3	VSS		VSS	J11	VSS	
RSVD_NCTF	AL30	VSS		VSS	J13	VSS	
VSS	J15	VSS		VSS	T11	VSS	
VSS	J4	VSS		VSS	U22	VSS	
VSS	K11	VSS		VSS	U23	VSS	
VSS	K13	VSS		VSS	U24	VSS	
VSS	K19	VSS		VSS	U27	VSS	
VSS	K26	VSS		VSS	V14	VSS	
VSS	K27	VSS		VSS	V28	VSS	

Table 7-48.Processor Ball List by Ball Name (Sheet 8 of 9)

Pin Name	Pin Number	Type	Dir.	Pin Name	Pin Number	Type	Dir.
VSS	K28	VSS		VSS	V29	VSS	
VSS	K30	VSS		VSS	W13	VSS	
VSS	K4	VSS		VSS	W2	VSS	
VSS	K8	VSS		VSS	L13	VSS	
VSS	L1	VSS		VSS	L18	VSS	
VSS	D22	VSS		VSS	W23	VSS	
RSVD_NCTF	E1	VSS		VSS	W25	VSS	
VSS	L22	VSS		VSS	W26	VSS	
VSS	L24	VSS		VSS	W28	VSS	
VSS	L25	VSS		VSS	W30	VSS	
VSS	L29	VSS		VSS	W4	VSS	
VSS	M28	VSS		VSS	W5	VSS	
VSS	M3	VSS		VSS	W6	VSS	
VSS	N1	VSS		VSS	W7	VSS	
VSS	N13	VSS		VSS	Y28	VSS	
VSS	N18	VSS		VSS	Y3	VSS	
VSS	N24	VSS		VSS	Y4	VSS	
VSS	N25	VSS		VSS	T29	VSS	
VSS	N28	VSS		VSSSENSE	B29	PWR	
VSS	N4	VSS		XDP_RSVD[0]	D12	XDP	
VSS	N5	VSS		XDP_RSVD[1]	A7	XDP	
VSS	N8	VSS		XDP_RSVD[2]	D6	XDP	
VSS	P13	VSS		XDP_RSVD[3]	C5	XDP	
VSS	P14	VSS		XDP_RSVD[4]	C7	XDP	
VSS	P16	VSS		XDP_RSVD[5]	C6	XDP	
VSS	P18	VSS		XDP_RSVD[6]	D8	XDP	
VSS	P19	VSS		XDP_RSVD[7]	B7	XDP	
VSS	P21	VSS		XDP_RSVD[8]	A9	XDP	
VSS	P3	VSS		XDP_RSVD[9]	D9	XDP	
VSS	P4	VSS		XDP_RSVD[10]	C8	XDP	
VSS	R25	VSS		XDP_RSVD[11]	B8	XDP	
VSS	R7	VSS		XDP_RSVD[12]	C10	XDP	
VSS	R8	VSS		XDP_RSVD[13]	D10	XDP	
VSS	V16	VSS		XDP_RSVD[14]	B11	XDP	
VSS	V18	VSS		XDP_RSVD[15]	B10	XDP	

Table 7-48.Processor Ball List by Ball Name (Sheet 9 of 9)

Pin Name	Pin Number	Type	Dir.
XDP_RSVD[16]	B12	XDP	
XDP_RSVD[17]	C11	XDP	

Pin Name	Pin Number	Type	Dir.

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Intel:

AU80610006237AAS LBX9 AU80610004653AAS LBMG