AWT921

900 MHz Integrated Power Amp

Data Sheet - Rev 2.0

FEATURES

- High Power Levels
- High Efficiency
- True Surface Mount Package With Integrated Heat Slug
- Internal Bias Circuit Requiring Nominal Input Voltages ±10%
- Low Cost
- Off Chip Output Matching Circuit Allows Application Optimization

APPLICATIONS

- Base Station Driver Amplifier
- u-Cell Base Station Output Stage
- Cellular Booster Amplifier

S11
SSOP-28
28 Pin Wide Body w/ Heat Slug

PRODUCT DESCRIPTION

The AWT921 is a monolithic amplifier for use in communication systems that require high gain and output intercept point. This device has been specifically designed for multi-carrier and micro-cell base station applications. This device is manufactured on a high power MESFET process and has an on-chip bias circuit that does not require highly regulated positive and negative supplies to establish the proper operating point.

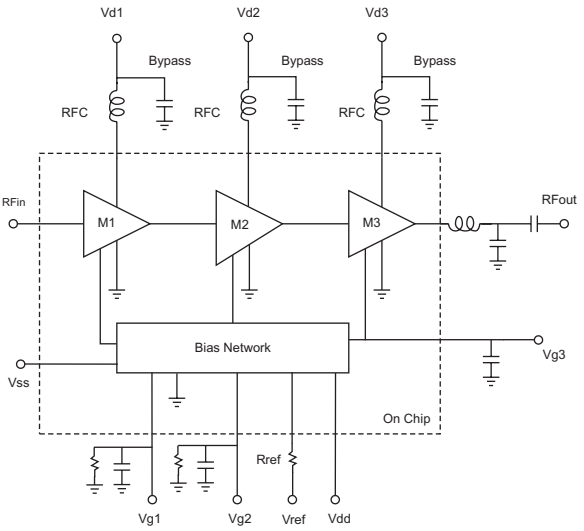


Figure 1: Block Diagram

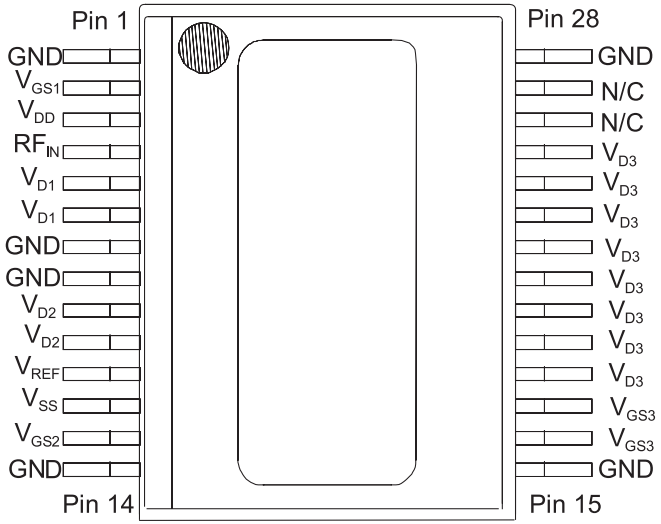


Figure 2: Pinout (X-Ray Top View)

Table 1: Pin Description

PIN	NAME	DESCRIPTION
1,14,15 28, slug	GND	AC and RF Ground
2	V_{GS1}	First Stage Gate Terminal
3	V_{DD}	Positive Supply of Bias Circuit
4	RF_{IN}	RF Input
5,6	V_{D1}	First Stage Drain Supply
7,8	GND	First Stage Source Ground
9,10	V_{D2}	Second Stage Drain Supply
11	V_{REF}	Bias Control Pin
12	V_{SS}	Negative Supply for Bias Circuit
13	V_{GS2}	Second Stage Gate Terminal
16,17	V_{GS3}	Third Stage Gate Terminal
18-25	V_{D3}	Third stage Drain Supply & RF_{OUT}
26,27	N/C	Not Connected

ELECTRICAL CHARACTERISTICS

Table 2: Absolute Minimum and Maximum Ratings

PARAMETER	MIN	MAX	UNIT
V_{DD}	0	+7	V_{DC}
RF_{IN}	0	+20	dBm
1st Stage Supply (V_{D1})	0	+10	V_{DC}
2nd Stage Supply (V_{D2})	0	+10	V_{DC}
3rd Stage Voltage (V_{D3})	0	+10	V_{DC}
Negative Supply (V_{SS})	-7	0	V_{DC}
Reference Voltage (V_{REF})	0	+7	V_{DC}
Storage Temperature	-55	+100	°C
Operating Temperature	-30	+85	°C

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.

Table 3: Operating Ranges

PARAMETER	MIN	TYP	MAX	UNIT
Operating Frequency	925	-	960	MHz
RF_{IN}	0	-	+14	dBm
1st Stage Supply (V_{D1})	0	+8.5	+9	V_{DC}
2nd Stage Supply (V_{D2})	0	+8.5	+9	V_{DC}
3rd Stage Voltage (V_{D3})	0	+8.5	+9	V_{DC}
Reference Voltage (V_{REF})	0	+5	+7	V_{DC}
Negative Supply (V_{SS})	-7	-3	-2.7	V_{DC}
Operating Temperature	-30	-	+85	°C

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

Table 4: Electrical Specifications [1]
(Pin = +12dBm, fo = 925-960 MHz, Vds1=Vds2=Vds3=8.5V, V_{SS} = -5 V, V_{REF} = +25 V, V_{DD} = +5 V, T_C = +25 °C, 50 Ω system[2])

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Frequency	fo	925	-	960	MHz
Power Output	P_{OUT}	-	+39	-	dBm
Power Added Efficiency	η_{EFF}	-	40	-	%
Gain @P_{OUT} = +39 dBm @P_{OUT} = +30 dBm	PG	- -	27 31	- -	dB
Harmonics [3] 2nd 3rd 4th		- - -	37 47 50	- - -	dBc
Stability: -60 dBc all spurious outputs relative to desired signal	-	-	3:1	-	VSWR load, all phase angles
Bias Supply Currents	I_{SS} I_{REF} I_{DD}	- - -	8 1.2 8	- - -	mA
Quiescent Currents	I_{DQ1} I_{DQ2} I_{DQ3}	- - -	100 250 200	- - -	mA
Input Return Loss	-	10	-	-	dB
Gain Flatness @ P_{OUT} = +39dBm @ P_{OUT} = +30 dBm	ΔPG	0.5 0.5	- -	- -	dB
Thermal Resistance [4]		-	4.5	-	C/W

Notes:
(1) As measured in ANADIGICS test fixture, see application section.
(2) 50 Ω Measurement system after off chip matching circuit, input terminated in 50 Ω.
(3) Measured at P_{OUT} =+ 39 dBm.
(4) Thermal resistance for junction to bottom of slug. $\Theta jc = (Tj-Tc)/((I_{D1}+I_{D2}+I_{D3})*V_{SUP} - P_{OUT})$

PERFORMANCE DATA

Figure 3: Output Power and Power Added Efficiency vs. Pin

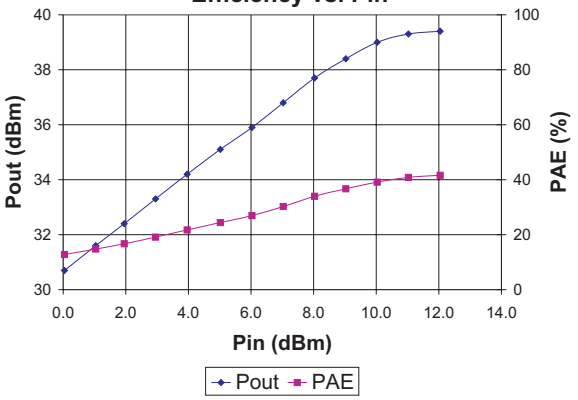


Figure 4: Output Power and Power Added Efficiency vs. Frequency

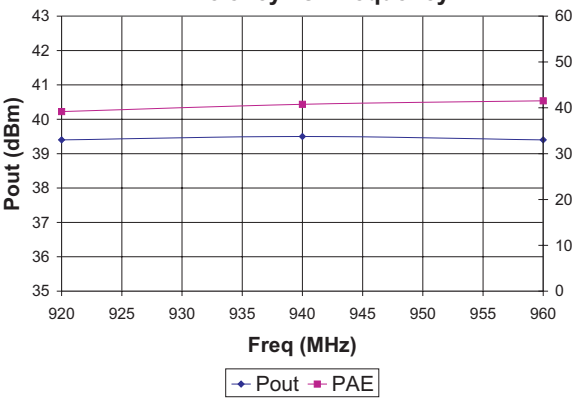


Figure 5: Output Power and PAE vs. Supply Voltage

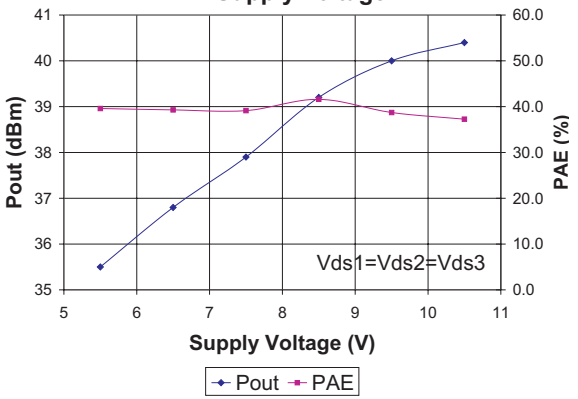


Figure 6: Third Stage Quiescent Current vs. Reference Voltage with Various R_{REF}

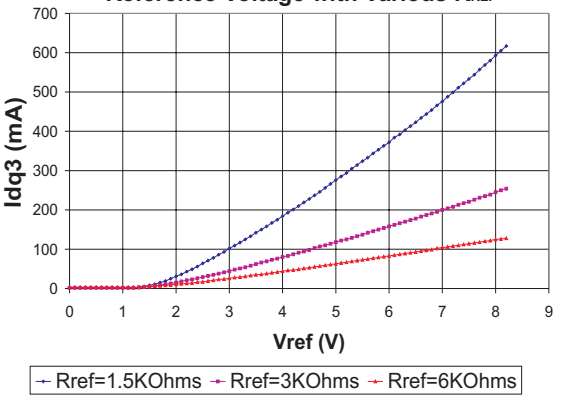


Figure 7: Third Stage Quiescent Current vs. V_{DD}, R_{REF} = 1.8 KΩ

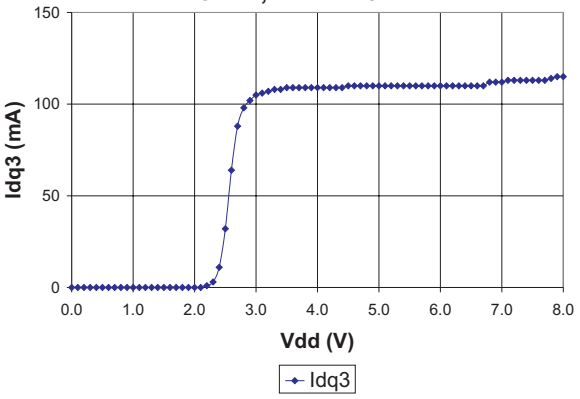


Figure 8: Third Stage Quiescent Current vs. V_{SS}, R_{REF} = 1.8 KΩ

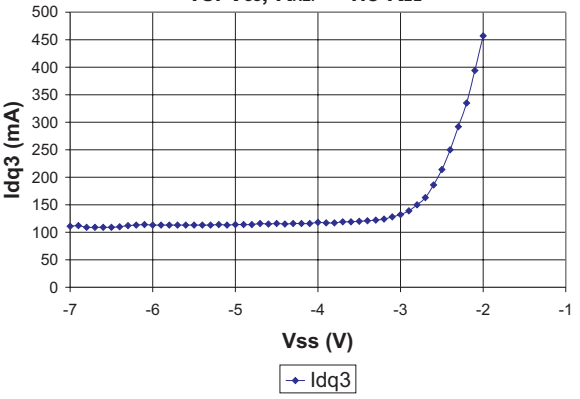


Figure 9: Small Signal Gain, Saturated Power, and Efficiency vs. Temperature

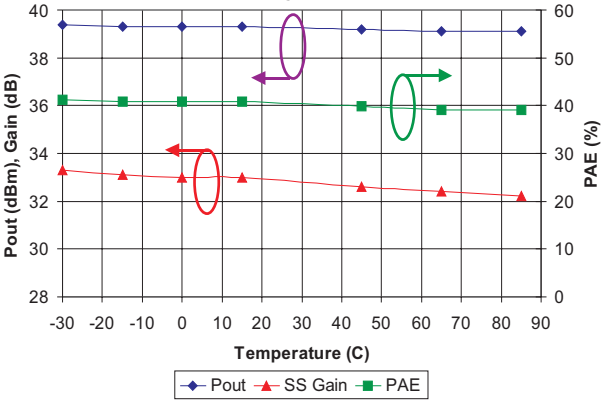


Figure 10: Third Stage Quiescent Current, Reference Current vs. Temperature

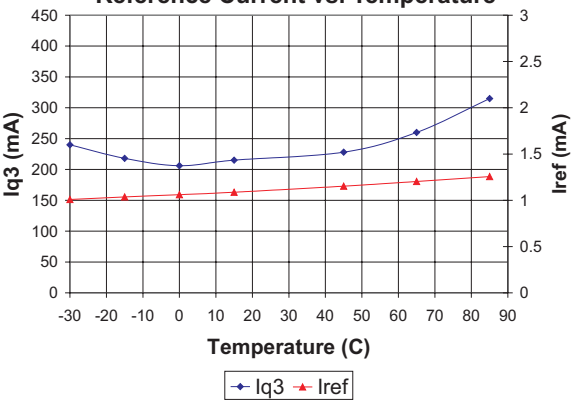


Figure 11: Test Circuit Impedance Presented to the First Stage Drain (Vd1)

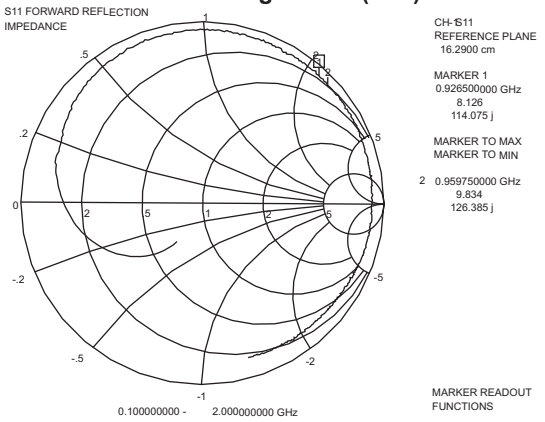


Figure 12: Test Circuit Impedance Presented to the Second Stage Drain (Vd2)

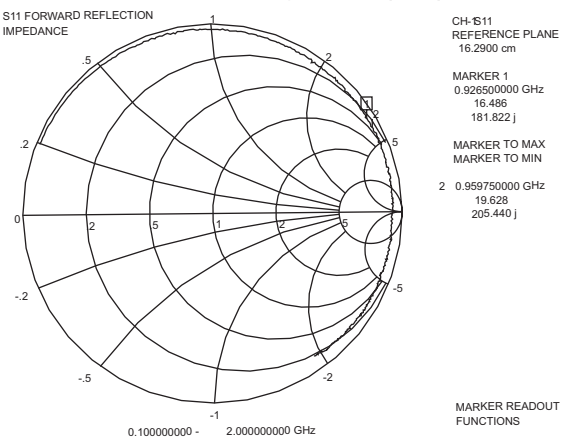
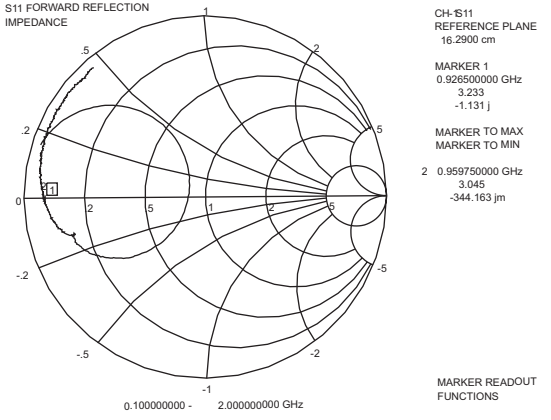


Figure 13: Test Circuit Impedance Presented to the Third Stage Drain (Vd3)



APPLICATION INFORMATION

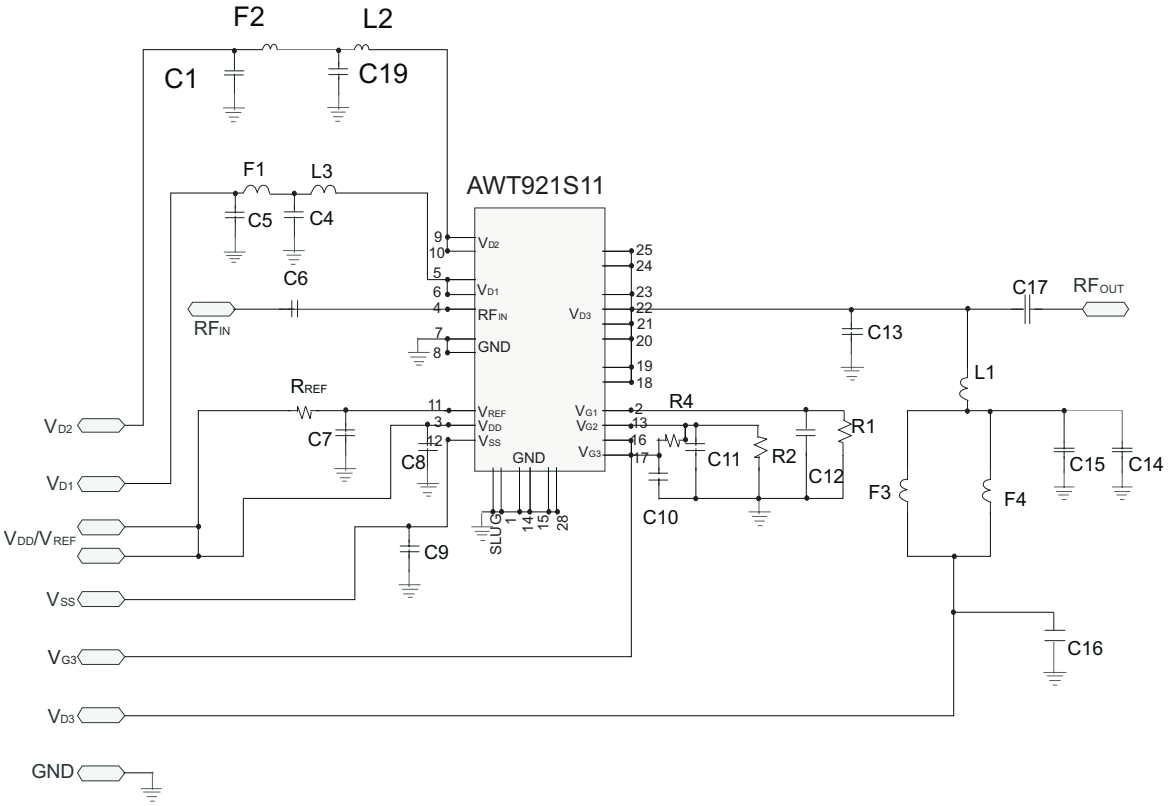
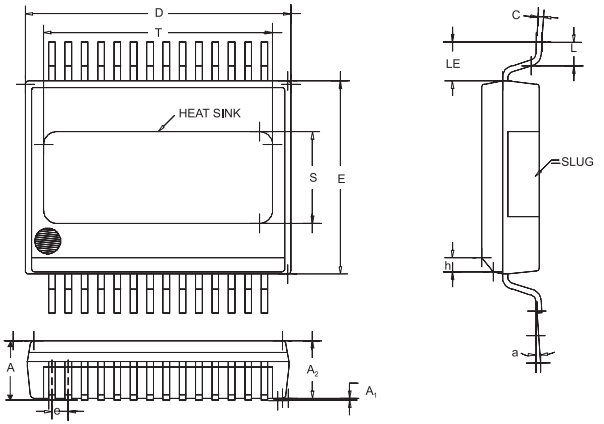


Figure 14: Application Circuit Schematic

Table 5: Application Circuit Component Values (925-960 MHz GSM Application)

DESIGNATION	VALUE	DESIGNATION	VALUE
R1	7500 Ω	C10, C11	2700 pF
R2	2.2 KΩ	C13	11 pF
R_{REF}	1.8 KΩ	C14	4700 pF
C1, C5, C16	2.2 µF	L1	8 nH Colicraft, A03T
C4, C15, C19	33 pF	L2	12 nH
C6, C17	47 pF	L3	6 nH
C7, C8, C9, C12	0.01 µF	F1, F2, F3, F4,	Ferrite 47 Ω @ 100 MHz, 1A Rating Taiyo Yuden, BK2125HS470

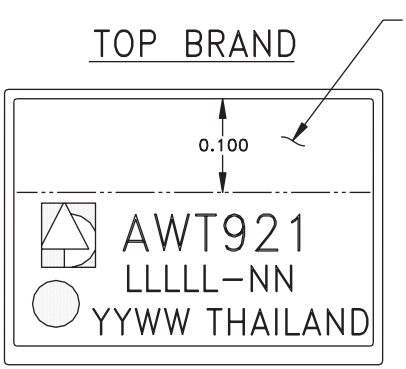
PACKAGE OUTLINE



	INCHES		MILLIMETERS		
SYMBOL	MIN.	MAX.	MIN.	MAX.	NOTE
A	0.087	0.093	2.21	2.36	
A_1	0.000	0.004	0.00	0.10	
A_2	0.087	0.089	2.21	2.25	
B	0.008	0.012	0.36	0.46	
C	0.007	0.009	0.18	0.25	
D	0.400	0.408	10.16	10.36	2
E	0.292	0.296	7.42	7.52	2
e	0.025	BSC	0.64	BSC	4
H	0.410	0.418	10.41	40.62	
h	0.018	0.024	0.48	0.61	
L	0.034	0.038	0.86	0.97	
LE	0.84		1.37		
a	0	8	0	8	
S	0.139	0.141	3.54	3.55	5
T	0.349	0.351	8.86	8.92	5

NOTES:
1. CONTROLLING DIMENSIONS : INCHES
2. DIMENSION "D" DOES NOT INCLUDEMOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, ROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006 (0.16mm)
3. DIMENSION "E" DOES NOT INCLUDE INTER-LEAD OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.010 (0.25mm) PER SIDE.
4. MAXIMUM LEAD TWIST/SKEW TO BE 0.002 (0.05mm)
5. MOLD FLASH SHALL NOT EXTEND MORE THAN 0.010 (0.25mm) ON ANY EDGE OF HEAT SLUG

Figure 15: S11 Package Outline - 28 Pin SSOP 28 Thermal Slug Package



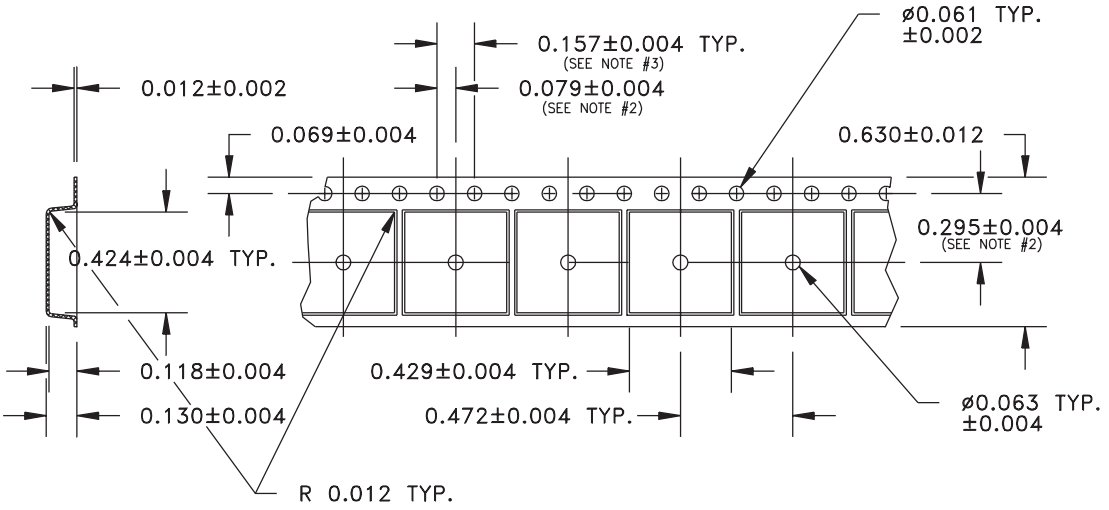
AREA MUST BE FREE OF MARKING

NOTES:

1. ANADIGICS LOGO SIZE: X=0.058±0.010 Y=0.069±0.010
2. PART NUMBER
3. WAFER LOT NUMBER: LLLLL–NN –where– LLLLL= FIVE NUMERIC CHARACTERS
   – DASH IS OPTIONAL
   NN= TWO ALPHABETIC CHARACTERS
4. PIN 1 INDICATOR: MOLD NOTCH –or– INK DOT
5. YEAR AND WORK WEEK: YYWW –where– YY = YEAR, LAST TWO DIGITS
   WW = WORK WEEK
6. COUNTRY CODE: THAILAND
7. TYPE : ELITE
   SIZE : PART # = 3 POINT
   WAFER # & DATE CODE = 2 POINT
   COLOR : WHITE or SILVER

Figure 16: Branding Specification

COMPONENT PACKAGING



NOTES: 1. MATERIAL – CONDUCTIVE POLYSTYRENE.
2. MEASURED FROM CENTERLINE OF SPROCKET HOLE TO CENTERLINE OF POCKET.
3. CUMULATIVE TOLERANCE OF 10 SPROCKET HOLES IS ± 0.008.

ALL DIMENSIONS ARE IN INCHES

ALL DIMENSIONS ARE REFERENCE ONLY.
SEMIPAC CORP PART #
CPSO16WA3–22B3–65

CARRIER TAPE, CONDUCTIVE
SOIC 16 LD WIDE BODY PACKAGE
DWG. NO.
4475

Figure 17: Tape & Reel Drawing

Table 6: Tape & Reel Dimensions

PACKAGE TYPE	TAPE WIDTH	POCKET PITCH	REEL CAPACITY	MAX REEL DIA
SSOP-28 WIDE BODY	0.630 INCHES	0.472 INCHES	3500	13 INCHES

NOTES

NOTES

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