ARIZONA MICROTEK, INC.

AZ100LVE310

ECL/PECL 2:8 Differential Clock Driver

FEATURES

- Operating Range of 3.0V to 5.5V
- Low Skew
- Guaranteed Skew Spec
- Differential Design
- V_{BB} Output
- 75kΩ Internal Input Pulldown Resistors
- Direct Replacement for ON Semiconductor MC100LVE310 & MC100E310

PACKAGE AVAILABILITY

PACKAGE	PART NUMBER	MARKING	NOTES
PLCC 28	AZ100LVE310FN	AZM100LVE310 <Date Code>	1,2

1 Add R2 at end of part number for 13 inch (2.5K parts) Tape & Reel.
2 Date code format: "YY" for year followed by "WW" for week.

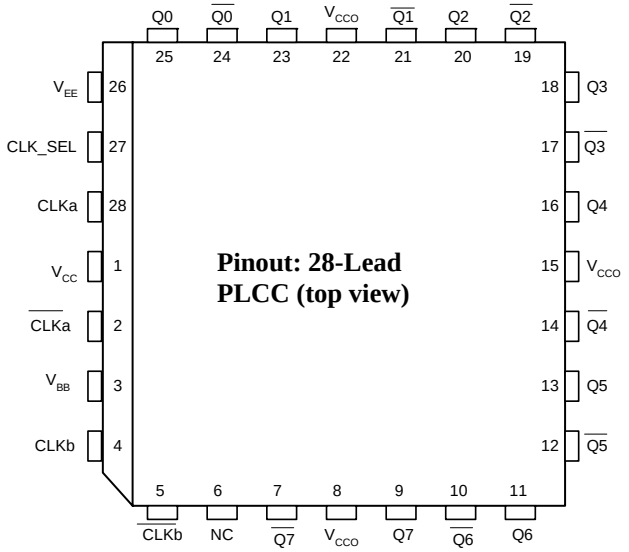
DESCRIPTION

The AZ100LVE310 is a low skew 2:8 fanout buffer designed with clock distribution in mind. The device features fully differential clock paths to minimize both device and system skew. The AZ100LVE310 offers two selectable clock inputs allowing redundant or test clocks to be incorporated into the system clock trees.

The AZ100LVE310 provides a V_{BB} output for single-ended use or a DC bias reference for AC coupling to the device. For single–ended input applications, the V_{BB} reference should be connected to one side of the CLKa/CLKb differential input pair. The input signal is then fed to the other CLKa/CLKb input. The V_{BB} pin should be used only as a bias for the AZ100LVE310 as its current sink/source capability is limited. When used, the V_{BB} pin should be bypassed to ground via a 0.01μF capacitor.

Both sides of the differential output must be terminated into 50Ω to ensure that the tight skew specification is met, even if only one side is used. In most applications all eight differential pairs will be used and therefore terminated. In the case where fewer than eight pairs are used, all output pairs on the same package side (sharing the same V_{CCO}) as the pairs being used should be terminated to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10–20ps) of the outputs being used; while not being catastrophic to most designs this will result in an increase in skew.

NOTE: Specifications in the ECL/PECL tables are valid when thermal equilibrium is established.



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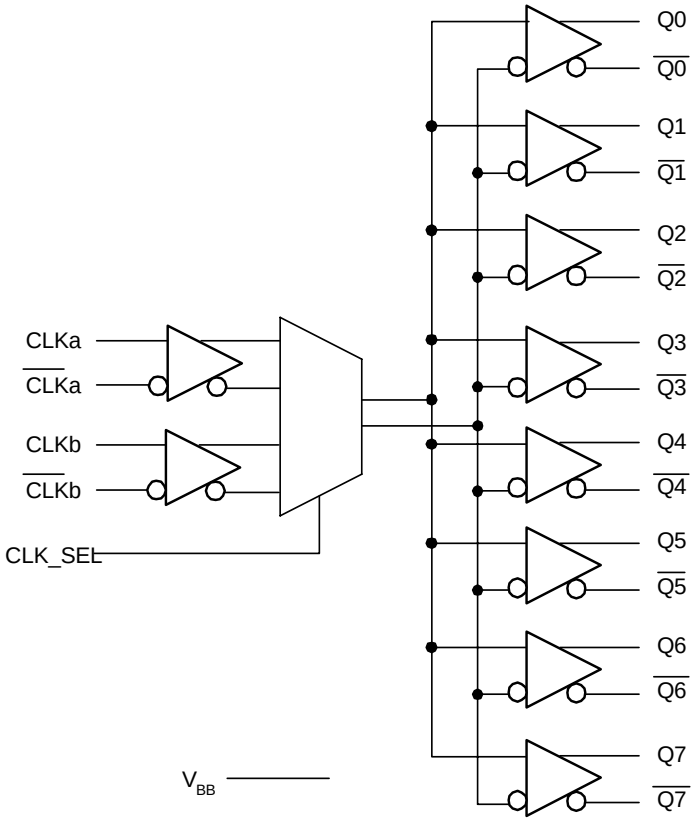
LOGIC SYMBOL



PIN DESCRIPTION

PIN	FUNCTION
CLKa, $\overline{CLKa}$	Differential Input Pairs
CLKb, $\overline{CLKb}$	Differential Input Pairs
CLK_SEL	Input Clock Select
Q0, $\overline{Q0}$ – Q7, $\overline{Q7}$	Differential Output Pairs
V_{BB}	V_{BB} Output
V_{CC} , V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

CLK_SEL	Input Clock
0	CLKa Selected
1	CLKb Selected

Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Rating	Unit
V_{CC}	PECL Power Supply (V_{EE} = 0V)	0 to +8.0	Vdc
V_I	PECL Input Voltage (V_{EE} = 0V)	0 to +6.0	Vdc
V_{EE}	ECL Power Supply (V_{CC} = 0V)	-8.0 to 0	Vdc
V_I	ECL Input Voltage (V_{CC} = 0V)	-6.0 to 0	Vdc
I_{OUT}	Output Current --- Continuous --- Surge	50 100	mA
T_A	Operating Temperature Range	-40 to +85	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C

100K ECL DC Characteristics (V_{EE} = -3.0V to -5.5V, V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage[1]	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	-1025	-955	-880	mV
V_{OL}	Output LOW Voltage[1]	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	-1810	-1705	-1620	mV
V_{IH}	Input HIGH Voltage	-1165		-880	-1165		-880	-1165		-880	-1165		-880	mV
V_{IL}	Input LOW Voltage	-1810		-1475	-1810		-1475	-1810		-1475	-1810		-1475	mV
V_{BB}	Reference Voltage	-1380		-1260	-1380		-1260	-1380		-1260	-1380		-1260	mV
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{IL}	Input LOW Current	0.5			0.5			0.5			0.5			µA
I_{EE}	Power Supply Current		55	60		55	60		55	60		65	70	mA

1. Each output is terminated through a 50Ω resistor to V_{CC} – 2V.

100K LVPECL DC Characteristics (V_{EE} = GND, V_{CC} = V_{CCO} = +3.3V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage[1,2]	2215	2295	2420	2275	2345	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage[1,2]	1470	1605	1745	1490	1595	1680	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage[1]	2135		2420	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage[1]	1490		1825	1490		1825	1490		1825	1490		1825	mV
V_{BB}	Reference Voltage[1]	1920		2040	1920		2040	1920		2040	1920		2040	mV
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{IL}	Input LOW Current	0.5			0.5			0.5			0.5			µA
I_{EE}	Power Supply Current		55	60		55	60		55	60		65	70	mA

1. For supply voltages other that 3.3V, use the ECL table values and ADD supply voltage value.
2. Each output is terminated through a 50Ω resistor to V_{CC} – 2V.

100K PECL DC Characteristics (V_{EE} = GND, V_{CC} = V_{CCO} = +5.0V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage[1,2]	3915	3995	4120	3975	4045	4120	3975	4045	4120	3975	4045	4120	mV
V_{OL}	Output LOW Voltage[1,2]	3170	3305	3445	3190	3295	3380	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage[1]	3835		4120	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage[1]	3190		3525	3190		3525	3190		3525	3190		3525	mV
V_{BB}	Reference Voltage[1]	3620		3740	3620		3740	3620		3740	3620		3740	mV
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{IL}	Input LOW Current	0.5			0.5			0.5			0.5			µA
I_{EE}	Power Supply Current		55	60		55	60		55	60		65	70	mA

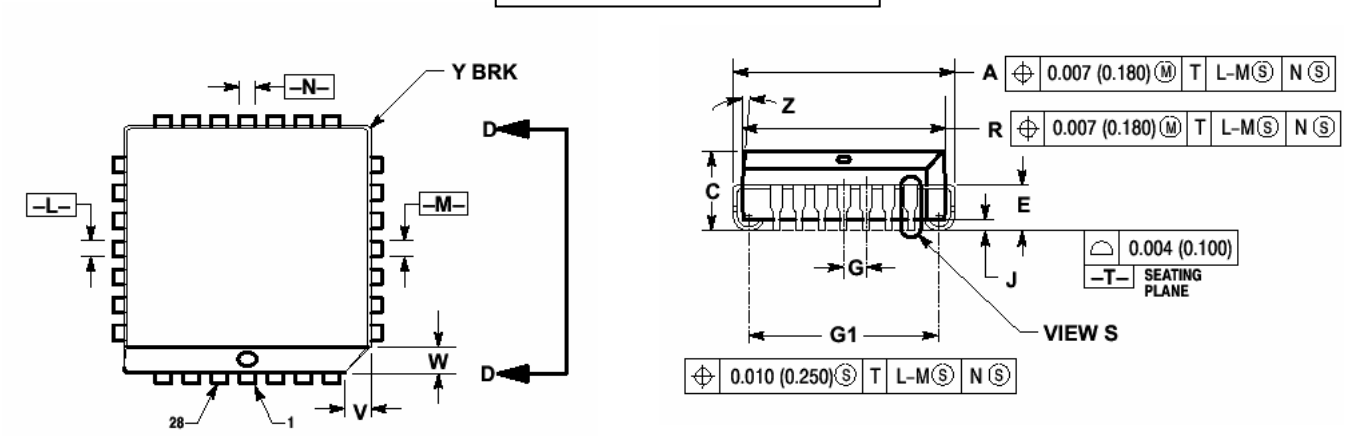
1. For supply voltages other that 5.0V, use the ECL table values and ADD supply voltage value.
2. Each output is terminated through a 50Ω resistor to V_{CC} – 2V.

AC Characteristics (V_{EE} = -3.0V to -5.5V, V_{CC} = V_{CCO} = GND or V_{EE} = GND, V_{CC} = V_{CCO} = +3.0 to +5.5V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH} / t_{PHL}	Propagation Delay to Output IN (Diff)[1] IN (SE)[2]	525 500		725 750	550 550		750 775	550 550		750 800	575 600		775 850	ps
t_{SKEW}	Within-Device Skew Part-to-Part Skew (Diff)[3]			75 250			75 250			50 200			50 200	ps
V_{PP} (AC)	Minimum Input Swing[4]	250			250			250			250			mV
V_{CMR}	Common Mode Range[5]	V_{EE} + 1.8		V_{CC} - 0.4	V_{EE} + 1.8		V_{CC} - 0.4	V_{EE} + 1.8		V_{CC} - 0.4	V_{EE} + 1.8		V_{CC} - 0.4	V
t_r / t_f	Rise/Fall Time 20 – 80%	250	450	650	275	375	600	275	375	600	275	375	600	ps

1. The differential propagation delay is defined as the delay from the crossing point of the differential input signals to the crossing point of the differential output signals.
2. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
3. The within-device skew is defined as the worst-case difference between any two similar delay paths within a single device.
4. V_{PP} is the minimum peak-to-peak differential input swing for which AC parameters are guaranteed. The V_{PP}(min) is AC limited for the LVE310, because differential input as low as 50 mV will still produce full ECL levels at the output.
5. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak-to-peak voltage is less than 1.0V and greater than or equal to V_{PP}(min).

PACKAGE DIAGRAM
PLCC 28



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.32	12.57	0.485	0.495
B	12.32	12.57	0.485	0.495
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51		0.020	
K	0.64		0.025	
R	11.43	11.58	0.450	0.456
U	11.43	11.58	0.450	0.456
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
T		0.50		0.020
Z	2^O	10^O	2^O	10^O
G1	10.42	10.92	0.410	0.430
K1	1.02		0.040	

NOTES:
1. DATUMS –L-, -M-, AND –N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T-, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALOWABLE MOLD FLASH IS 0.010mm (0.250in.) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKGE BOTTOM BY UP TO 0.012mm (0.300in.). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, THE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025mm (0.635in.).