

AZ10ELT22

AZ100ELT22

CMOS/TTL to Differential PECL Translator

FEATURES

- Green / RoHS Compliant / Lead (Pb) Free package available
- 0.5ns Typical Propagation Delay
- <100ps Typical Output to Output Skew
- Differential PECL Outputs
- Flow Through Pinouts
- Operating Range of 3.0V to 5.5V
- Direct Replacement for ON Semiconductor MC10ELT22 & MC100ELT22
- IBIS Model Files Available on Arizona Microtek Website

PACKAGE AVAILABILITY

PACKAGE	PART NUMBER	MARKING	NOTES
SOIC 8	AZ10ELT22D	AZM10 ELT22	1,2,4
SOIC 8 RoHS Compliant / Lead (Pb) Free	AZ10ELT22D+	AZM10+ ELT22	1,2,4
SOIC 8	AZ100ELT22D	AZM100 ELT22	1,2,4
SOIC 8 RoHS Compliant / Lead (Pb) Free	AZ100ELT22D+	AZM100+ ELT22	1,2,4
TSSOP 8	AZ10ELT22T	AZT LT22	1,2,4
TSSOP 8 RoHS Compliant / Lead (Pb) Free	AZ10ELT22T+	AZT+ LT22	1,2,4
TSSOP 8	AZ100ELT22T	AZH LT22	1,2,4
TSSOP 8 RoHS Compliant / Lead (Pb) Free	AZ100ELT22T+	AZH+ LT22	1,2,4

DESCRIPTION

The AZ10/100ELT22 is a dual CMOS/TTL to differential PECL translator. Because PECL (Positive ECL) levels are used, only V_{CC} and ground are required. The small outline packaging and the low skew, dual gate design of the ELT22 makes it ideal for applications that require the translation of a clock and a data signal.

The ELT22 is available in both PECL standards: the 10ELT is compatible with PECL 10K logic levels while the 100ELT is compatible with PECL 100K logic levels.

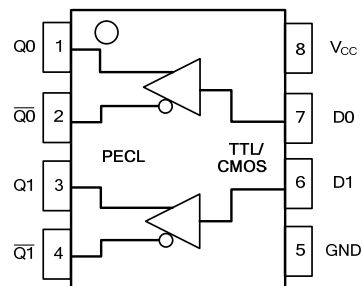
NOTE: Specifications in PECL tables are valid when thermal equilibrium is established.

- 1 Add R1 at end of part number for 7 inch (1K parts), R2 for 13 inch (2.5K parts) Tape & Reel.
- 2 Date code format: "Y" or "YY" for year followed by "WW" for week.
- 3 Parts marked JNB for date codes prior to 4WW (prior to 2004).
- 4 Date code "YWW" or "YYWW" on underside of part.

PIN DESCRIPTION

PIN	FUNCTION
Q0, Q0, Q1, Q1	Differential PECL Outputs
D0, D1	CMOS/TTL Input
V_{CC}	Positive Supply
GND	Ground

LOGIC DIAGRAM AND PINOUT



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Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	8.0	V
V _{IN}	Input Voltage	0 to 6.0	V
I _{OUT}	Current Applied to Output in Low Output State ---Continuous ---Surge	50 100	mA
T _A	Operating Temperature Range (In Free-Air)	-40 to +85	°C
T _{STG}	Storage Temperature Range	-65 to +150	°C

TTL/CMOS INPUT DC CHARACTERISTICS (GND = 0.0V, V_{CC} = +3.0V to +5.5V)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I _{IH}	Input HIGH Current			15	μA	V _{IN} = 2.7V
I _{IH}	Input HIGH Current			20	μA	V _{IN} = V _{CC}
I _{IL}	Input LOW Current			-0.1	mA	V _{IN} = 0.5V
V _{IK}	Input Clamp Diode Voltage			-1.2	V	I _{IN} = -18mA
V _{IH}	Input HIGH Voltage	2.0			V	
V _{IL}	Input LOW Voltage			0.8	V	

10K LVPECL DC Characteristics GND = 0.0V, V_{CC} = +3.3V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V _{OH}	Output HIGH Voltage ^{1,2}	2170		2410	2245		2460	2295	2400	2490	2390		2580	mV
V _{OL}	Output LOW Voltage ^{1,2}	1350		1685	1350		1670	1350	1550	1670	1350		1705	mV
I _{CC}	Power Supply Current ³			24			24			24			25	mA

1. Output parameters vary 1:1 with V_{CC}.
2. Each output is terminated through a 50Ω resistor to V_{CC} - 2V.
3. I_{CC} is measured with outputs open.

10K PECL DC Characteristics (GND = 0.0V, V_{CC} = +5.0V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V _{OH}	Output HIGH Voltage ^{1,2}	3870		4110	3945		4160	3995	4100	4190	4090		4280	mV
V _{OL}	Output LOW Voltage ^{1,2}	3050		3385	3050		3370	3050	3250	3370	3050		3405	mV
I _{CC}	Power Supply Current ³			24			24			24			25	mA

1. Output parameters vary 1:1 with V_{CC}.
2. Each output is terminated through a 50Ω resistor to V_{CC} - 2V.
3. I_{CC} is measured with outputs open.

100K LVPECL DC Characteristics (GND = 0.0V, V_{CC} = +3.3V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V _{OH}	Output HIGH Voltage ^{1,2}	2160		2420	2205		2420	2235	2345	2420	2255		2420	mV
V _{OL}	Output LOW Voltage ^{1,2}	1470		1745	1490		1680	1490	1595	1680	1490		1680	mV
I _{CC}	Power Supply Current ³			24			24			24			25	mA

1. Output parameters vary 1:1 with V_{CC}.
2. Each output is terminated through a 50Ω resistor to V_{CC} - 2V.
3. I_{CC} is measured with outputs open.

100K PECL DC Characteristics (GND = 0.0V, V_{CC} = +5.0V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V _{OH}	Output HIGH Voltage ^{1,2}	3860		4120	3905		4120	3935	4045	4120	3955		4120	mV
V _{OL}	Output LOW Voltage ^{1,2}	3170		3445	3190		3380	3190	3295	3380	3190		3380	mV
I _{CC}	Power Supply Current ³			24			24			24			25	mA

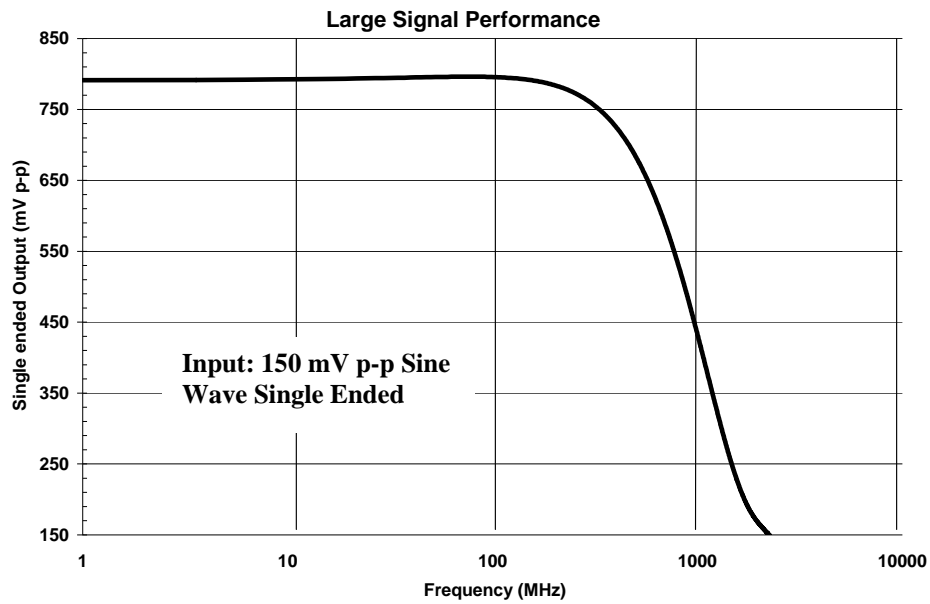
1. Output parameters vary 1:1 with V_{CC}.
2. Each output is terminated through a 50Ω resistor to V_{CC} - 2V.
3. I_{CC} is measured with outputs open.

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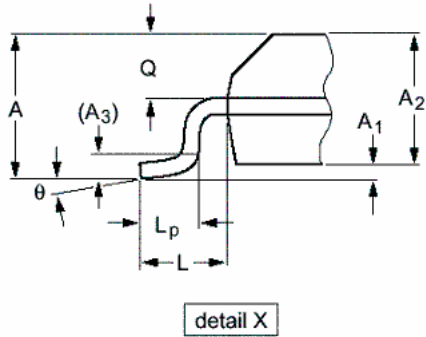
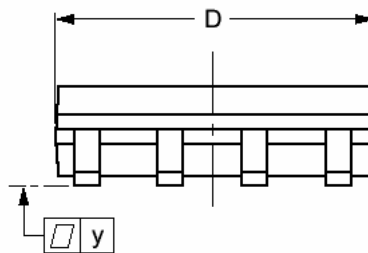
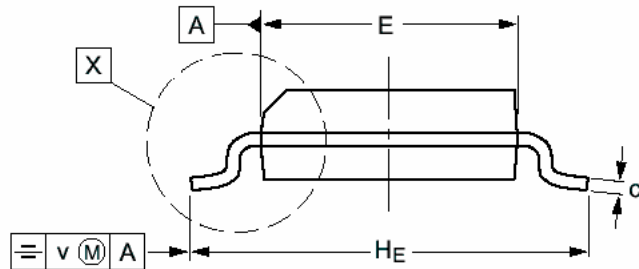
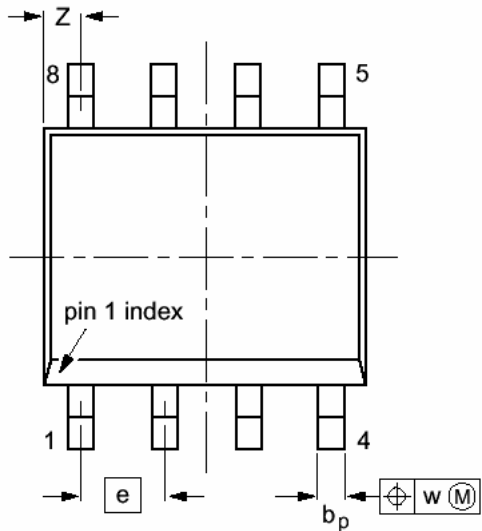
AC Characteristics (GND = 0.0V, V_{CC} = +3.0V to +5.5V)

Symbol	Characteristic	-40°C		0°C		25°C			85°C		Unit	Condition
		Min	Max	Min	Max	Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay ¹	0.2	0.7	0.2	0.7	0.2	0.4	0.7	0.2	0.7	ns	
t _{PHL}	Propagation Delay ¹	0.2	0.7	0.2	0.7	0.2	0.4	0.7	0.2	0.7	ns	
t _r /t _f	Output Rise/Fall Time	0.25	0.7	0.25	0.7	0.25		0.7	0.25	0.7	ns	20-80%
f _{MAX}	Maximum Frequency ²	350		350		350			350		MHz	
f _{MAX}	Maximum Frequency ³	670		800		800			800		MHz	

1. Propagation delay is measured from +1.5V on the input to 50% of the PECL output swing. Input rise/fall times are < 1ns/V.
2. Full swing PECL output.
3. Output at -3 dB.



**PACKAGE DIAGRAM
SOIC 8**



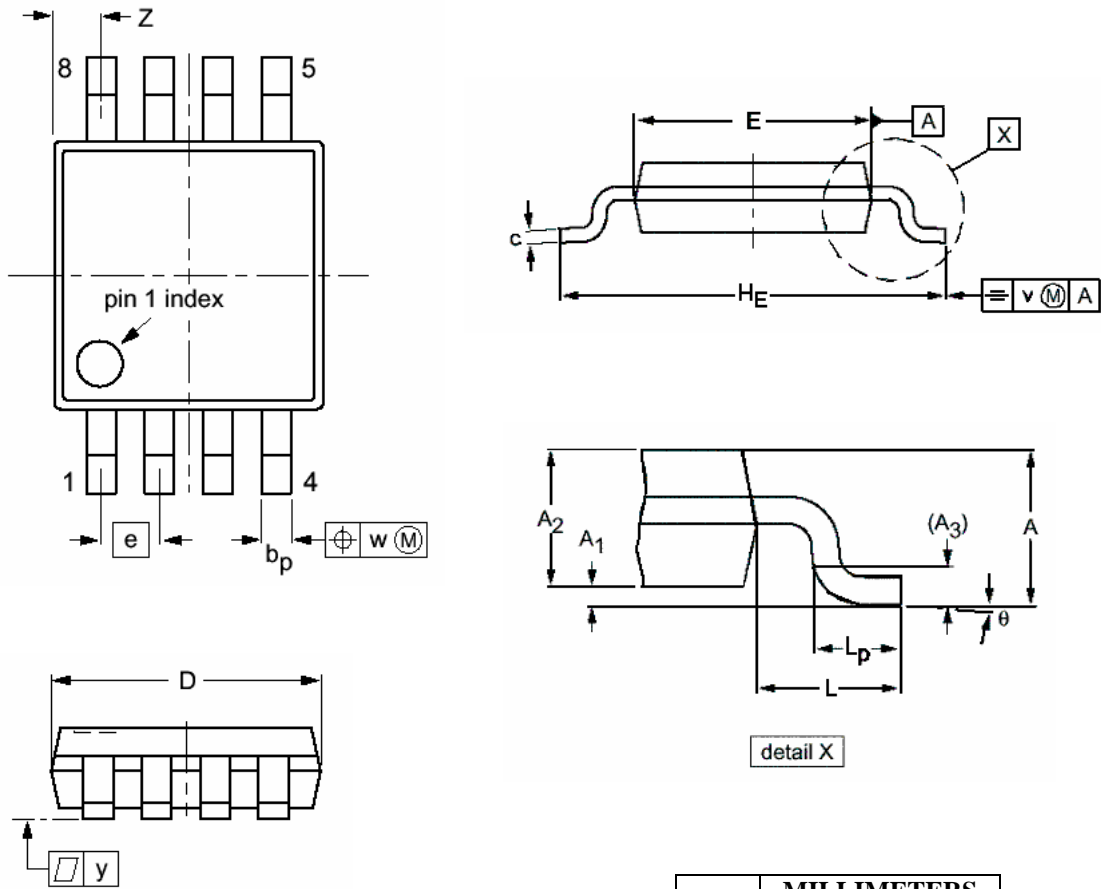
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	.053	0.069
A ₁	0.10	0.25	0.004	0.010
A ₂	1.28	1.57	0.050	0.062
A ₃	0.25		0.01	
b _p	0.36	0.49	0.014	0.019
c	0.19	0.25	0.0075	0.0100
D	4.80	5.00	0.19	0.20
E	3.80	4.00	0.15	0.16
e	1.27		0.050	
H _E	5.80	6.20	0.228	0.244
L	1.05		0.041	
L _p	0.40	1.27	0.016	0.050
Q	0.60	0.70	0.024	0.028
v	0.25		0.01	
w	0.25		0.01	
y	0.10		0.004	
Z	0.30	0.70	0.012	0.028
θ	0°	8°	0°	8°

NOTES:

1. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
2. MAXIMUM MOLD PROTRUSION FOR D IS 0.15mm.
3. MAXIMUM MOLD PROTRUSION FOR E IS 0.25mm.

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**PACKAGE DIAGRAM
TSSOP 8**



- NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
 2. MAXIMUM MOLD PROTRUSION FOR D IS 0.15mm.
 3. MAXIMUM MOLD PROTRUSION FOR E IS 0.25mm.

DIM	MILLIMETERS	
	MIN	MAX
A		1.10
A ₁	0.05	0.15
A ₂	0.75	0.95
A ₃	0.25	
b _p	0.22	0.40
c	0.13	0.23
D	2.90	3.10
E	2.90	3.10
e	0.65	
H _E	4.75	5.05
L	0.95	
L _p	0.40	0.70
v	0.10	
w	0.08	
y	0.10	
Z	0.38	0.64
θ	0°	6°

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