2-channel BTL driver for CD players

BA5912AFP-Y

The BA5912AFP-Y is a 2-channel BTL driver developed to drive CD player motors and actuators. Perfect for compact applications with the use of the HSOP 25-pin package.

●Applications

CD players, CD-ROM

●Features

1) 2-channel BTL driver.
2) Perfect for compact applications with the use of the HSOP 25-pin power package.
3) Wide dynamic range.
4) External mute pin enables the muting of the output current (independent muting for channels 1 and 2). Muting both channels causes the IC to enter the standby mode.
5) Two internal multi-purpose operational amplifiers.
6) Power supply is divided into three systems (Pre V_{CC}, Pow V_{CC} for channel 1, and Pow V_{CC} for channel 2)
7) Internal standard two operational amplifier.
8) Internal thermal shutdown circuit.

●Absolute maximum ratings (Ta = 25 °C)

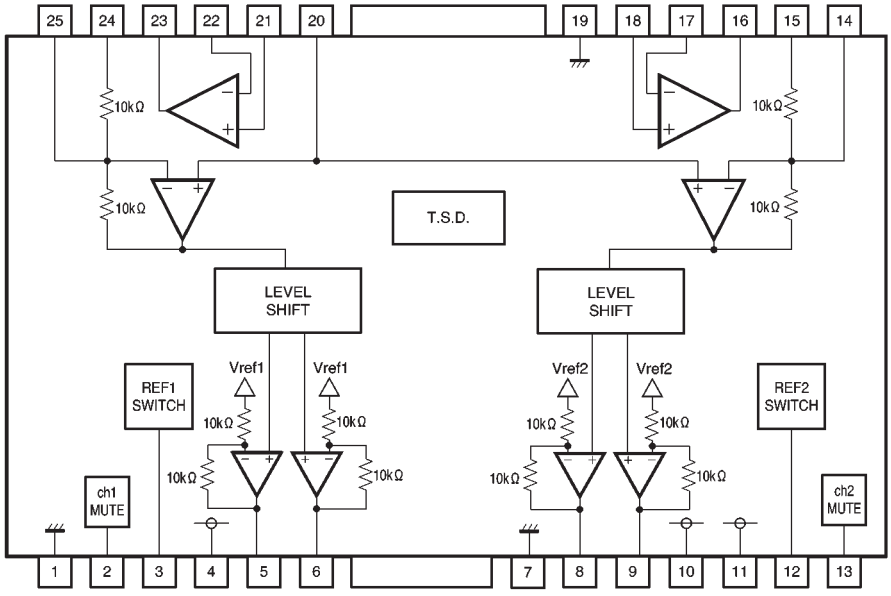
Parameter	Symbol	Limits	Unit
Power supply voltage	V_{CC}	13.5	V
Power dissipation	Pd	1.45*1	W
Operating temperature	Topr	−35～+85	℃
Storage temperature	Tstg	−55～+150	℃

*1 When mounted on a 70mm×70mm×1.6mm glass epoxy board with copper foil coverage of less than 3%. Reduced by 11.6mW for each increase in Ta of 1℃ over 25℃.

●Recommended operating conditions (Ta = 25 °C)

Parameter	Symbol	Limits	Unit
Power supply voltage	Pre V_{CC}	4.5～13.2	V
Power-stage power supply voltage	Pow V_{CC}	4.5～Pre V_{CC}	V

●Block diagram



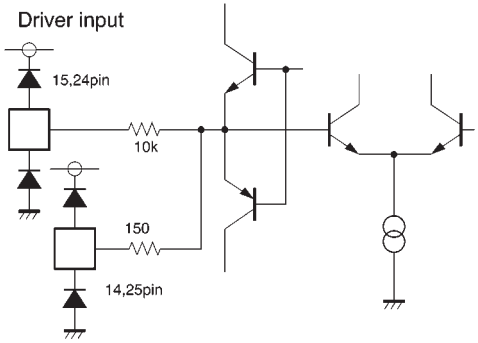
●Pin descriptions

Pin No.	Pin name	Function	Pin No.	Pin name	Function
1	GND	Substrate GND	14	IN2'	Input for channel 2 gain adjustment
2	MUTE1	Channel 1 mute	15	IN2	Channel 2 gain fixed input
3	REF1	Channel 1 Vref switch	16	OP1-OUT	Op-amp 1 output
4	Pow Vcc1	Pow Vcc (channel 1)	17	OP1-IN−	Op-amp 1 negative input
5	OUT1−	Channel 1 negative output	18	OP1-IN+	Op-amp 1 positive input
6	OUT1+	Channel 1 positive output	19	GND	Substrate GND
7	GND	Substrate GND	20	BIAS	Bias input
8	OUT2+	Channel 2 positive output	21	OP2-IN+	Op-amp 2 positive input
9	OUT2−	Channel 2 negative output	22	OP2-IN−	Op-amp 2 negative input
10	Pow Vcc2	Pow Vcc (channel 2)	23	OP2-OUT	Op-amp 2 output
11	Pre Vcc	PreVcc	24	IN1	Channel 1 gain fixed input
12	REF2	Channel 2 Vref switch	25	IN1'	Input for channel 1 gain adjustment
13	MUTE2	Channel 2 mute			

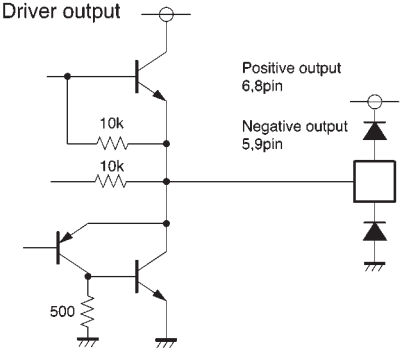
Note: Positive output and negative output are the polarities with respect to the input.

●Input / output circuits

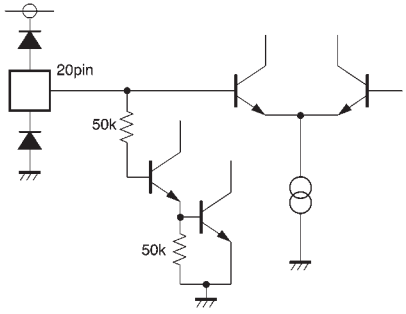
Driver input



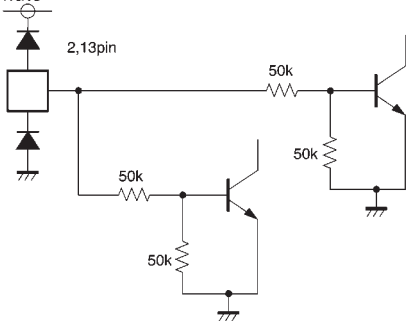
Driver output



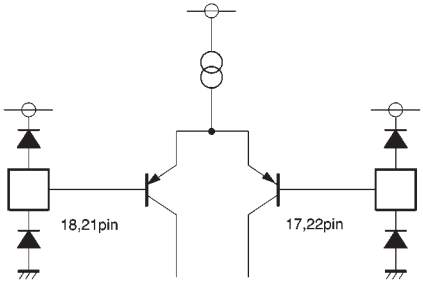
Bias



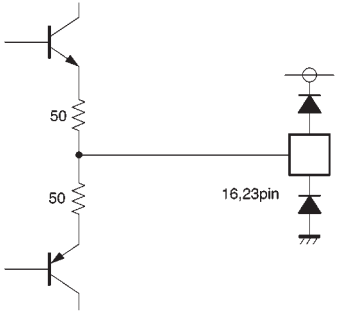
Mute



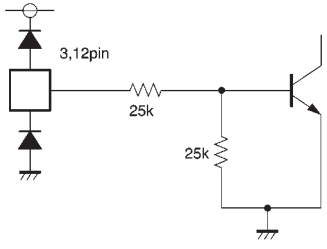
Op-amp input



Op-amp output



Vref switch



●Electrical characteristics (unless otherwise noted, Ta = 25 °C, Pre V_{CC} = Pow V_{CC} = 5V, BIAS = 2.5V, R_L = 8Ω)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Circuit current	I_{CC}	—	9.0	14.0	mA	No load, REF1, 2≧2.0V
Circuit current during standby	I_{SCC}	—	0	100	μA	No load, REF1, 2≦0.5V
〈Driver〉						
Output offset voltage	V_{OO}	−50	—	50	mV	
Maximum output amplitude 1	V_{OM1}	3.2	3.5	—	V	REF1, 2≦0.5V
Maximum output amplitude 2	V_{OM2}	3.7	4.0	—	V	Pre V_{CC}=12V, Pow V_{CC}=5V REF1, 2>2.0V
Closed-loop voltage gain	G_{VC}	10.0	11.5	13.0	dB	V_{IN}=BIAS±0.5V
Mute on voltage	V_{MON}	GND	—	0.5	V	
Mute off voltage	V_{MOFF}	2.0	—	V_{CC}	V	
Vref switch voltage 1	V_{ref1}	GND	—	0.5	V	Pre V_{CC}=Pow V_{CC}
Vref switch voltage 2	V_{ref2}	2.0	—	V_{CC}	V	Pre V_{CC}>Pow V_{CC}+VF
〈Operational amplifier〉						
Offset voltage	V_{OFOP}	−5	0	5	mV	
Input bias current	I_{BOP}	—	—	300	nA	
Output high level voltage	V_{OHOP}	4.00	4.36	—	V	
Output low level voltage	V_{OLOP}	—	0.74	1.1	V	
Output drive current sink	I_{SINK}	10	50	—	mA	50Ω at V_{CC}
Output drive current source	I_{SOURCE}	10	40	—	mA	50Ω at GND
Slew rate	SR_{OP}	—	1	—	V/μs	100kHz rectangular wave, $4V_{P-P}$ output

●Measurement circuits

〈Driver block〉

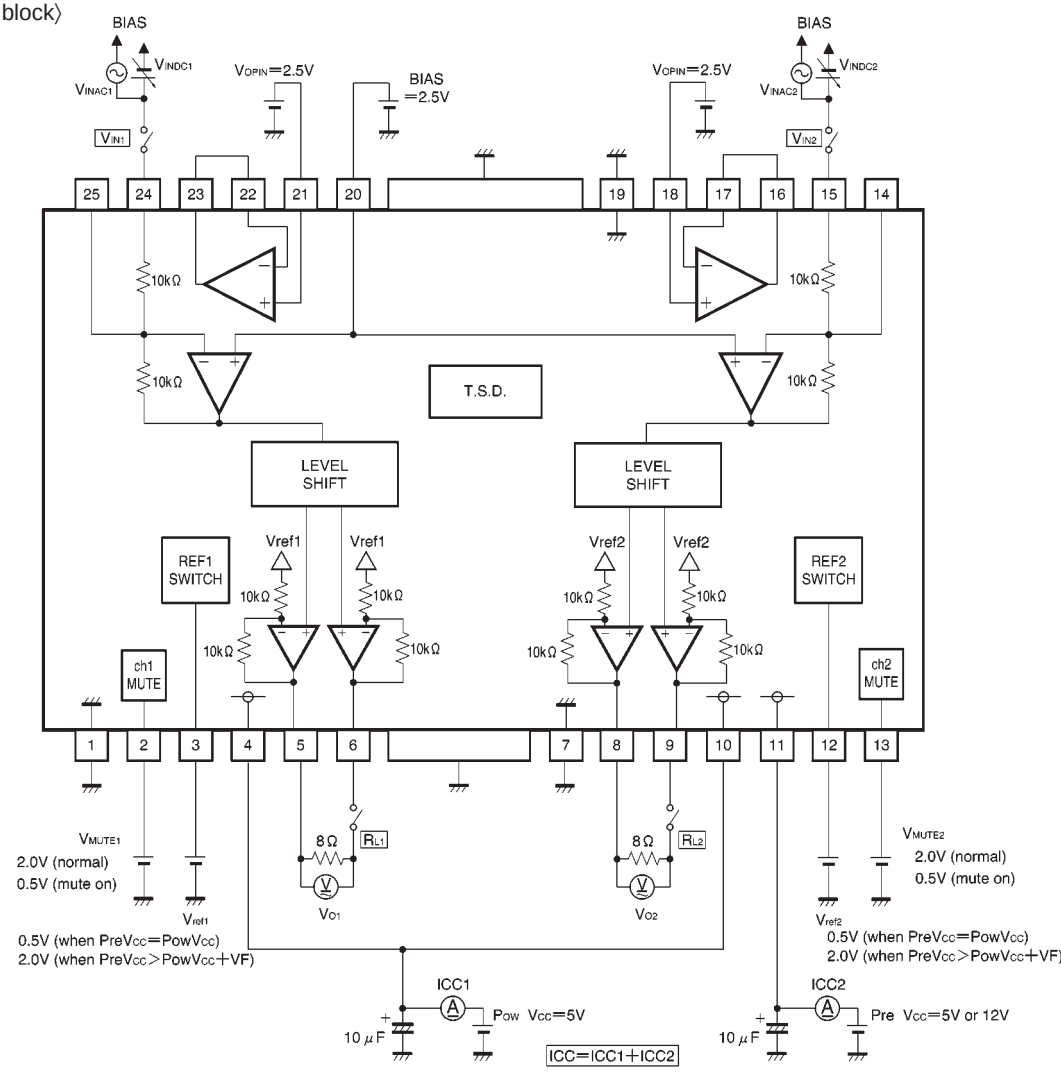


Fig.1

〈Operational amplifier block〉

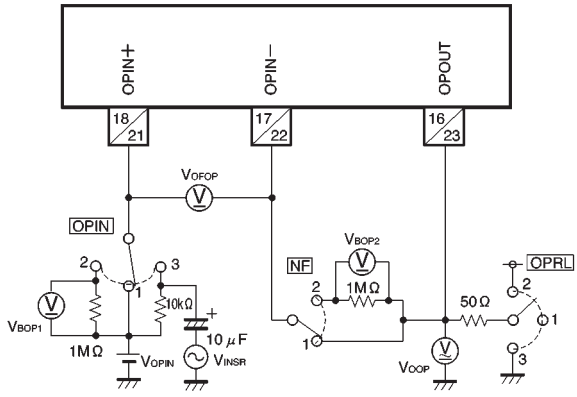


Fig.2

●Application example

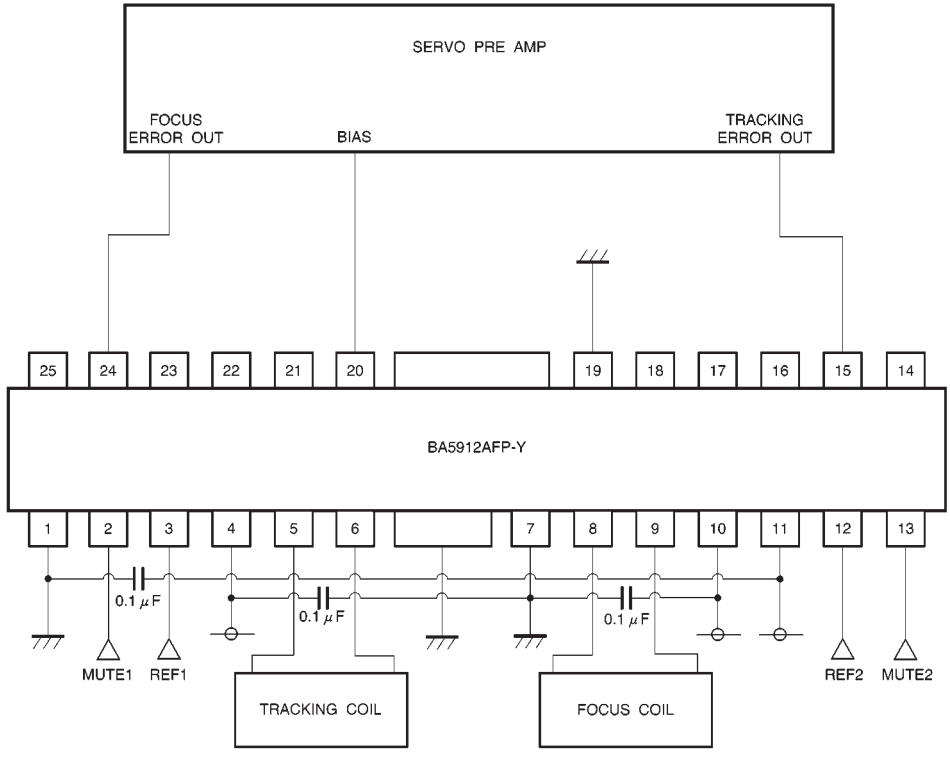


Fig.3

●Operation notes

(1) The BA5912AFP-Y contains a thermal shutdown circuit. When the chip temperature reaches 175°C (Typ.), the output current is muted. If the chip temperature then drops below 150°C (Typ.), then the mute is released.

(2) By having the voltage of the mute pins (pins 2 and 13) open or lowered to 0.5V or below, you can independently mute the output current for channels 1 and 2. For normal conditions, have the voltages for the mute pins (pins 2 and 13) pulled up to 2.0V or greater. If the both mute pins (pins 2 and 13) are open or 0.5V or less, then the IC automatically enters the standby mode.

(3) If the voltage of the bias pin (pin 20) drops below 1.4V (Typ.), outputs are muted. For normal conditions, have the voltage above 2.0V.

(4) If the power supply voltage drops below 3.5V (Typ.), internal circuits turn off. If the power supply voltage then rises to 4.0V (Typ.), the circuits turn on.

(5) If the voltage of the thermal shutdown, mute ON, or bias pin drops, or if the power supply voltage drops, the mute is activated; however, in these situations, only the drivers are muted. Also, the output pin voltage becomes the internal bias voltage.

(6) When Pre V_{CC} = Pow V_{CC}, have the Vref switch pin open or at 0.5V or less (internal bias voltage = (Pow V_{CC} − VF) / 2). When Pre V_{CC} > Pow V_{CC} + VF, have the Vref switch pin pulled up to 2.0V (internal bias voltage = Pow V_{CC} / 2).

(7) Connect a bypass capacitor (approx. 0.1μF) between the bases of the power supply pins of this IC.

(8) Even though the radiation fins are connected to ground within the package, be sure to also connect them to a ground externally as well.

●Electrical characteristic curves

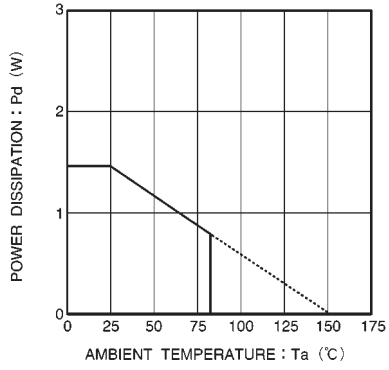


Fig.4 Thermal derating curve

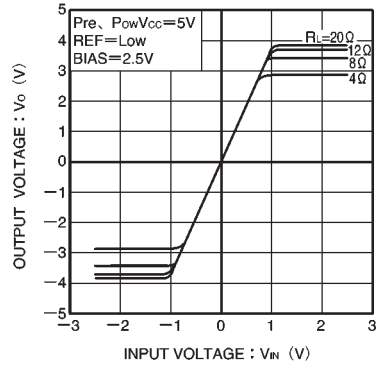


Fig.5 Driver I / O characteristics
(When PreVcc=PowVcc, with load regulation)

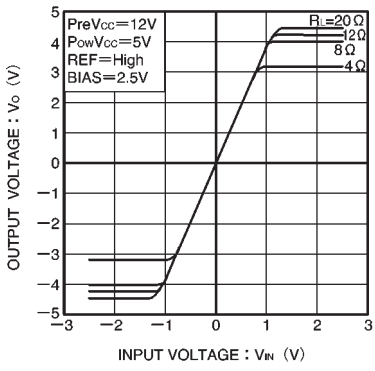


Fig.6 Driver I / O characteristics
(When PreVcc≧PowVcc+VF, with load regulation)

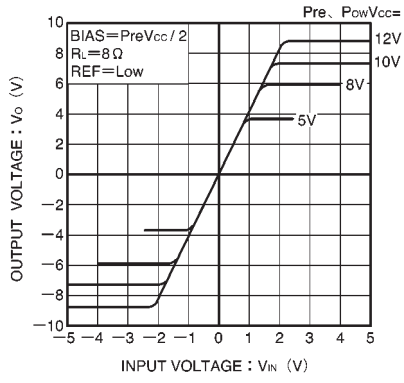


Fig.7 Driver I / O characteristics
(With PreVcc and PowVcc regulation)

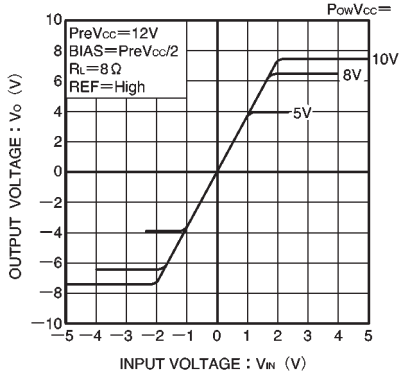


Fig.8 Driver I / O characteristics
(With PowVcc regulation)

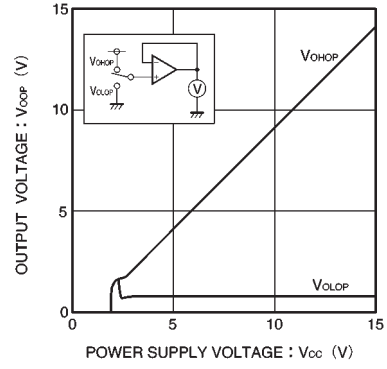
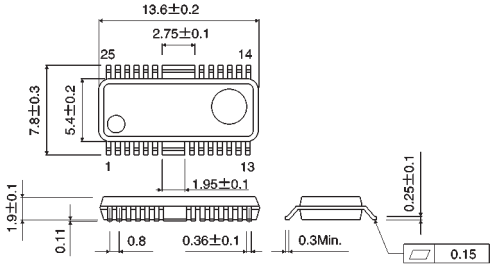


Fig.9 Power supply voltage vs.
op-amp output voltage

●External dimensions (Units: mm)



HSOP25