

VIF/SIF signal processor

BA7356S

The BA7356S is a multi-format (M, B/G, D/F, and I) VIF/SIF signal processor for television and VCR applications. It features a built-in sound-trap and band-pass filters, and employs a pulse-count audio detector that does not require adjustment. This IC reduces external component requirements, and allows space savings.

● Applications

TVs and VCRs

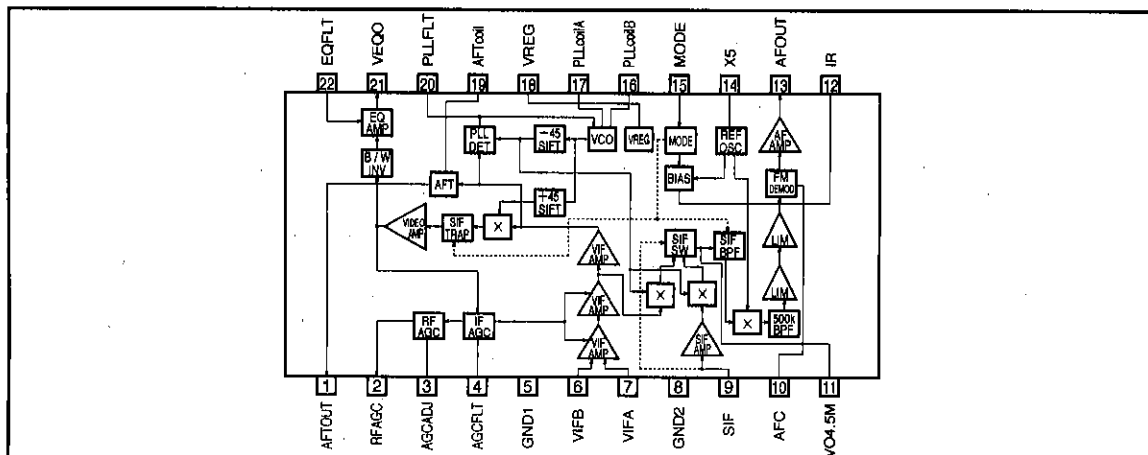
● Features

- 1) Separate-carrier PLL with full synchronous detection. Excellent DG/DP, CS beat (920kHz) and cross color. In addition, by pulling down the SIF input (pin 9) it can be used as an intercarrier.
- 2) The IF AGC time constant is dual-layered to allow faster speeds.
- 3) The variable-gain amplifier has excellent linearity to ensure low distortion, and AGC variance and temperature drift have been minimized.
- 4) Built-in SOUND filter (SOUND trap and SOUND BPF). The MODE switch can be used to switch between M, B/G, I, and D/K (4.5MHz, 5.5MHz, 6.0MHz, and 6.5MHz

respectively). In particular, the SOUND BPF gives a larger attenuation ratio than conventional discrete circuits by using two-layer SIF+500kHz BPFs.

- 5) The audio detector uses a 500kHz BEAT DOWN pulse-counter detector that does not require adjustment. This eliminates the need for a detector coil and gives better linearity and S/N.
- 6) Use of pulse-counter detection and the built-in SOUND filter means fewer pins, external components and adjustment locations are required. The IC is available in a 22-pin SDIP package and will enable cost and space savings.

● Block diagram



● Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Applied voltage	V _{CCMax}	10.5 *1	V
Power dissipation	P _{dMax}	1250 *2	mW
Operating temperature	T _{opr}	-15 ~ 65	°C
Storage temperature	T _{stg}	-40 ~ 150	°C
Pin 2 input voltage	V _{P2Max}	10.5	V

*1 27 Ω resistor connected between V_{CC} and V_{REG}.

*2 When IC is stand alone, reduced by 12.5mW for each increase in Ta of 1°C over 25°C.

● Recommended operating conditions (Ta=25°C)

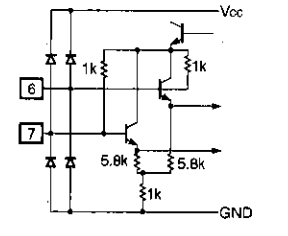
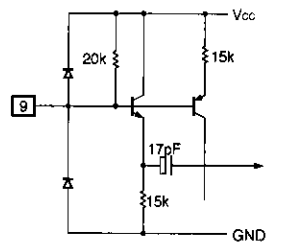
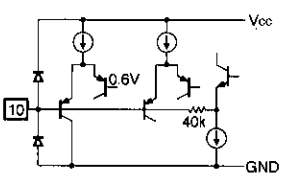
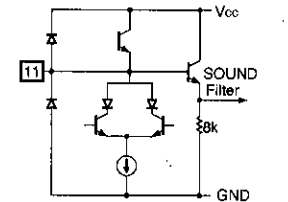
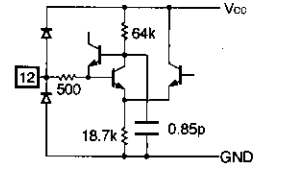
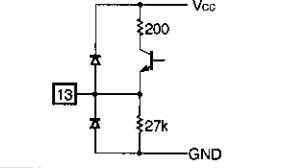
Parameter	Symbol	Limits	Unit
Power supply voltage (9V)	V _{CC 9V}	8.8 ~ 9.2 *1	V
Power supply voltage (12V)	V _{CC 12V}	11.7 ~ 12.3 *2	V

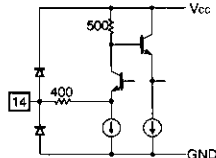
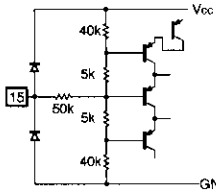
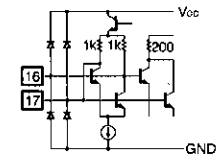
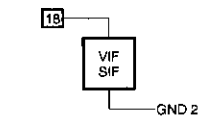
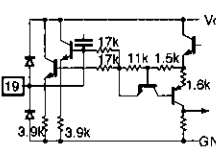
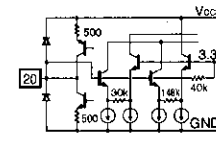
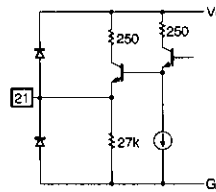
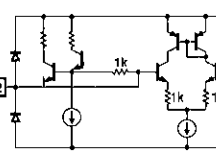
*1 27 Ω resistor connected between V_{CC} and V_{REG}.

*2 62 Ω resistor connected between V_{CC} and V_{REG}.

● Pin description

Pin No.	Pin Name	IN / OUT	Standard voltage	Equivalent circuit	Function
1	AF - TOUT	OUT	—		AFT output. VREG/GND push-pull output.
2	RF - AGC	OUT	—		RF-AGC output. Open-collector output. Gain can be set using an external resistor (minimum value of the maximum sink current of pin 2 is 0.7mA). Keep the pin 2 voltage at 10.5V or less.
3	AGC - ADJ	—	2.1V (when 100kΩ resistor connected)		RF-AGC delay point adjustment. Connect to GND via a variable resistor (approx. 100kΩ).
4	AGC - FLT	—	5.0V		For filter time constant for VIF AGC.
5	GND1		0V		GND for VIF, AGC and AFT.

Pin No.	Pin Name	IN / OUT	Standard voltage	Equivalent circuit	Function
6 7	VIFB VIFA	IN	4.2V		Video IF input. Use with balanced input.
8	GND2	—	0V		SIF and PLL GND.
9	SIF	IN	6.6V		Audio IF input. Can set to intercarrier mode by pulling down via a 2k Ω resistor.
10	AFC	—	2.7V		Holding the audio output DC level fixed. Connect to GND via a 4.7 μF capacitor and to VREG via a 10 μF capacitor to reduce buzz. Set this pin to 0.3V or lower to apply audio/video mute.
11	VO - 4.5M	—	5.2V		2nd SIF output. Connect a trap to this pin to vary the sound filter characteristics. The internal impedance is a high 1k Ω, so connect a buffer to output.
12	IR	—	2.4V		Reference current source for adjusting the internal filter. Use connected to GND via a 24k Ω resistor. Use an accurate resistor with good temperature characteristics (e.g. ±1% metal film).
13	AFOUT	OUT	3.2V		Audio signal output. The standard output in the case of B/G is 520mVrms (when f = 50kHz). Connect to GND via a 10k Ω resistor.

Pin No.	Pin Name	IN / OUT	Standard voltage	Equivalent circuit	Function
14	X5	—	5.0V		For connection to a 5MHz oscillator (when M format is used). Use as a reference oscillator for automatic adjustment of the internal filter, and as the signal for the SIF signal low frequency conversion. (B/G, D/K format: 6MHz, I format: 6.5MHz).
15	MODE	IN	3.4V		Input Trap Filter switch. 0V: M format (4.5MHz) 2.4V: D/K format (6.5MHz) 4.3V: I format (6.0MHz) VREG: B/G format (5.5MHz)
16 17	PLL - COILA PLL - COILB	—	3.6V		For connection of IF detector VCO oscillator coil.
18	VREG	—	6.6V		IF circuit power supply. Pin 18 has a built-in shunt regulator.
19	AFT - COIL	—	3.0V		For connection of AFT coil. To apply AFT defeat, connect to GND via a 1kΩ (approx.) resistor.
20	PLL - FLT	—	3.4V		Time constant circuit for the PLL filter.
21	VEQO	OUT	2.0V (SYNC)		VIDEO output. Output is via the sound trap, B/W noise inverter, and EQ AMP. Connect to GND via a 4.7kΩ resistor.
22	EQFLT	—	5.2V		EQ Filter. Connect to GND via an LCR series resonant circuit. R should be ≥ 1kΩ

* Vcc and Vcc2 in the equivalent circuit diagrams are connected to the VREG pin (pin 18).

●Electrical characteristics (Unless otherwise specified Ta=25°C, Vcc=9V, and P=38.9MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	
(VREG)							
Circuit current	I _{CC}	—	92	105	mA		
Regulated voltage	V _{REG}	6.2	6.6	7.0	V		
(VIF)							
Input sensitivity	V _{VMin.}	38	43	48	dB μ	V _{VO} = -3dB point	
Maximum allowable input level	V _{VMax.}	100	110	—	dB μ	V _{VO} = +1dB point	
AGC range	GR	62	66	—	dB	V _{VO} = \pm 3dB range	
Quiescent video output voltage	V _{P21}	3.9	4.3	4.7	V	No signal, V _{P4} = V _{REG}	
Video detector output level	V _{VO}	1.7	2.0	2.4	V _{P-P}	V _i = 80dB μ , AM87.5%MOD	
Synchronous signal tip voltage	V _{P21SY}	1.7	2.0	2.3	V	100% white video signal	
Video output DG	DG	—	2	8	%	V _i = 80dB μ , AM87.5%MOD	
Video output DP	DP	—	3	8	deg	3STEP video signal	
Sound Trap attenuation	M, B / G	G _{VOS}	33	45	—	dB	20 * LOG (V _{OS} / V _{O0.2M})
	D / K, I		28	45	—		
920kHz beat level	I ₉₂₀	37	44	—	dB	P=0, P / C=4, P / S=14dB	
Video output S/N	S / N _v	47	53	—	dB	V _i = 90dB μ , 100% white	
White noise threshold voltage	V _{WTH}	4.7	5.0	5.3	V	CW = 70dB μ frequency variation and pin 21 voltage variation	
White noise clamp voltage	V _{WCL}	2.9	3.2	3.5	V		
Black noise threshold voltage	V _{BTH}	1.1	1.4	1.7	V		
Black noise clamp voltage	V _{BCL}	2.6	2.9	3.2	V		
RFAGC maximum sink current	I _{P2SI}	0.7	1.2	—	mA	CW=100dB μ , AGCADJ=100k	
(AFT)							
Maximum AFT voltage	V _{P1Max.}	6.0	6.4	—	V	CW=38.4MHz	
Minimum AFT voltage	V _{P1Min.}	—	0.3	0.8	V	CW=39.4MHz	
AFT detection sensitivity	S _i	35	50	—	mV / kHz	CW frequency variation	
AFT defeat starting voltage	V _{AFTDET}	—	—	1.2	V	CW=38.4MHz	
AFT defeat voltage	V _{1DEF}	2.9	3.3	3.6	V	CW=38.4MHz	
(PLL)							
PLL capture range 1	f _{CU}	0.6	+1.2	—	MHz	CW = 80dB μ frequency variation	
PLL capture range 2	f _{CL}	—	-1.2	-0.6	MHz		
PLL lock range 1	f _{LU}	0.6	+1.3	—	MHz		
PLL lock range 2	f _{LL}	—	-1.3	-0.6	MHz		
VCO control sensitivity	β	0.5	1.0	—	kHz / mV		

● Application example

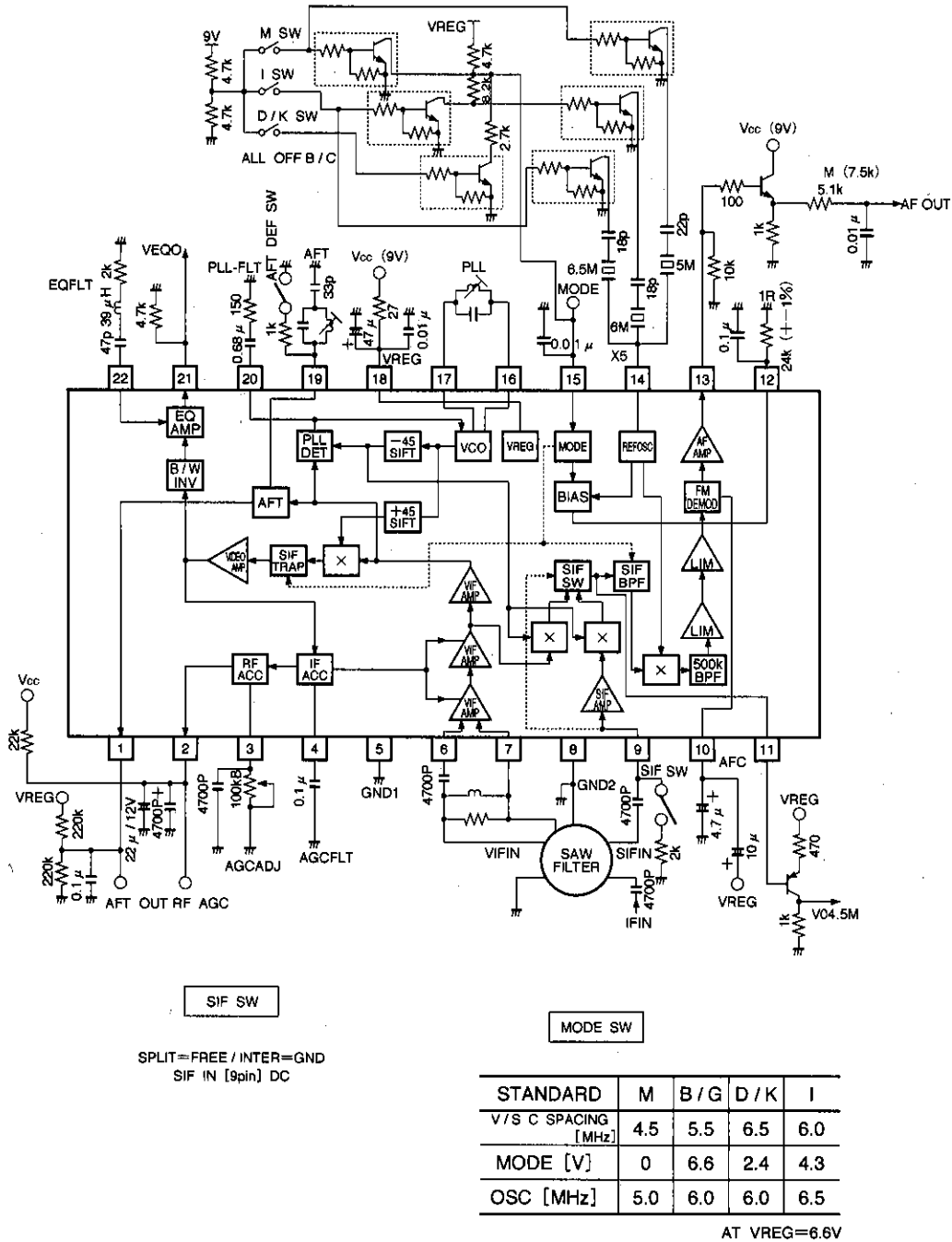


Fig.2

● Operation notes

- Simultaneous audio and video output muting function
It is possible to simultaneously mute the audio and video output by pulling the AFC filter pin down.
- AFT defeat function
AFT defeat can be applied by pulling the AFT coil pin down via a 1kΩ resistor.
- Recommended SIF input range for intercarrier mode P/S=20 to 30dB (including SAW-FILTER).
- IF input range for RF-AGC switching
60 to 95dB μ.
- Intercarrier mode switching
Intercarrier mode can be set by pulling the SIF pin down via a 2kΩ resistor.
- IR pin external resistor
This resistor sets the filter system reference current, so use an accurate component that has good temperature characteristics.

- Adjustment of the evaluation board
Before performing measurements, adjust the coils as described below.

1. VCO coil

Lower the VIF input level, and apply a voltage of AGCFLT=6V. Monitor the PLL-FIL voltage (V1). Next, input a signal of VIFIN=80dB μ, 38.9MHz, and with the AGCFLT free, adjust the VCO so that the voltage at this time, V2, becomes the same as V1.

2. AFT coil

Input a signal of VIFIN=80dB μ, 38.9MHz, set the AFT defeat switch to open, and monitor the AFT output pin voltage. Rotate the AFT coil, adjust the output voltage to 1/2VREG (Typ. 3.3V) at the point where the output voltage changes steeply.

● External dimensions (Units: mm)

