

75Ω driver with Y / C MIX circuit

BA7664FV

The BA7664FV is a 75Ω driver with a 6dB amplifier and a Y / C MIX circuit. The 75Ω driver is capable of driving a load sufficient for two circuits, as well as being equipped with a sag correction function which reduces the capacitance of the output coupling capacitor. The IC comes in the compact 8-pin SSOP-B package. The composite Y signal input pin is sync chip clamped input, while the chrominance input pin is bias input. An internal power-saving circuit is also included which provides an output muting function and output pin shorting protection.

●Applications

Video cameras, electronic cameras and others

●Features

- 1) The compact 8-pin SSOP-B package is used.
- 2) Operates at a low power consumption (60mW Typ.).
- 3) Internal Y / C MIX circuit.
- 4) Internal output muting circuit.
- 5) Internal power-saving circuit.
- 6) Internal output protection circuit.
- 7) Internal sag correction function makes it possible to reduce the capacitance of the output coupling capacitor.
- 8) A load sufficient for two circuits can be driven.

●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V _{cc}	8	V
Power dissipation	P _d	350	mW
Operating temperature	T _{opr}	- 25 ~ + 75	°C
Storage temperature	T _{stg}	- 55 ~ + 125	°C

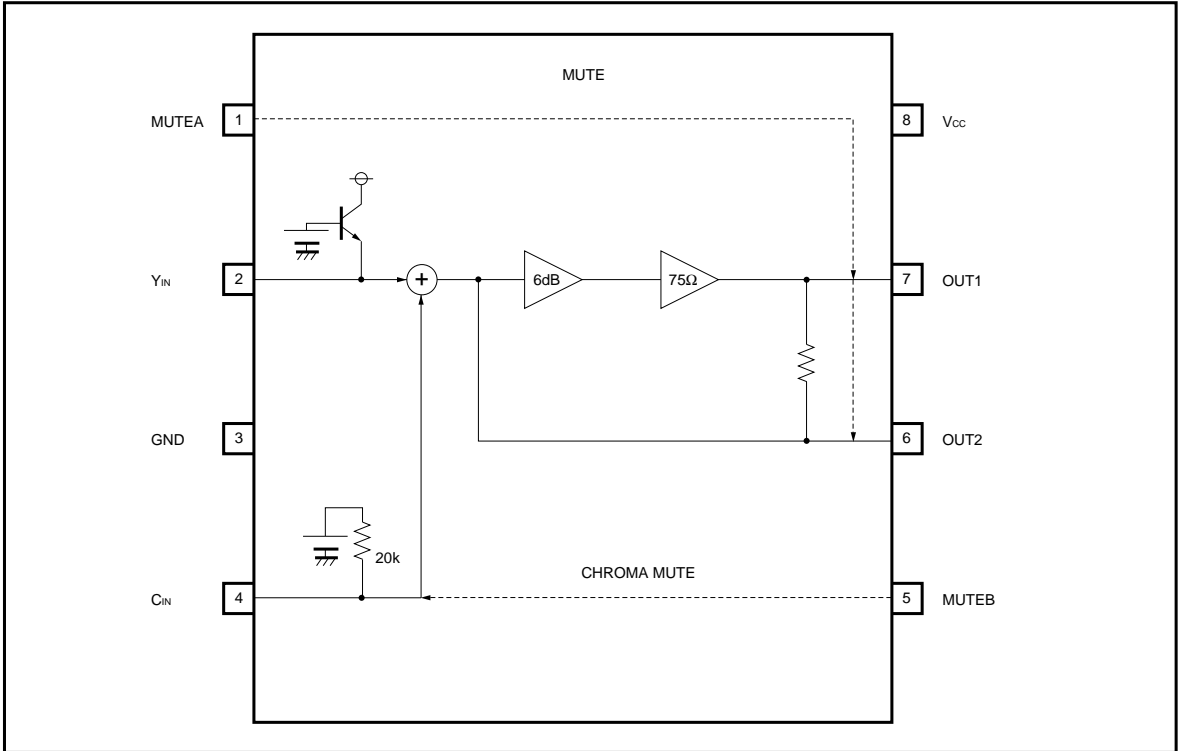
* Reduced by 3.5mW for each increase in Ta of 1°C over 25°C

●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating power supply voltage	V _{cc}	4.5	5.0	5.5	V

*Not designed for radiation resistance.

●Block diagram



●Pin descriptions and input / output circuits

Pin. No	Pin name	IN	OUT	Reference potential	Equivalent circuit	Pin description
1 5	MUTEA MUTEB	○	—	—		<p>Muting control</p> <p>If MUTEA (pin 1) is set to HIGH, the output is muted. If MUTEB (pin 8) is set to HIGH, only the chrominance signal is muted. (The Y signal is output without being muted.)</p>
2	Y _{IN}	○	—	2.0V		<p>Signal input</p> <p>This is the input pin for composite Y signals, and is sync chip clamped input.</p>
3	GND	—	—	0V		<p>Ground</p>
4	C _{IN}	○	—	2.0V		<p>Signal input</p> <p>This is the input pin for chrominance signals, and is bias-type input. The input impedance is 20kΩ.</p>
6 7	MIXOUT2 MIXOUT1	—	○	0.9V 0.95V		<p>Signal output</p> <p>These are the Y / C MIX signal output. Pin 6 is the pin for sag correction. If pin 7 is set to 0.2V or less, the protective circuit is triggered and the power-saving mode is accessed.</p>
8	V _{CC}	—	—	5.0V		<p>Power supply</p>

●Electrical characteristics (unless otherwise noted, $T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Circuit current	I_{CC}	6.1	12.2	18.3	mA	With no signal
Max. output level	V_{om}	2.6	3.0	—	V_{P-P}	$f = 1\text{kHz}$, $\text{THD} = 1\%V_{O2}$
Voltage gain	G_V	-1.0	-0.2	0.6	dB	$f = 4.43\text{MHz} / V_{O1}$
Frequency characteristic	G_F	-1.5	-0.5	0.5	dB	$f = 7\text{MHz} / 1\text{MHz}$, $1V_{P-P} / V_{O1}$
Muting attenuation	M_T	—	-60	—	dB	$f = 4.43\text{MHz}$, $1V_{P-P} / V_{O1}$
Muting switching high level	V_{THH}	2.2	—	V_{CC}	V	—
Muting switching low level	V_{THL}	0	—	0.7	V	—
Input impedance	Z_{IN}	16	20	24	$k\Omega$	Chrominance input pin (pin 7)
Circuit current when muted	I_{MUTE}	—	1.3	2.6	mA	MUTEA "H"

●Guaranteed design parameters (unless otherwise noted, $T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Differential gain	DG	—	1.0	2.0	%	$V_{IN} = 1.0V_{P-P}$ reference staircase signal
Differential phase	DP	—	0.5	2.0	DEG	$V_{IN} = 1.0V_{P-P}$ reference staircase signal

●Mute switch mode settings

• MUTEA (1pin)

H	MUTE
L	NORMAL

• MUTEB (5pin)

H	CHROMA MUTE
L	NORMAL

●Measurement circuit

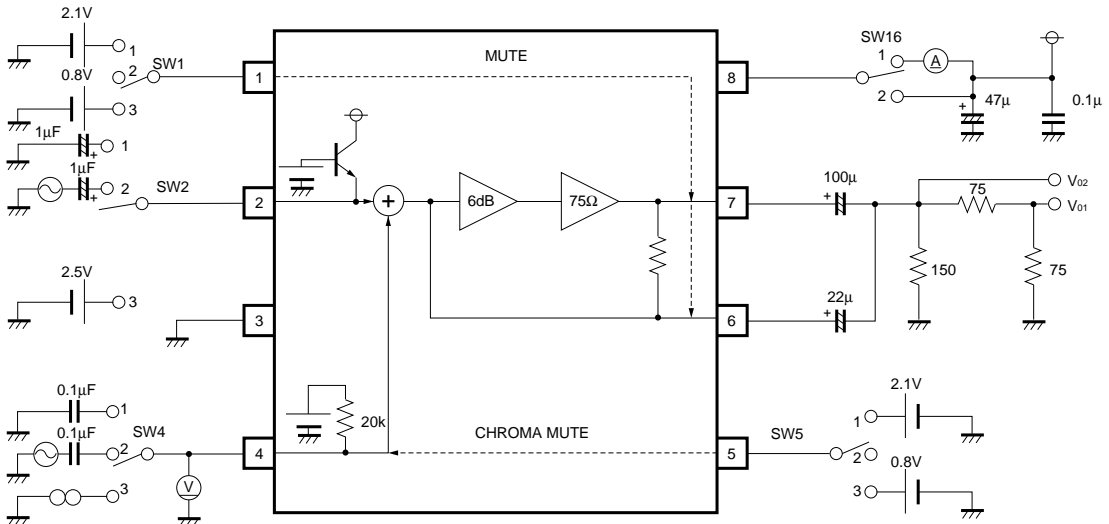


Fig.1

●Measurement conditions

Parameter	Symbol	SW Conditions					Measurement method	
		1	2	4	5	8		
Circuit current	I _{CC}	2	1	1	2	1	*1	
Max. output level	V _{OM}	3	2	1	3	2	*2	
Voltage gain	Y→OUT	G _{V1}	3	2	1	3	2	*3
	C→OUT	G _{V2}	3	3	2	3	2	*3
Frequency characteristic	G _F	3	1	2	3	2	*4	
Muting attenuation	M _T	1	2	1	3	2	*5	
Chroma muting attenuation	M _{TC}	3	3	2	1	2	*5	
Input impedance	Z _{IN}	3	1	3	3	2	*6	
Circuit current when muted	I _{MUTE}	1	1	1	2	1	*7	

* The muting switching level is substituted by carrying out the above measurement at H = 2.1V, L = 0.8V.

Measurement method

- *1 Measure the circuit current when no signal is present.
- *2 Apply a sine wave of f = 1kHz to the input, and adjust the input level so that the output distortion is 1%.
At this time, set the output voltage to the maximum output level of V_{OM} [V_{P-P}].
- *3 Measure the output V_O [V_{P-P}] with a sine wave of f = 4.43MHz, 1V_{P-P} applied to the input.
Voltage gain G_V is: $G_V = 20 \text{ Log } (V_O / V_{IN})$ [dB]
- *4 Measure the outputs V_{O7} and V_{O1} [V_{P-P}] each with sine waves of f = 7MHz, 1V_{P-P} and f = 1MHz, 1V_{P-P} applied to the input.
Voltage frequency G_F is: $G_F = 20 \text{ Log } (V_{O7} / V_{O1})$ [dB]
- *5 Measure the output V_O [V_{P-P}] with a sine wave of f = 4.43MHz, 1V_{P-P} applied to the input.
The muting attenuation M_T is: $M_T = 20 \text{ Log } (V_O / V_{IN})$ [dB]
- *6 Measure the input voltage V_{IN0} [V] and the open voltage of the input V_{INO} [V] when 50μA is introduced.
The input impedance Z_{IN} is: $Z_{IN} = [V_{IN0} - V_{INO}] / 50 \times 1000$ [kΩ]
- *7 Measure the circuit current when MUTEA (pin 1) is HIGH.

●Application examples

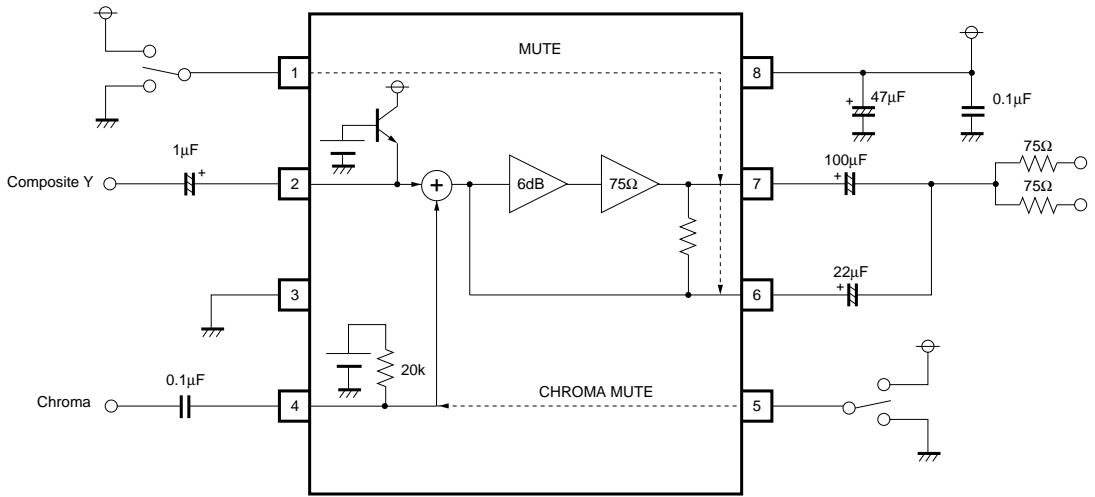


Fig.2

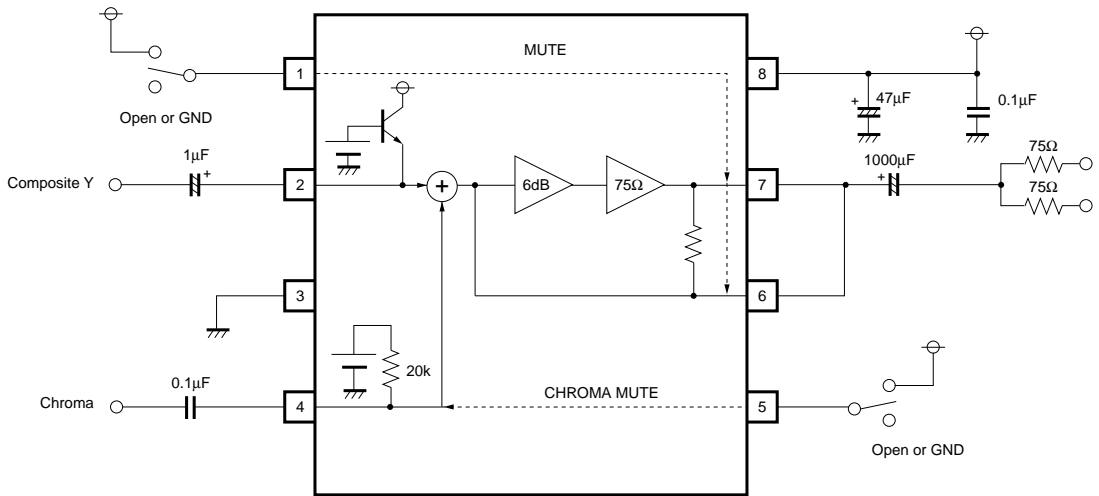


Fig.3

●External dimensions (Units: mm)

