3-phase brushless motor pre-driver

BD63002MUV

●General Description

BD63002MUV is pre-driver of 3-phase brushless motor. It generates a driving signal from the Hall sensor and drives PWM through the input control signal. Since there is a built-in booster circuit, Nch-Nch MOS transistors can be used on the external power transistor. In addition, the power supply can use 12V or 24V and it has various controls and protection functions built-in, making it useful for a variety of purposes. Because it adopts small packages, it can also be used on small diameter motors.

●Key Specifications

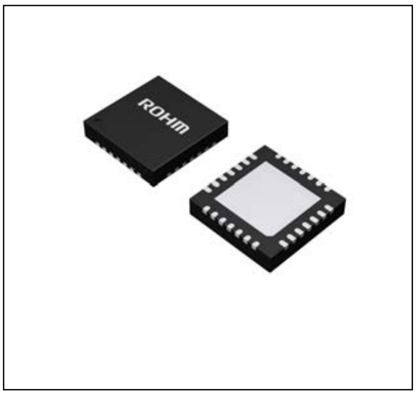
- Power supply voltage rating: 30V
- Operating temperature range: -40°C to +85°C
- Stand-by current: 1.2mA(Max.)
- Range of in-phase input voltage for hall input: V_{REG}-1.7V(Max.)
- Current limit detect voltage: 0.2V±10%
- UVLO Lock out voltage: 6.0V(Typ.)
- OVLO Lock out voltage 1: 16.0V(Typ.)
- OVLO Lock out voltage 2: 28.5V(Typ.)

●Features

- Built-in 120° commutation logic circuit.
- Driving with Nch-Nch MOS transistors.
- PWM control mode (low side arm switching).
- Built-in power-saving circuit.
- CW/CCW function.
- Short brake function.
- FG output (Open drain).
- Built-in protection circuit for current limiting, overheating, under voltage, over voltage, motor lock.

●Package

Package	W(Typ) x D(Typ) x H(Max)
VQFN028V5050	5.00mm x 5.00mm x 1.00mm



VQFN028V5050

●Applications

- OA machines.
- Other general civil equipments.

●Typical Application Circuit

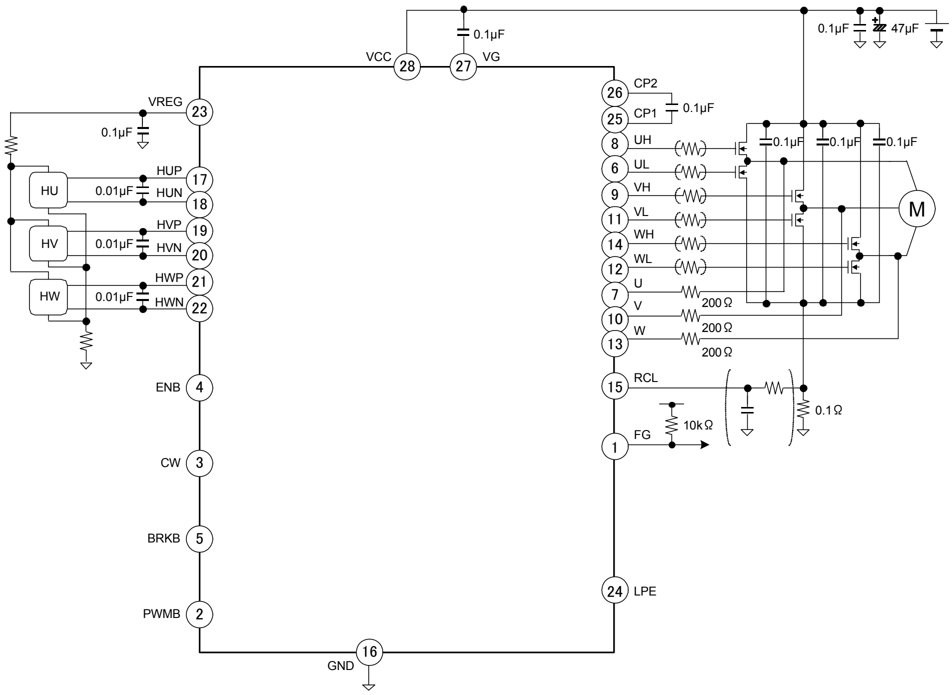


Figure 1. Application circuit

○Product structure：Silicon monolithic integrated circuit　○This product is not designed protection against radioactive rays

●**Pin Configuration**

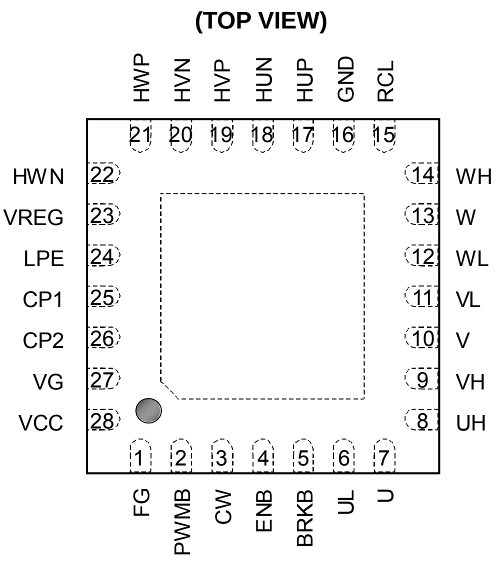


Figure 2. Pin configuration

●**Block Diagram**

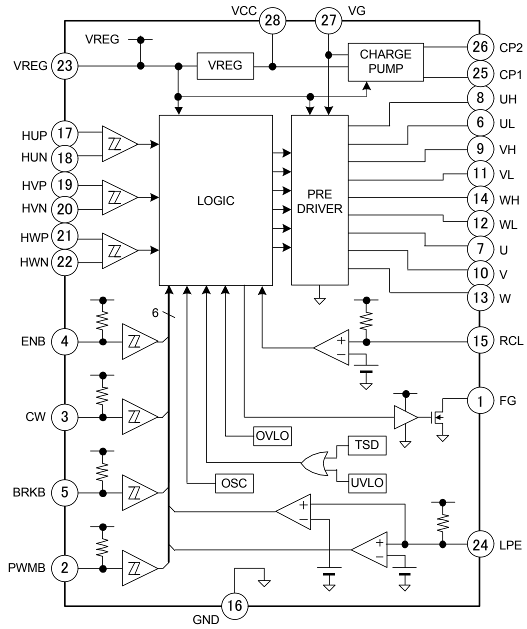


Figure 3. Block diagram

●**Pin Description**

Pin No.	Pin name	Function	Pin No.	Pin name	Function
1	FG	FG output	15	RCL	Detect voltage input for over current
2	PWMB	PWM input (negative logic)	16	GND	GND
3	CW	CW/CCW input (H:CW, L:CCW)	17	HUP	U phase Hall input＋
4	ENB	Enable (negative logic)	18	HUN	U phase Hall input－
5	BRKB	Brake input (negative logic)	19	HVP	V phase Hall input＋
6	UL	U phase lower output	20	HVN	V phase Hall input－
7	U	U phase output feedback	21	HWP	W phase Hall input＋
8	UH	U phase upper output	22	HWN	W phase Hall input－
9	VH	V phase upper output	23	VREG	VREG output (turn off at stand-by)
10	V	V phase output feedback	24	LPE	Setting about motor lock protection and OLVO (H/M/L input)
11	VL	V phase lower output	25	CP1	Charge pump setting 1
12	WL	W phase lower output	26	CP2	Charge pump setting 2
13	W	W phase output feedback	27	VG	Charge pump output
14	WH	W phase upper output	28	VCC	Power supply

●Description of operation

1) Commutation logic (120° commutation)

Truth table

HU	HV	HW	CW (CW=H or open)						CCW (CW=L)						FG
			UH	UL	VH	VL	WH	WL	UH	UL	VH	VL	WH	WL	
H	L	H	$\overline{PWM}$	PWM*	H	L	L	L	H	L	$\overline{PWM}$	PWM*	L	L	L
H	L	L	$\overline{PWM}$	PWM*	L	L	H	L	H	L	L	L	$\overline{PWM}$	PWM*	L
H	H	L	L	L	$\overline{PWM}$	PWM*	H	L	L	L	H	L	$\overline{PWM}$	PWM*	L
L	H	L	H	L	$\overline{PWM}$	PWM*	L	L	$\overline{PWM}$	PWM*	H	L	L	L	Hi-z
L	H	H	H	L	L	L	$\overline{PWM}$	PWM*	$\overline{PWM}$	PWM*	L	L	H	L	Hi-z
L	L	H	L	L	H	L	$\overline{PWM}$	PWM*	L	L	$\overline{PWM}$	PWM*	H	L	Hi-z
H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	Hi-z

* When PWMB=L，PWM="H"，When PWMB=H，PWM="L".

2) Enable input terminal (ENB)
Output of each phase can be set to ON/OFF (negative logic) through ENB terminal. When applied voltage is below V_{ENA}, the motor is driven (enable), when applied voltage is V_{STBY}, the motor suspends (stand-by). Stand-by mode has precedence to other control input signal, VREG output will be OFF. In addition, ENB terminal is pulled up by internal power supply through a resistance of 100kΩ(Typ)±30kΩ.

ENB	Operation
H or open	Stand-by
L	Enable

3) PWM input terminal (PWMB)
Speed can be controlled by inputting PWM signal into PWMB terminal (negative logic). Synchronous rectifier PWM can be realized through lower switching. When PWMB=" L", lower output that belongs to Hall input logic is “H”. When PWMB="H" or open, lower output is “L”. When PWMB="H" or OPEN status is detected 104μs(Typ), the synchronous rectifier will be OFF. Synchronous rectifier will be ON through rising and falling edges of subsequent PWMB. Additionally, PWMB terminal is pulled up by VREG through a resistance of 100kΩ(Typ)±30kΩ.

PWMB	Low side output
H or open	L
L	H

4) Brake input terminal (BRKB)
Motor rotation can be quickly stopped by BRKB terminal (negative logic). When BRKB="L", lower output will short brake all "H". When BRKB="H" or OPEN, then short brake action will be released. What’s more, BRKB terminal is pulled up by VREG through a resistance of 100kΩ(Typ)±30kΩ.

BRKB	Operation
H or open	Normal
L	Short brake

5) CW/CCW input terminal (CW)
Rotation direction can be switched with CW terminal. When CW="H" or OPEN, the direction is CW, when CW="L", the direction will be CCW. Though we do not recommend switching rotation direction when motor is rotating, if rotation direction is switched when rotating, the rotation speed will become hall frequency, which will be up to less than 40Hz and it will be switched to set rotation direction after the action short brake. And the CW terminal is pulled up by VREG through a resistance of 100kΩ(Typ)±30kΩ.

CW	Direction
H or open	CW
L	CCW

6) FG output
FG output is reshaped Hall U phase signal and output through FG terminal. It is not output in stand-by mode. In addition, because FG terminal is output from open drain, please use resistance of about 10kΩ ~ 100kΩ to pulled up from outside.

7) Hall input
Hall input amplifier is designed with hysteresis (±15mV(Typ) in order to prevent incorrect action due to noise inside. So please set bias current for Hall element to make amplitude of Hall input voltage over minimum input voltage ($V_{HALLMIN}$). Here, we recommend you to connect the ceramic capacitor with about 100pF ~ 0.01μF between difference input terminals of Hall amplifier. What's more, because the in-phase input voltage range (V_{HALLCM}, 0V ~ VREG-1.7V(Typ)) is designed for Hall input amplifier, so when bias to Hall element, please set within this range. When Hall inputs all become "H" or "L", detect circuit through Hall input abnormalities to make driver output all "L".

8) Booster circuit
There is built-in booster circuit used to drive upper Nch MOS transistor. VG terminals can produce a boost voltage (from the VCC voltage + 2×VF voltage (7V(Typ) reduced by internal regulator) through connecting capacitors between CP1-CP2 and between VG-VCC. We recommend connected condensers to be over 0.1μF. In addition, because there is built-in protection circuit for insufficient booster, when VG voltage is below V_{GUVON} (VCC+4V (Typ)), driver outputs will all be "L".

9) Current limit circuit (CL circuit)
Output current limit (Current limit: CL) circuit can be formed by connecting a low resistor used for testing current between RCL terminal & GND terminal. When RCL voltage is detected over 0.2V(Typ), lower output will all become "L". It (32μs(Typ)) resets automatically after a set amount of time. This action does not synchronize with the action that PWM signal is input into PWMB terminal. In addition, in order to avoid misdetection of output current due to RCL noise, the IC employs detection-masking period (1～2μsec(Typ)), during which current detection is disabled immediately after the output transistor is turned on.

10) Thermal Shut Down circuit (TSD circuit)
When chip temperature of driver IC rises and exceeds the set temperature (175°C(Typ)), the thermal shut down circuit (Thermal Shut Down: TSD) begins working. At this time, the driver outputs all become "L". In addition, the TSD circuit is designed with hysteresis (25°C(Typ)), therefore, when the chip temperature drops, it will return to normal working condition. Moreover, the purpose of the TSD circuit is to protect driver IC from thermal breakdown, therefore, temperature of this circuit will be over working temperature when it is started up. Thus, thermal design should have sufficient margin, so do not take continuous use and action of the circuit as precondition.

11) Under voltage lock out circuit (UVLO circuit)
There is a built-in under voltage lock out circuit (Under Voltage Lock Out: UVLO circuit) used to ensure the lowest power supply voltage for drive IC to work and to prevent error action of IC. When VCC voltage declined to V_{UVL} (6V (Typ)), all of the driver outputs should be "L". At the same time, UVLO circuit is designed with hysteresis (1V(Typ)), so when VCC voltage reaches more than V_{UVH} (7V(Typ)), it will enter normal working condition.

12) Over voltage lock out circuit (OVLO circuit)
There is built-in over voltage lock out circuit (Over Voltage Lock Out: OVLO circuit) used to restrain rise of VCC voltage when motor decelerating. When LPE terminal is at "M" and VCC voltage is over V_{OVH1} (16V(Typ)), and when LPE terminal is at "H" or "M" and VCC voltage of is over V_{OVH2} (28.5V(Typ)), a certain time (4ms(Typ)) of short brake action will be conducted. What's more, because OVLO circuit is designed with hysteresis (1V(Typ)), therefore, when V_{OVH1} is below V_{OVL1} (15V(Typ)) and when V_{OVH2} is below V_{OVL2} (27.5V(Typ)), it can return to normal working condition after a certain time of short brake action.

13) Motor Lock Protection circuit (MLP circuit)

There is built-in motor lock protection circuit (Motor Lock Protection: MLP), ON/OFF of MLP circuit and OVLO threshold can be set from LPE terminal. Monitor Hall signals, when the LPE = "H" or "M", if Hall signal logic does not change to 1.1sec(Typ), driver outputs will all be locked as "L". Latch can be released via standby status or through switching BRKB/CW logic. Moreover, when PWMB = "H" or open state is detected for about 15ms, latch can be released by rising and falling edges of subsequent PWMB. However, when LPE = "L", when short brake action (including switching rotation direction) enables or TSD circuit works, MLP circuit doesn't work. And LPE terminal is pulled up by VREG through a resistance of 50kΩ(Typ)±15 kΩ.

LPE	Monitoring time	OVLO threshold
H or open	1.1sec(Typ)±30%	V_{OVH2}, V_{OVL2}
M	1.1sec(Typ)±30%	V_{OVH1}, V_{OVL1}
L	Disable	V_{OVH2}, V_{OVL2}

14) Pre-driver output

Driving signal is output to external output power transistor through drive signal generated from internal logic output drive signal is output for external power supply transistor. Driving voltage of upper gate is VG voltage (Vcc+7V(Typ)) and driving voltage of lower gate is VREG voltage (5V(Typ)). In addition, a dead time (1μs(Typ)±30%) is designed between driving signals of upper gate and lower gate in order to prevent upper and lower FET from being set to ON synchronously when PWM is rectified synchronously. Due to the influence of the motor's counter electromotive force, the output feedback terminal might swing under GND potential. When excessive current occurs (about over 30mA), incorrect action or even damage might be caused. Therefore, please insert a resistor of about 100Ω ~ 510 Ω before putting into use. Moreover, we recommend you to use output feedback terminal with a slow rate of over 50ns.

15) Control signal sequence

Though we recommend you input control signals of ENB, CW, PWMB, BRKB and LPE terminals after inputting VCC, if input control signals before inputting VCC, there won't be any problem. If LPE terminal is set to "H" or "M" when being started, please be informed that if motor rotation cannot be detected within the set time (edge of FG signal cannot be input), then the MLP circuit starts and motor fails to start. Moreover, the order of priority is set to control signal and IC internal signal. Please refer to the following table.

Priority of control signal

Priority	Input / Internal signals
1st	ENB, UVLO
2nd	BRKB↑↓,CW↑↓,PWMB ↓
3rd	TSD, MLP, HALLERR
4th	OVLO
5th	VG_UVLO
6th	BRKB
7th	CL
8th	PWMB, CW

Note) ↑↓ means rising and falling edges of signal.
For signal name, please see state transition diagram.

●Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Limit	Unit
Power supply voltage	V_{CC}	-0.3 to +30.0(Note 1)	V
VG voltage	V_{G}	-0.3 to +38.0(Note 1)	V
Output voltage of pre-driver	$V_{(UH,VH,WH)}$	-0.3 to +38.0	V
	$V_{(UL,VL,WL)}$	-0.3 to +7.0	V
FG terminal voltage	V_{FG}	-0.3 to +7.0	V
RCL terminal voltage	V_{RCL}	-0.3 to +5.5	V
Voltage of input of control and Hall terminals	$V_{I/O}$	-0.3 to +5.5	V
Output current of pre-driver(DC)	$I_{OMAX(OUT)}$	±15(Note 1)	mA
FG output current	$I_{OMAX(FG)}$	5(Note 1)	mA
VREG output current	$I_{OMAX(VREG)}$	-30(Note 1)	mA
Operating temperature range	T_{OPR}	-40 to +85	°C
Storage temperature range	T_{STG}	-55 to +150	°C
Power dissipation	Pd	0.38(Note 2)	W
Junction temperature	T_{jmax}	150	°C

(Note 1) Do not exceed Pd..
(Note 2) Derate by 3.04mW/°C when operating above Ta=25°C (IC only).
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

●Recommended Operating Range (Ta=25°C)

Item	Symbol	Range	Unit
Power supply voltage	V_{CC}	8.0 to 26.4	V

●**Electrical Characteristic (Unless otherwise specified Ta=25°C, V_{CC}=24V)**

Item	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
[Whole]						
Circuit current	I_{CC}	-	2.5	5.0	mA	V_{ENB}=0V
Stand-by current	I_{STBY}	-	0.6	1.2	mA	ENB=OPEN
VREG voltage	V_{REG}	4.5	5.0	5.5	V	I_O=-10mA
[Booster circuit]						
VG voltage	V_G	V_{CC}+6	V_{CC}+7	V_{CC}+8	V	
VG UVLO voltage	V_{GUVON}	V_{CC}+3	V_{CC}+4	V_{CC}+5	V	
[Driver output]						
High side output voltage H	V_{OHH}	V_G-0.6	V_G-0.2	V_G	V	I_O=-5mA
High side output voltage L	V_{OHL}	0	0.2	0.6	V	I_O=5mA
Low side output voltage H	V_{OLH}	4.1	4.8	5.5	V	I_O=-5mA
Low side output voltage L	V_{OLL}	0	0.2	0.6	V	I_O=5mA
Source current of High side	$I_{HSOURCE}$	100	130	-	mA	Pulse width tw≦1usec
Sink current of High side	I_{HSINK}	50	65	-	mA	Pulse width tw≦1usec
Source current of Low side	$I_{LSOURCE}$	50	65	-	mA	Pulse width tw≦1usec
Sink current of Low side	I_{LSINK}	100	130	-	mA	Pulse width tw≦1usec
Dead Time	T_{DT}	0.7	1.0	1.3	μsec	
[Hall input]						
Input bias current	I_{HALL}	-2.0	-0.1	2.0	μA	V_{IN}=0V
Range of in-phase input voltage	V_{HALLCM}	0	-	V_{REG}-1.7	V	
Minimum input voltage	$V_{HALLMIN}$	50	-	-	mV_{p-p}	
HYS level ＋	$V_{HALLHY+}$	5	15	25	mV	
HYS level －	$V_{HALLHY-}$	-25	-15	-5	mV	
[Input of control：ENB]						
Input current	I_{ENB}	-75	-45	-25	μA	V_{ENB}=0V
Standby voltage	V_{STBY}	2.0	-	5.5	V	
Enable voltage	V_{ENA}	0	-	0.8	V	
[Input of control：PWMB, CW, BRKB]						
Input current	I_{IN}	-80	-50	-30	μA	V_{IN}=0V
Voltage input H	V_{INH}	2.0	-	5.5	V	
Voltage input L	V_{INL}	0	-	0.8	V	
Minimum input pulse width	t_{PLSMIN}	1	-	-	msec	CW, BRKB
Range of input frequency	F_{PWM}	10	-	50	kHz	PWMB
[Input of control：LPE]						
Input current	I_{LPE}	-160	-100	-60	μA	V_{LPE}=0V
Input voltage H	V_{LPH}	0.8×V_{REG}	-	V_{REG}	V	
Input voltage M	V_{LPM}	0.4×V_{REG}	-	0.6×V_{REG}	V	
Input voltage L	V_{LPL}	0	-	0.2×V_{REG}	V	
[FG output]						
Output voltage L	V_{FGOL}	0	0.1	0.3	V	I_O=2mA
Leak current	I_{FGLEAK}	-	0	1	μA	V_{FG}=5V
[Current limit]						
Detect voltage	V_{CL}	0.18	0.20	0.22	V	
Input bias current	I_{RCL}	-32	-20	-12	μA	V_{RCL}=0V
Range of input voltage	V_{RCL}	-0.3	-	1.0	V	

●**Electrical Characteristic (Unless otherwise specified Ta=25°C, V_{CC}=24V)**

Item	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
[UVLO]						
Release voltage	V_{UVH}	6.5	7.0	7.5	V	
Lock out voltage	V_{UVL}	5.5	6.0	6.5	V	
[OVLO]						
Release voltage1	V_{OVL1}	14.0	15.0	16.0	V	LPE="M"
Lock out voltage1	V_{OVH1}	15.0	16.0	17.0	V	LPE="M"
Release voltage2	V_{OVL2}	26.5	27.5	28.5	V	LPE="H" or "L"
Lock out voltage2	V_{OVH2}	27.5	28.5	29.5	V	LPE="H" or "L"
[MLP]						
Motor lock protection detect time	T_{LPE}	0.77	1.10	1.43	sec	LPE="H" or "M"

●**Reference Data (Unless otherwise specified V_{CC}=24V)**

Item	Symbol	Reference			Unit	Condition
		Min	Typ	Max		
[Current limit]						
Mask time	T_{CLMASK}	0.7	-	2.6	μsec	Ta=25°C
[Protect]						
TSD ON temperature	T_{TSDON}	150	175	200	°C	Junction temperature (Tj)
TSD Hysteresis	T_{TSDHTS}	15	25	35	°C	Junction temperature (Tj)

Above-Data for reference, not under guaranteed.

Typical Performance Curves (Reference Data)

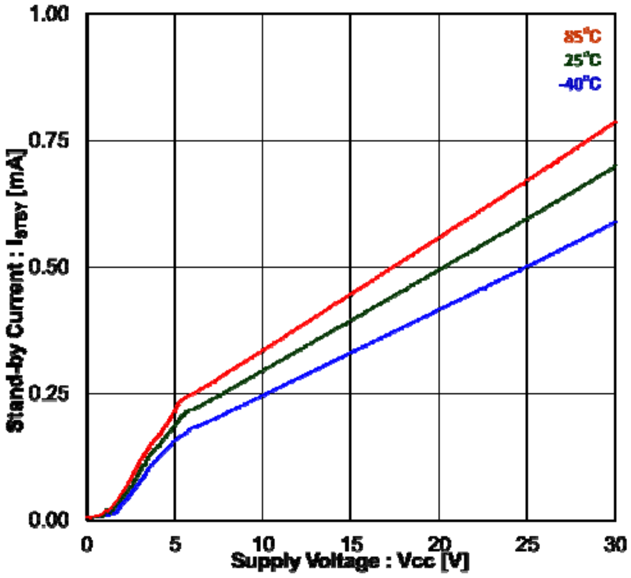


Figure 4. Stand-by Current vs Supply Voltage
(Stand-by Current)

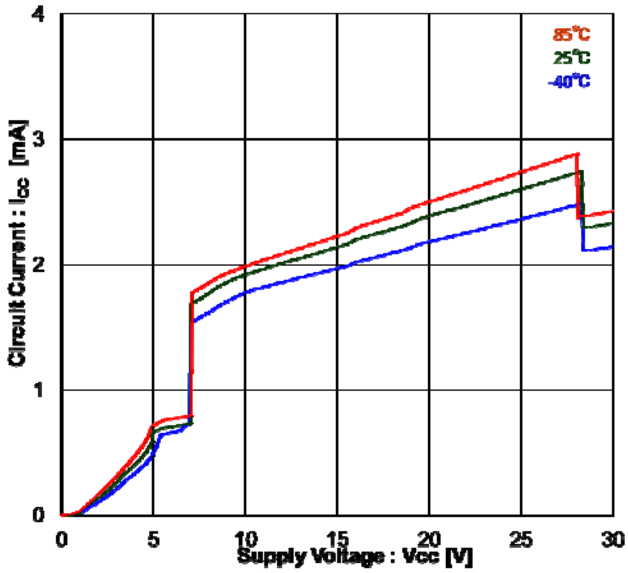


Figure 5. Circuit Current vs Supply Voltage
(Circuit Current)

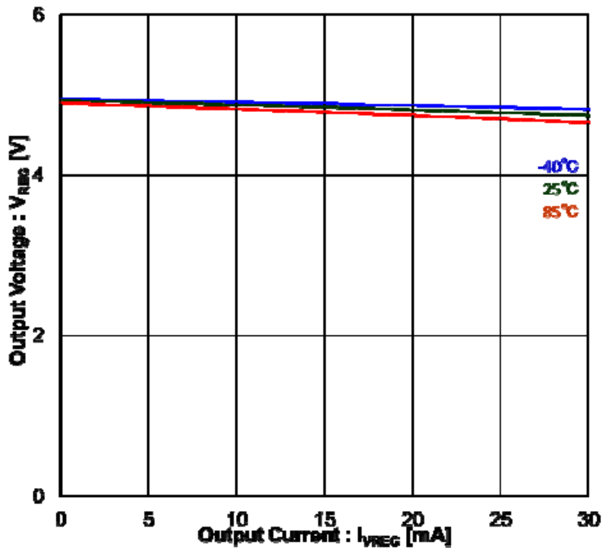


Figure 6. Output Voltage vs Output Current
(VREG Voltage)

Typical Performance Curves (Reference Data) - continued

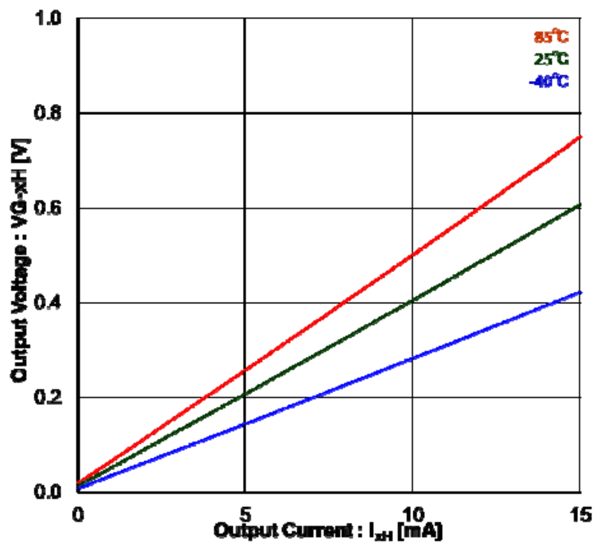


Figure 7. Output Voltage vs Output Current
(High side Output voltage H)

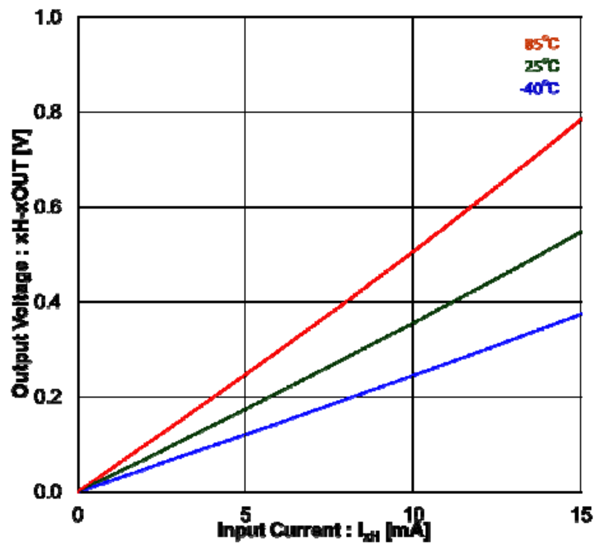


Figure 8. Output Voltage vs Output Current
(High side Output voltage L)

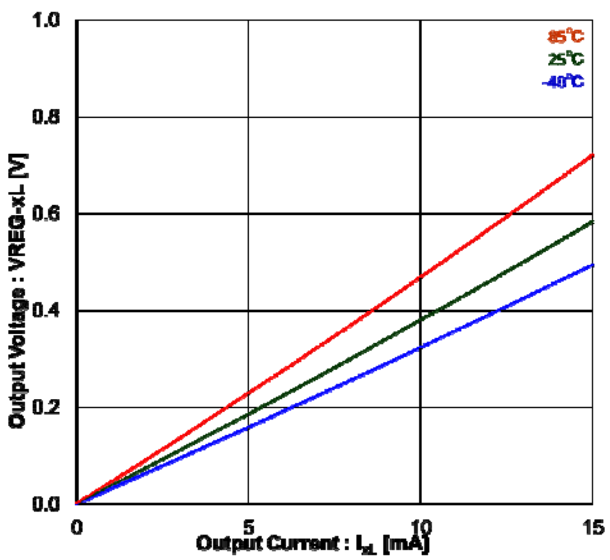


Figure 9. Output Voltage vs Output Current
(Low side Output voltage H)

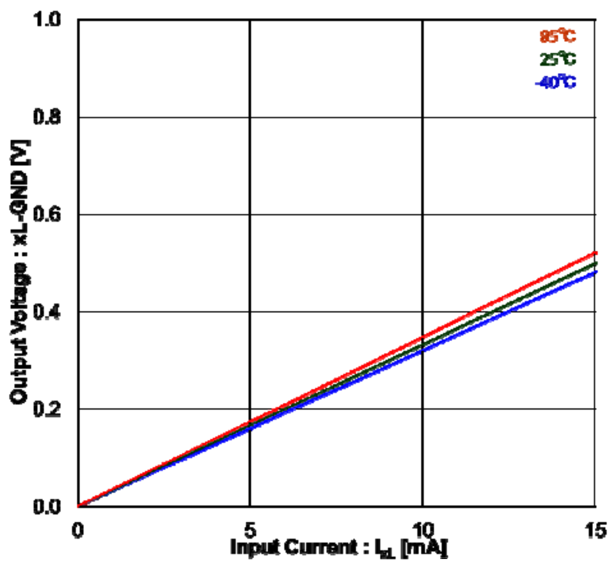


Figure 10. Output Voltage vs Output Current
(Low side Output voltage L)

Typical Performance Curves (Reference Data) - continued

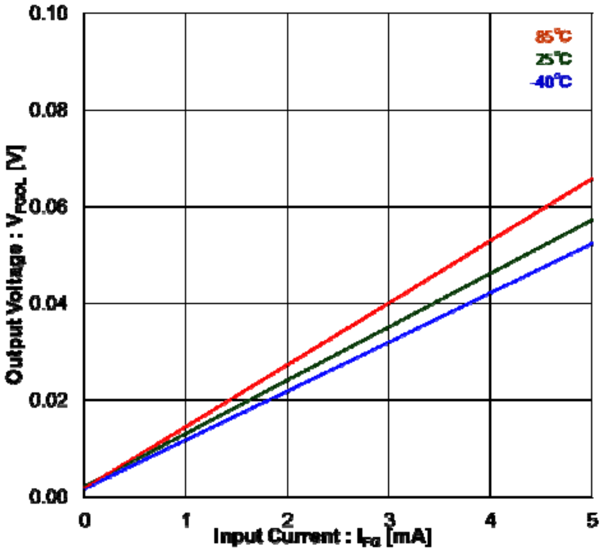


Figure 11. Output Voltage vs Input Current
(FG Output Voltage L)

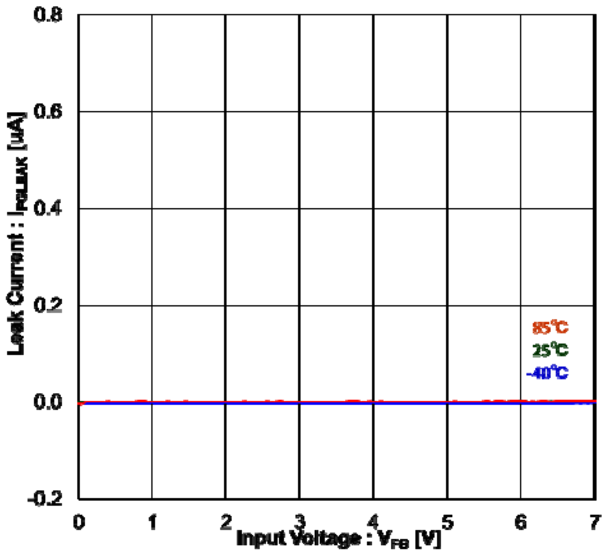


Figure 12. Leak Current vs Input Voltage
(FG Leak Current)

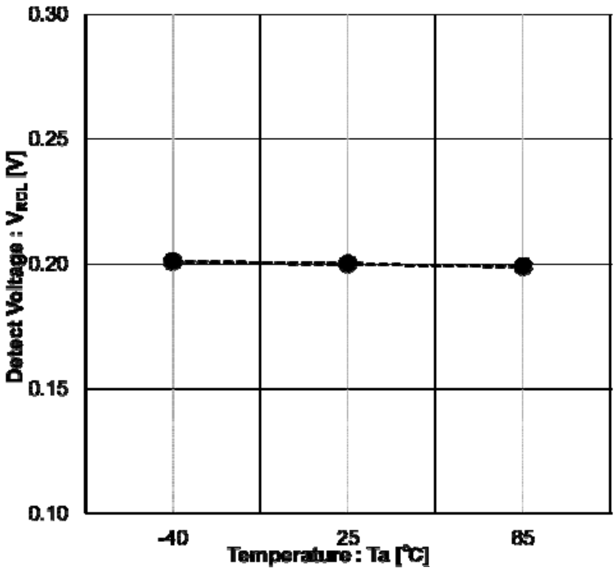


Figure 13.Detect Voltage vs Temperature
(CL Detect Voltage)

Typical Performance Curves (Reference Data) - continued

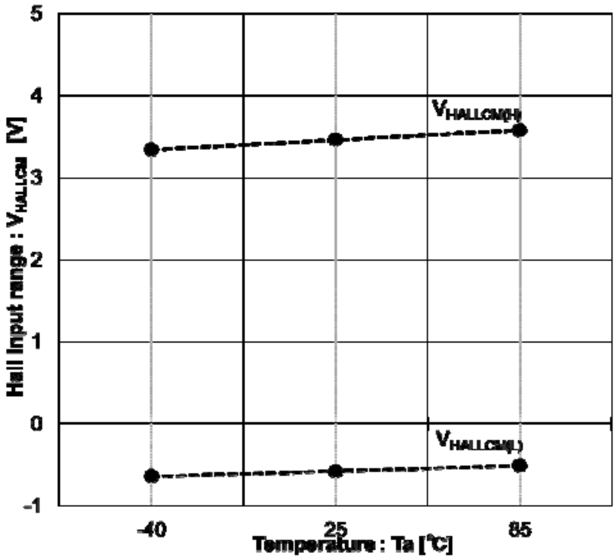


Figure 14. Input Range vs Temperature
(Range of in-phase input voltage for Hall input)

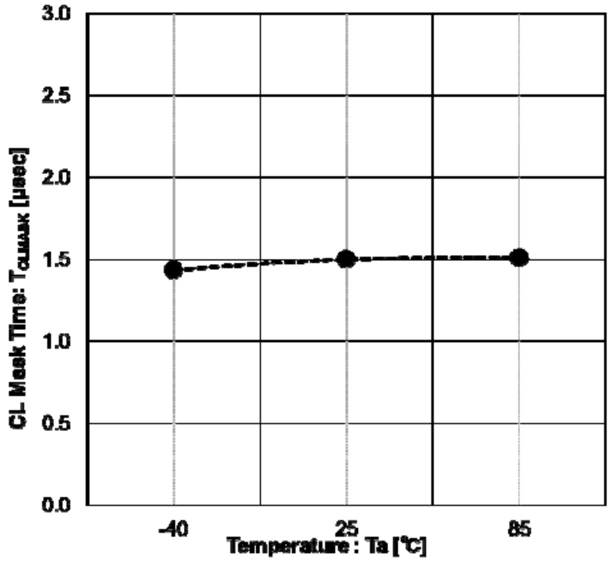


Figure 15. CL Mask Time vs Temperature
(Current Limit Mask time)

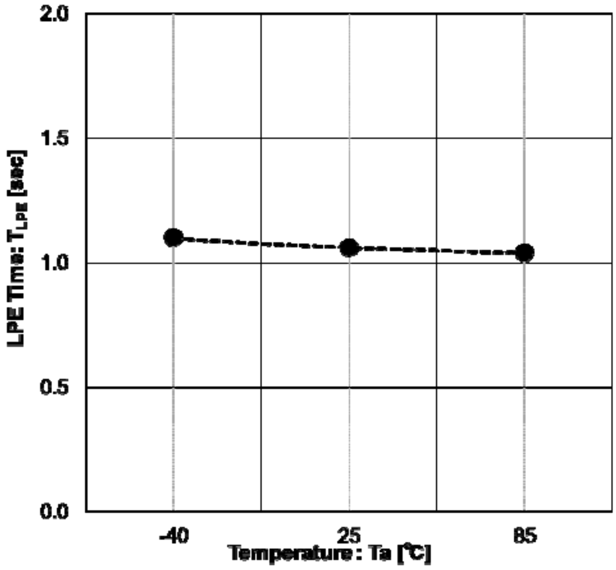
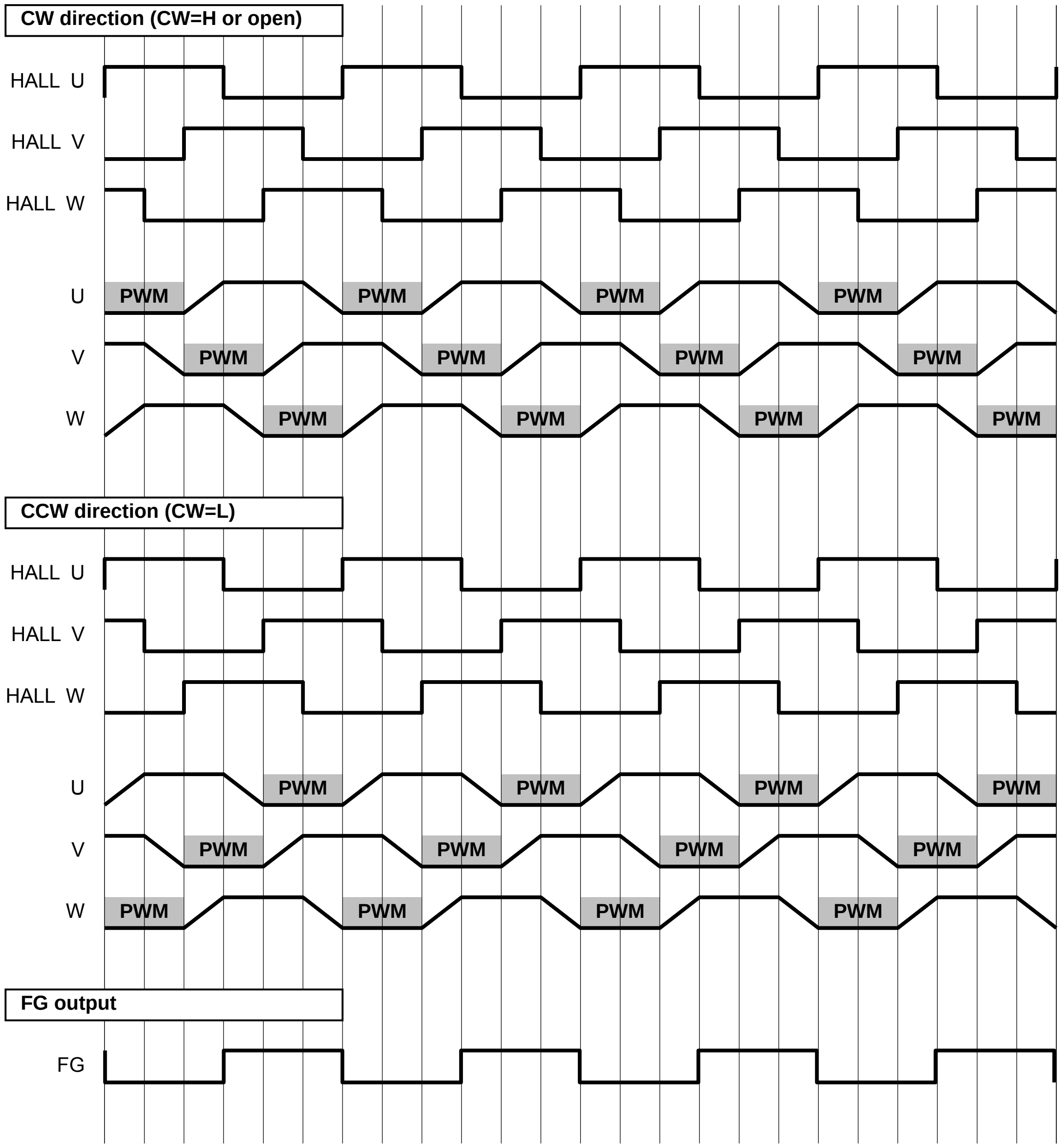
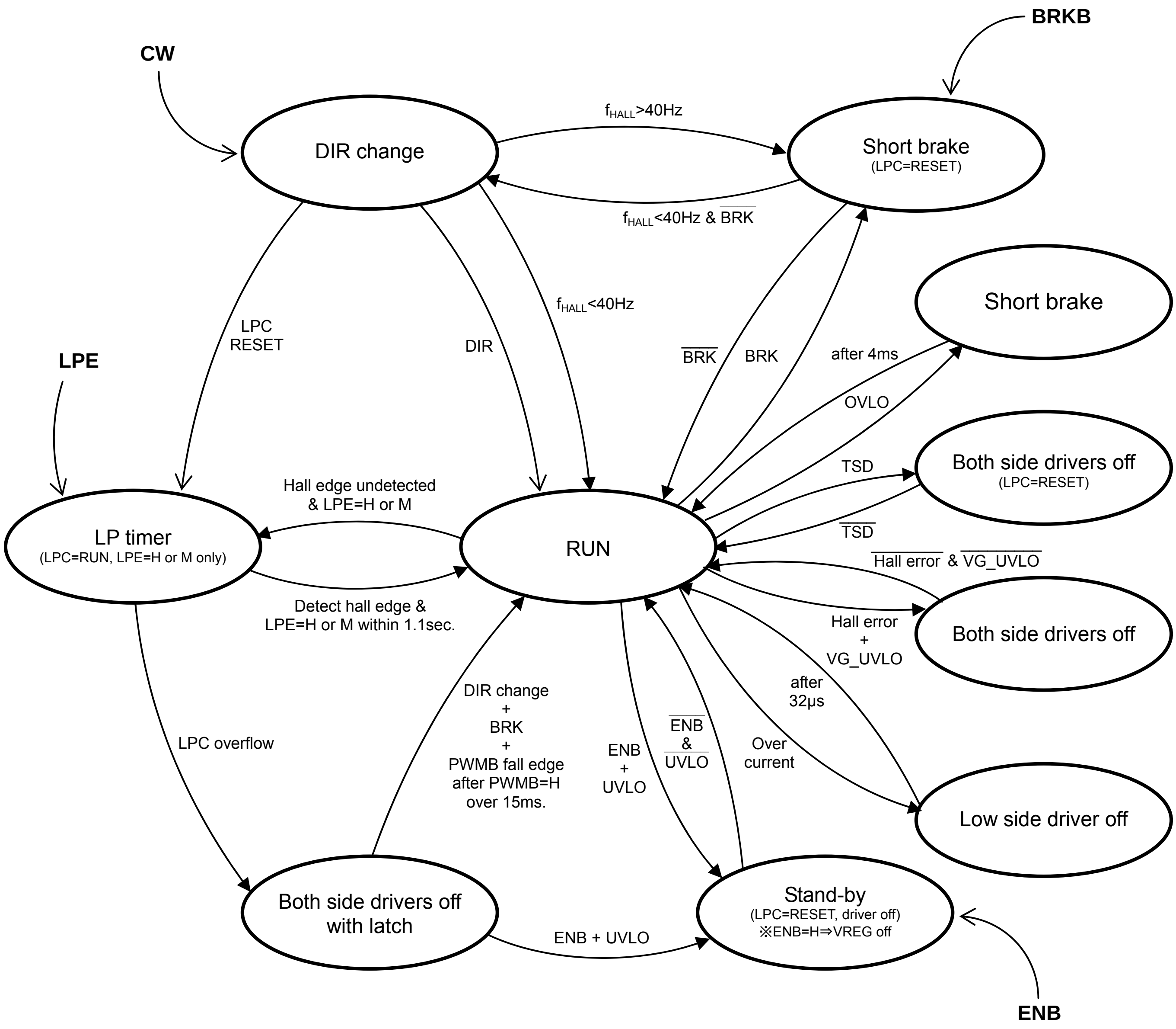


Figure 16. LPE Time vs Temperature
(Detect Time of Motor Lock Protection)

●**Timing Chart**



●State transition diagram



Legend:

DIR: motor rotational direction
LP: motor lock protection
LPC: internal counter for the motor lock protection (watch-dog timer)
f_{HALL}: hall signal frequency
Hall error: HU=HV=HW
&: logical "AND"
+: logical "OR"

Note) All values are typical.

●I/O equivalence circuits

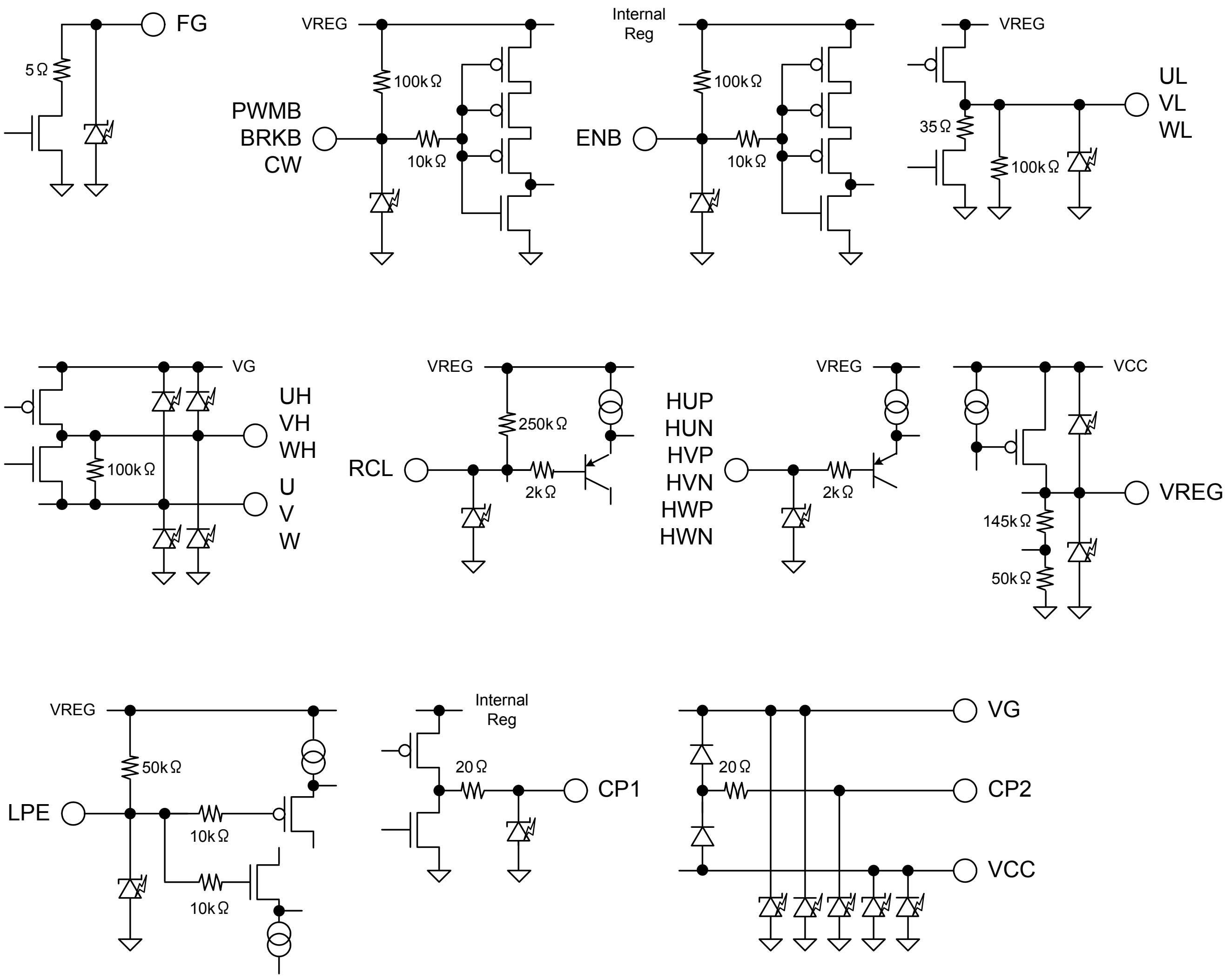


Figure 17. I/O equivalence circuits

●Power Dissipation

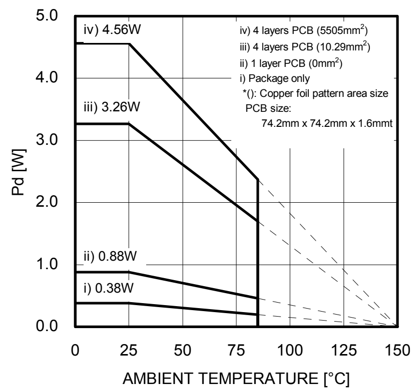


Figure 18. Derating curve
(VQFN028V5050)

Package thermal resistor

Board	$\theta_{j\text{-}a}$ [°C/W]
Board (4)	27.4
Board (3)	38.3
Board (2)	142.0
Board (1)	328.9

Note） Values about heat reducing curve and packaged thermal resistor are tested values.

Operational Notes

1. **Reverse Connection of Power Supply**
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
Except for pins the output and the input of which were designed to go below ground, ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. **Unused Input Pins**
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. **Regarding the Input Pin of the IC**
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

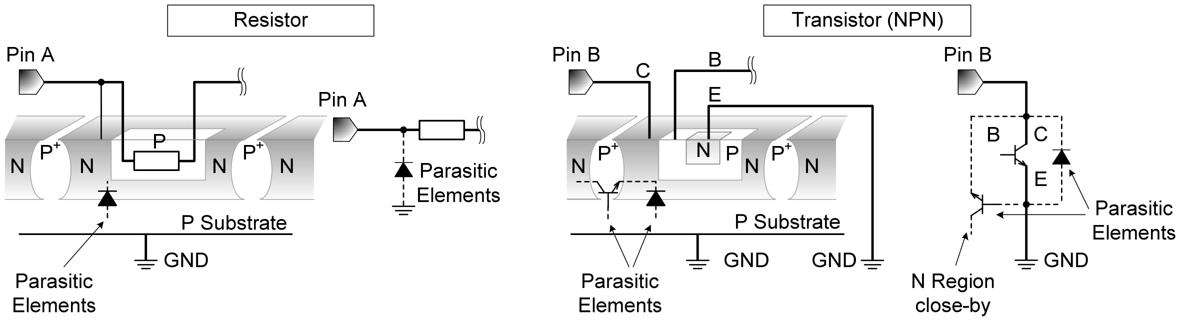


Figure 19. Example of monolithic IC structure

13. **Ceramic Capacitor**
When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. **Thermal Shutdown Circuit(TSD)**
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

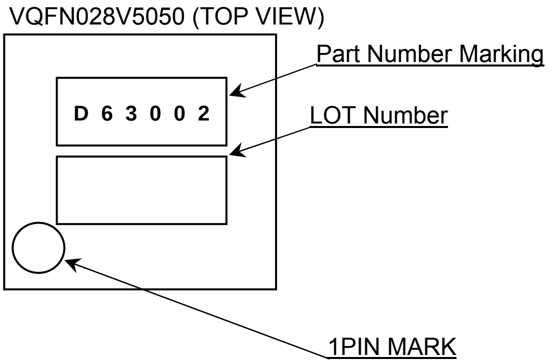
15. **Metal on the backside (Define the side where product markings are printed as front)**
The metal on the backside is shorted with the backside of IC chip therefore it should be connected to GND. Be aware that here is a possibility of malfunction or destruction if it is shorted with any potential other than GND.

●Ordering Information

B	D	6	3	0	0	2	M	U	V	-	E	2

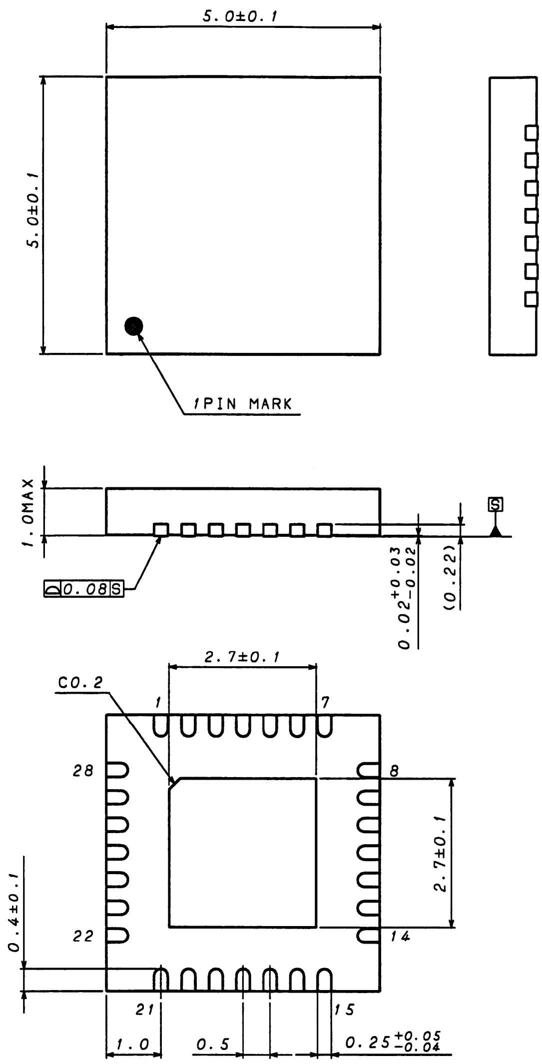
- Part Number: BD63002
- Package: MUV: VQFN028V5050
- Packaging and forming specification: E2: Embossed tape and reel

●Marking Diagram



●Physical Dimension Tape and Reel Information

Package Name	VQFN028V5050

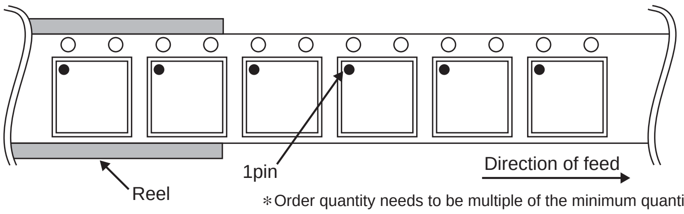


(UNIT:mm)

PKG:VQFN028V5050
Drawing No.EX473-5002-2

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

●Revision History

Date	Revision	Changes
25.Feb.2015	001	New Release
3.Jul.2015	002	Add Electrical Characteristics and Typical Performance Curves

Notice

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

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BD63002MUV - Web Page

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Distribution Inventory

Part Number	BD63002MUV
Package	VQFN028V5050
Unit Quantity	2500
Minimum Package Quantity	2500
Packing Type	Taping
Constitution Materials List	inquiry
RoHS	Yes