

STRUCTURE Silicon Monolithic Integrated Circuit

NAME OF PRODUCT DC-AC Inverter Control IC

TYPE **BD9240F / BD9240FV**

FUNCTION

- 20V High voltage process
- 2CH control with Push-Pull
- Lamp current and voltage sense feed back control
- Sequencing easily achieved with Soft Start Control
- Short circuit protection with Timer Latch
- Under Voltage Lock Out
- Mode-selectable the operating or stand-by mode by stand-by pin
- Automatic Judge function for External synchronization of lamp oscillation
- BURST mode controlled by PWM and DC input

○ Absolute Maximum Ratings (T_a = 25°C)

Parameter	Symbol	Limits	Unit
Supply Voltage	VCC	20	V
Operating Temperature Range	Topr	-40~+85	°C
Storage Temperature Range	Tstg	-55~+150	°C
Maximum Junction Temperature	Tjmax	+150	°C
Power Dissipation	Pd	*1 1063 (BD9240FV)	mW
		*2 750 (BD9240F)	

*1Pd derate at 8.5mW/°C for temperature above Ta = 25°C (When mounted on a PCB 70.0mm×70.0mm×1.6mm)

*2Pd derate at 6.0mW/°C for temperature above Ta = 25°C (When mounted on a PCB 70.0mm×70.0mm×1.6mm)

○ Operating condition

Parameter	Symbol	Limits	Unit
Supply voltage	VCC	8.0 ~ 19.0	V
oscillation frequency	FOUT	30 ~ 90	kHz
BCT oscillation frequency	FBCT	0.05 ~ 1.00	kHz

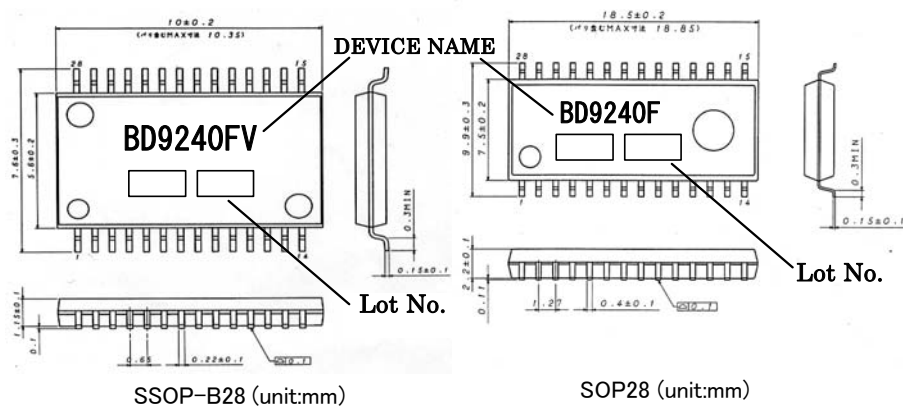
○ Electric Characteristics (Ta=25°C, VCC=12V)

Parameter	Symbol	Limits			Unit	Conditions
		MIN.	TYP.	MAX.		
((WHOLE DEVICE))						
Operating current	Icc1	—	6.2	12.0	mA	FOUT=60kHz, FB=GND
Stand-by current	Icc2	—	21	60	uA	
((STAND BY CONTROL))						
Stand-by voltage H 1	Vsth1	VCCx0.85	—	VCC	V	System ON (DUTY 2ch input mode)
Stand-by voltage H 2	Vsth2	2	—	VCCx0.5	V	System ON (DUTY 1ch input mode)
Stand-by voltage L	VstL	-0.3	—	0.8	V	System OFF
((UVLO BLOCK))						
Operating voltage (VCC)	Vuvlo	6.65	7.00	7.35	V	
Hysteresis width (VCC)	ΔVuvlo	0.37	0.50	0.63	v	
Operating voltage (UVLO)	Vvlo_u	2.4	2.5	2.6	V	
Hysteresis width (UVLO)	ΔVvlo_u	0.075	0.100	0.125	V	
((SOFT START BLOCK))						
Soft start current	Iss	1.5	2.0	2.5	uA	
SS_COMP detect voltage	Vss	2.3	2.5	2.7	V	
((OSC BLOCK))						
RT Output Voltage	VRT	1.05	1.50	1.95	V	
STR ON Resistor value	RSRT	—	100	200	Ω	
((BOSC BLOCK))						
BOSC Max voltage	VBCTH	1.94	2.00	2.06	V	fBCT=0.3kHz
BOSC Min voltage	VBCTL	0.40	0.50	0.60	V	fBCT=0.3kHz
BOSC constant current	IBCT	1.35/BRT	1.50/BRT	1.65/BRT	A	
BOSC frequency	FBCT	291	300	309	Hz	(BRT=36.2kΩ, BCT=0.047uF)
((FEED BACK BLOCK))						
IS threshold voltage 1	Vis1	1.225	1.250	1.275	V	
IS threshold voltage 2	Vis2	—	VREFIN	VIS1	V	VREF applying voltage
VS threshold voltage	Vvs	1.220	1.250	1.280	V	
IS source current 1	Iis1	—	—	0.9	uA	DUTY=2.0V
IS source current 2	Iis2	40	50	60	uA	DUTY=0V, IS=1.0V
VS source current	Ivs	—	—	0.9	uA	
IS COMP detect voltage 1	VISCOMP1	0.64	0.66	0.68	V	VREFIN ≥ 1.25V
IS COMP detect voltage 2	VISCOMP2	—	0.5	—	V	VREFIN=1V
VREF input voltage range	VREFIN	0.6	—	1.6	V	No effect at VREF>1.25V
((OUTPUT BLOCK))						
NA output voltage H	VoutAH	VCC-0.3	VCC-0.1	—	V	
NB output voltage H	VoutBH	VCC-0.3	VCC-0.1	—	V	
NA output voltage L	VoutAL	—	0.1	0.3	V	
NB output voltage L	VoutBL	—	0.1	0.3	V	
NA output sink resistance	Rsink_NA	1.3	2.5	5.0	Ω	
NA output source resistance	Rsource_NA	4.0	8.0	16.0	Ω	
NB output sink resistance	Rsink_NB	1.3	2.5	5.0	Ω	
NB output source resistance	Rsource_NB	4.0	8.0	16.0	Ω	
Drive output frequency	Fout	57.9	60.0	62.1	kHz	RT=21kΩ
((GT SYNCHRONOUS BLOCK : CLKIN pin))						
Input High voltage range	VCT_CLKIN_H	2.5	—	5.0	V	
Input Low voltage range	VCT_CLKIN_L	-0.3	—	0.5	V	

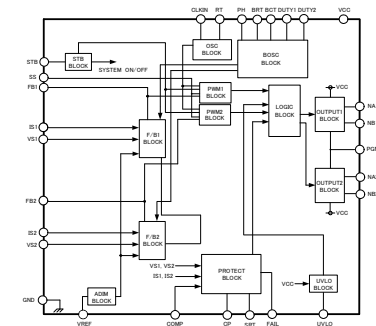
((FAIL BLOCK : FAIL pin))						
FAIL High voltage	VFAIL_H	2.95	3.1	3.25	V	
FAIL Low voltage	VFAIL_L	-0.3	-	0.5	V	
((TIMER LATCH BLOCK : CP pin))						
CP timer latch detect voltage	VCP	1.91	2.00	2.09	V	
CP timer latch charge current	ICP	0.85	1.05	1.25	uA	
((COMP BLOCK))						
COMP over voltage detect voltage	VCOMP	3.88	4.00	4.12	V	VSS > 2.4V
Hysteresis width (COMP)	ΔV_{comp}	0.138	0.185	0.232	V	
((PHASE SHIFT BLOCK))						
PH voltage H 1	VphH1	VCCx0.85	-	VCC	V	PHASESHIFT MODE1
PH voltage H 2	VphH2	2	-	VCCx0.5	V	PHASESHIFT MODE2
PH voltage L	VphL	-0.3	-	0.8	V	PHASESHIFT MODE3

(This product is not designed to be radiation-resistant.)

OPackage Dimensions



OBlock Diagram



OPin Description

PIN No.	PIN NAME	FUNCTION	PIN No.	PIN NAME	FUNCTION
1	PGND	Power Ground for FET drivers	15	CP	External capacitor between CP and GND for timer latch
2	NA2	NMOS FET driver (Channel 2 side)	16	FAIL	Error Indication output pin Normal : H, Error : L
3	NB2	NMOS FET driver (Channel 2 side)	17	PH	Selector pin for phase shift
4	UVLO	Input of Under Voltage Lock Out	18	VS2	Error amplifier input 1 (Channel 2)
5	CLKIN	CT Synchronous signal input	19	IS2	Error amplifier input 2 (Channel 2)
6	SRT	External resistor between SRT and RT for adjustment frequency of kick-off	20	FB2	Error amplifier output (Channel 2)
7	RT	External resistor between RT and GND for adjustment frequency of saw tooth wave	21	VS1	Error amplifier input 1 (Channel 1)
8	GND	Ground	22	IS1	Error amplifier input 2 (Channel 1)
9	BCT	External capacitor between BCT and GND for adjusting the BURST triangle oscillator	23	FB1	Error amplifier output (Channel 1)
10	BRT	External resistor between BRT and GND for adjustment frequency of Burst dimming	24	SS	External capacitor between SS and GND for Soft Start Control and detect the time of Soft Start
11	VREF	Reference voltage input pin for Error amplifier	25	COMP	Input of over voltage detector
12	DUTY1	Control Burst-dimming by PWM signal or DC (Channel 1)	26	VCC	Power supply input with UVLO Protection
13	DUTY2	Control Burst-dimming by PWM signal or DC (Channel 2)	27	NB1	NMOS FET driver (Channel 1 side)
14	STB	Stand-by switch	28	NA1	NMOS FET driver (Channel 1 side)

ONOTE FOR USE

1. This product is produced with strict quality control, but might be destroyed if used beyond its absolute maximum ratings. Once IC is destroyed, failure mode will be difficult to determine, like short mode or open mode. Therefore, physical protection countermeasure, like fuse is recommended in case operating conditions go beyond the expected absolute maximum ratings.
2. The circuit functionality is guaranteed within of ambient temperature operation range as long as it is within recommended operating range. The standard electrical characteristic values cannot be guaranteed at other voltages in the operating ranges, however the variation will be small.
3. Mounting failures, such as misdirection or miscounts, may harm the device.
4. A strong electromagnetic field may cause the IC to malfunction.
5. The GND pin should be the location within $\pm 0.3V$ compared with the PGND pin.
6. BD9240F/FV incorporate a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation of the thermal shutdown circuit is assumed.
7. Absolute maximum ratings are those values that, if exceeded, may cause the life of a device to become significantly shortened. Moreover, the exact failure mode caused by short or open is not defined. Physical countermeasures, such as a fuse, need to be considered when using a device beyond its maximum ratings.
8. About the external FET, the parasitic Capacitor may cause the gate voltage to change, when the drain voltage is switching. Make sure to leave adequate margin for this IC variation.
9. Under operating CP charge (under error mode) analog dimming and burst dimming are not operate.
10. By STB and PH voltage, BD9240F/FV are changed to 3 states. Therefore, do not input STB and PH pin voltage between one state and the other state (0.8~2.0V, $VCC \times 0.5 \sim VCC \times 0.85$ V)
11. By the DUTY1 pin for setting of Burst dimming Mode, When Burst dimming by DC signal do not input DUTY1 voltage between one state and the other state (0.485~0.515V, 1.985~2.015V)
When Burst dimming by PWM signal, set ON time and OFF time of the input PWM pulse signal to more than 30us (Dimming of 0% and Dimming of 100% are no problem)
12. The pin connected a connector need to connect to the resistor for electrical surge destruction.
13. This IC is a monolithic IC which (as shown is Fig.1)has P⁺ substrate and between the various pins. A P-N junction is formed from this P layer of each pin. For example, the relation between each potential is as follows.
○(When GND > PinB and GND > PinA, the P-N junction operates as a parasitic diode.)
○(When PinB > GND > PinA, the P-N junction operates as a parasitic transistor.)
Parasitic diodes can occur inevitably in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits as well as operation faults and physical damage. Accordingly you must not use methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin.

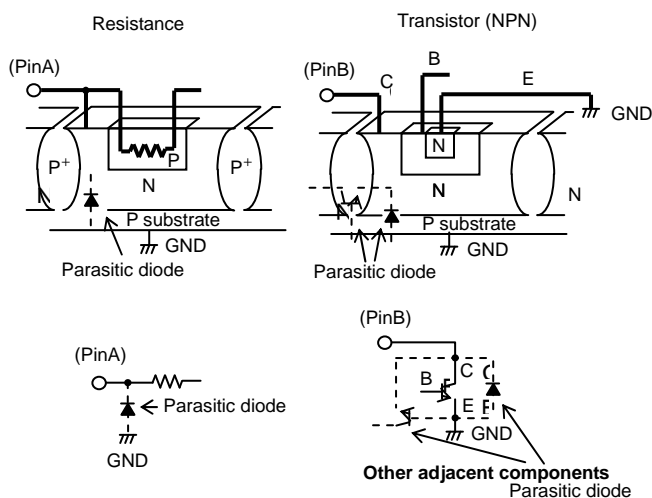


Fig.1 Simplified structure of a Bipolar IC

Notes

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