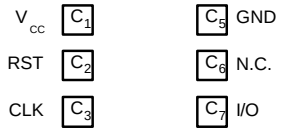
BL7430EC 104-bit EEPROM Smart Counter Circuit

Description

BL7430EC is a IC Card chip (module)made by 1.2μmCMOS EERPOM process. It has 104 bits EEPROM with logical encryption and function. It can be widely used in payphone Card and other kinds of prepay IC Cards.

Pin assignment



Features

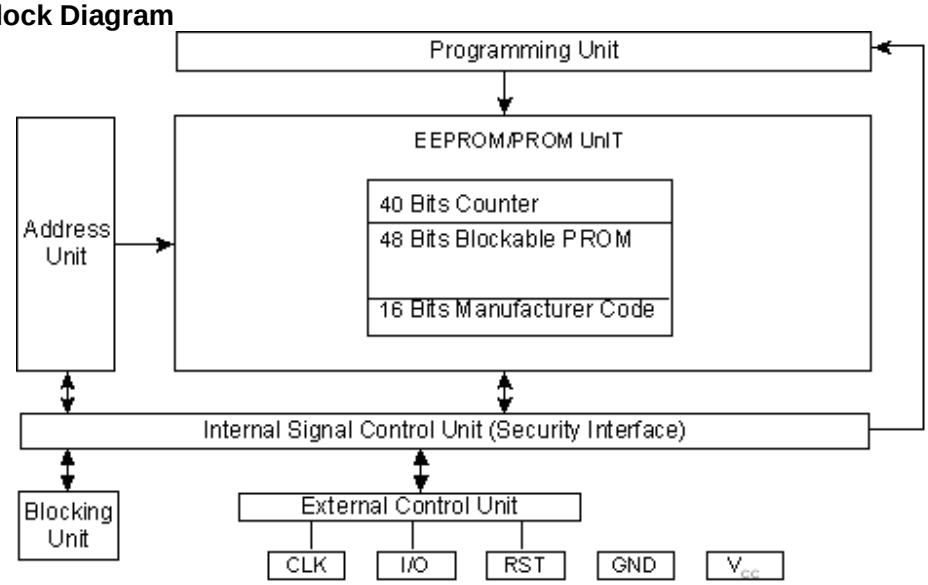
- 104 x 1 bit organization
- Maximum of 20480 counting units
- Logical encryption
- EEPROM programming time :5ms
- Supply voltage:5V
- Working current:<1mA
- Minimum erasing times 100,000
- Data retention time :>10 years
- Contacts configuration and serial interface according to ISO 7816 standard (synchronous transmission)

Pin Description

Pin No.	Parameter	Symbol	Test Condition
1	C1	V_{CC}	Supply Voltage
2	C2	RST	Control input (reset signal)
3	C3	CLK	Clock input
4	C5	GND	Ground
5	C6	N.C.	Not connected
6	C7	I/O	Bidirectional data line (open drain)

Function Description

- **Block Diagram**

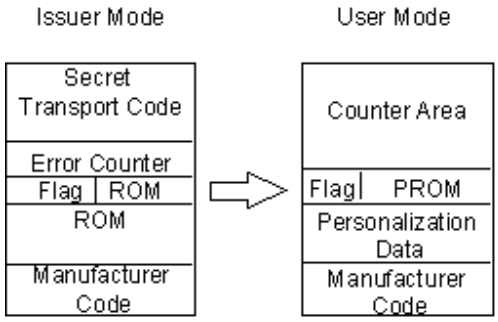


BL7430EC circuits consists of 104 bits EEPROM. The whole storing area is divided into three areas according to different usage.

- **Organization of Memory**

Pin No.	Address	Memory Type	Function
1	0~15	ROM	Manufacturer code
2	16~63	PROM	Card Data
3	64	PROM	Control flag
	65~71	PROM	Uppermost non-erasable counter stage; up to 3 bits(69~71) already canedled by testing upon delivery
	72~103	EEPROM	Count range

Mentioned above is the user mode after card being personalized. When chips are transferred to card-manufacturer, they are in issue mode, after being personalized, then changed to user mode. The differences between issue mode and user mode are presented on the right figure.



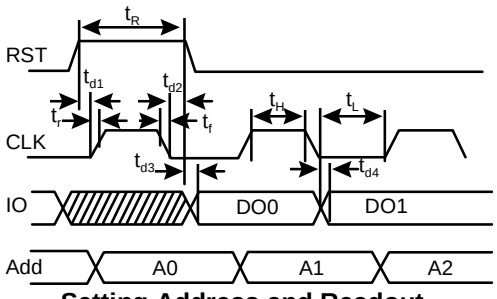
- **Counting Method**

The counting area consists of 36 bits EEPROM. The structure of counter is 5-stage with 8 bits , each stage like an abcus, but the highest stage has only 4 bits, the counting scope is 20480,while counting, the first stage is erased after writing any bit of the second counting stage, all do like this, then the fourth counting stage is erased after writing any bit of the fifth stage. But the fifth counting stage can be erased, so the contents of counting cells are continuously reduced to zero. In one counting stage, if the writable numbers more than the number which should be written, this can be operated without any problem. If the writable number is less than the number should be written, we can do like this: first write each writable number of this stage, then we write on bit of higher stage and erase 8 bits of current stage. Thus we can write the remaining number in current stage.

- **Reading/Writing operation**

Reading operation

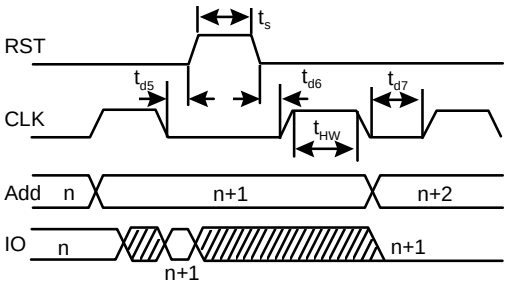
Internal address-counter works following bit clock, at the clock rising edge and RST is low ,the address-counter add 1 after the clock falling edge, the content of the relative address is output to I/O port. Both CLK and RST are high , the address-counter is reset to 0.



Setting Address and Readout

Writing operation

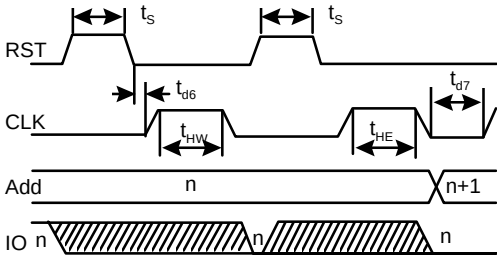
When RST=1 and CLK=0, we set R mark, under this condition if next clock pulse comes the address-counter will not increase and go into writing operation during the clock high level. The address-counter is re-effective and writing is finished at the clock falling edge. During the issue mode, R mark is useless to the cells of manufacturer code area; during the user mode, R mark is useless to the cells of code area for both manufacturer and issuer.



Write Address

Erasing operation

Erasing operation to any stage will lead to the automatic erasing of next lower stage.



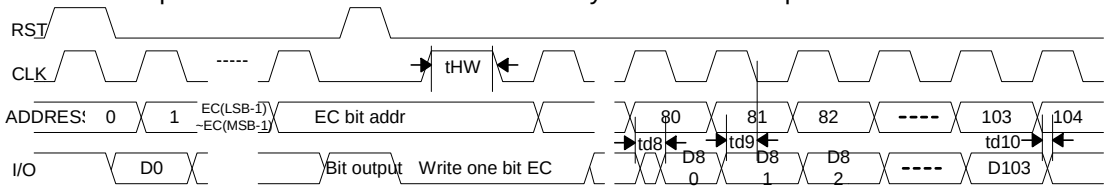
Erasing 8 Bits with Carry

Power on and reset

The address is reset after power on. RST keep"1" and must last longer than one clock cycle. When RST is changed to low level, the content in the "0" address is shown on I/O port. The unstability of V_{CC} also can induce the address reset .

About Comparison of Transmission Password

Password comparison must be executed immediately after write "0" operation



- **Package**

Module package, the module type according to customer demand.

Electrical Parameter

- **Absolute Maximum Ratings**

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	Max		
Supply voltage	V_{CC}	-0.3		6.0	V	
Input voltage (any pin)	V_I	-0.3		6.0	V	
Storage temperature	T_S	-40		125	℃	
ESD protection	Vs	4000			V	ISO/IEC 7816-1
Endurance		10^5			Write/erase cycles/bit	
Data retention		10			Years	

- **Operation Range**

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	Max		
Supply voltage	V_{CC}	4.75	5.0	5.5	V	
Supply current	I_{CC}			3.0	mA	V_{CC}=5V
Ambient temperature	Ta	-35		+80	℃	

- **DC characteristics**

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	Max		
High-level input voltage (I/O,CLK,RST)	V_{IN}	3.5		V_{CC}	V	
Low-level input voltage (I/O,CLK,RST)	V_{IL}			0.8	V	
Low-level output current(I/O)	I_{OL}			1	mA	V_{OL} =0.5V,open drain
High-level output current(I/O)	I_{OL}			10	μA	V_{OH} =0.5V,open drain

- **AC characteristics**

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	Max		
RST(address reset)	t_R	50			μs	
RST(set R-flag)	t_s	10			μs	
CLK (count,H-level)	t_H	10			μs	
CLK (count,L-level)	t_L	10			μs	
CLK (write,H-level)	t_{HW}	5			ms	
CLK (erase,H-level)	t_{HE}	5			ms	
Delay time	t_{d1}	5			μs	
	t_{d2}	5			μs	
	t_{d3}	5			μs	
	t_{d4}	3.5			μs	
	t_{d5}	5			μs	
	t_{d6}	5			μs	
	t_{d7}	10			μs	
	t_{d8}	3.5			μs	
	t_{d9}	3.5			μs	
	t_{d10}	3.5			μs	