



Ultra Low Power/Voltage CMOS SRAM 512K X 16 bit

BS616UV8011

■ FEATURES

- Ultra low operation voltage : 1.8 ~ 2.3V
- Ultra low power consumption :
 - V_{cc} = 2.0V C-grade: 20mA (Max.) operating current
 - I-grade : 25mA (Max.) operating current
 - 0.6uA (Typ.) CMOS standby current
- High speed access time :
 - 70 70ns (Max.) at V_{cc}=2V
 - 10 100ns (Max.) at V_{cc}=2V
- Automatic power down when chip is deselected
- Three state outputs and TTL compatible
- Fully static operation
- Data retention supply voltage as low as 1.5V
- Easy expansion with CE2, $\overline{CE1}$ and \overline{OE} options
- I/O Configuration x8/x16 selectable by LB and UB pin

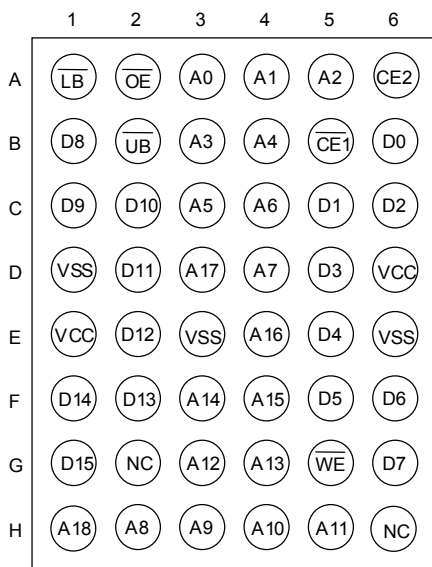
■ DESCRIPTION

The BS616UV8011 is a high performance, ultra low power CMOS Static Random Access Memory organized as 524,288 words by 16 bits and operates from a wide range of 1.8V to 2.3V supply voltage. Advanced CMOS technology and circuit techniques provide both high speed and low power features with a typical CMOS standby current of 0.6uA and maximum access time of 70/100ns in 2V operation. Easy memory expansion is provided by an active LOW chip enable($\overline{CE1}$), active HIGH chip enable (CE2), active LOW output enable(\overline{OE}) and three-state output drivers. The BS616UV8011 has an automatic power down feature, reducing the power consumption significantly when chip is deselected. The BS616UV8011 is available in 48-pin BGA package.

■ PRODUCT FAMILY

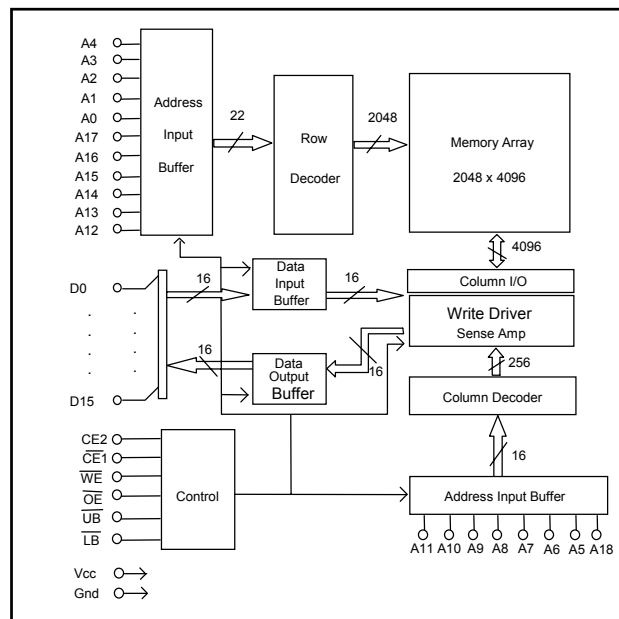
PRODUCT FAMILY	OPERATING TEMPERATURE	V _{cc} RANGE	SPEED (ns)	POWER DISSIPATION		PKG TYPE
				STANDBY (I _{ccsb1} , Max)	Operating (I _{cc} , Max)	
				V _{cc} =2V	V _{cc} =2V	
BS616UV8011DC	+0°C to +70°C	1.8 ~ 2.3V	70 / 100	15uA	20mA	DICE
BS616UV8011BC						BGA-48-0810
BS616UV8011FC						BGA-48-0912
BS616UV8011DI	-40°C to +85°C	1.8 ~ 2.3V	70 / 100	20uA	25mA	DICE
BS616UV8011BI						BGA-48-0810
BS616UV8011FI						BGA-48-0912

■ PIN CONFIGURATIONS



48-Ball CSP top View

■ BLOCK DIAGRAM



Brilliance Semiconductor Inc. reserves the right to modify document contents without notice.

■ PIN DESCRIPTIONS

Name	Function
A0-A18 Address Input	These 19 address inputs select one of the 524,288 x 16-bit words in the RAM.
$\overline{CE1}$ Chip Enable 1 Input CE2 Chip Enable 2 Input	$\overline{CE1}$ is active LOW and CE2 is active HIGH. Both chip enables must be active when data read from or write to the device. If either chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high impedance state when the device is deselected.
\overline{WE} Write Enable Input	The write enable input is active LOW and controls read and write operations. With the chip selected, when \overline{WE} is HIGH and \overline{OE} is LOW, output data will be present on the DQ pins; when \overline{WE} is LOW, the data present on the DQ pins will be written into the selected memory location.
\overline{OE} Output Enable Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when \overline{OE} is inactive.
\overline{LB} and \overline{UB} Data Byte Control Input	Lower byte and upper byte data input/output control pins.
D0 - D15 Data Input/Output Ports	These 16 bi-directional ports are used to read data from or write data into the RAM.
Vcc	Power Supply
Gnd	Ground

■ TRUTH TABLE

MODE	$\overline{CE1}$	CE2	\overline{WE}	\overline{OE}	\overline{LB}	\overline{UB}	D0~D7	D8~D15	Vcc CURRENT
Not selected (Power Down)	H	X	X	X	X	X	High Z	High Z	I_{CCSB}, I_{CCSB1}
	X	L	X	X	X	X	High Z	High Z	I_{CCSB}, I_{CCSB1}
Output Disabled	L	H	H	H	X	X	High Z	High Z	I_{CC}
Read	L	H	H	L	L	L	Dout	Dout	I_{CC}
					H	L	High Z	Dout	I_{CC}
					L	H	Dout	High Z	I_{CC}
Write	L	H	L	X	L	L	Din	Din	I_{CC}
					H	L	X	Din	I_{CC}
					L	H	Din	X	I_{CC}

■ ABSOLUTE MAXIMUM RATINGS⁽¹⁾

SYMBOL	PARAMETER	RATING	UNITS
VTERM	Terminal Voltage with Respect to GND	-0.5 to $V_{CC}+0.5$	V
TBIAS	Temperature Under Bias	-40 to +125	°C
TSTG	Storage Temperature	-60 to +150	°C
PT	Power Dissipation	1.0	W
IOUT	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	Vcc
Commercial	0°C to +70°C	1.8V ~ 2.3V
Industrial	-40°C to +85°C	1.8V ~ 2.3V

■ CAPACITANCE⁽¹⁾ (TA = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
CIN	Input Capacitance	VIN=0V	10	pF
CDQ	Input/Output Capacitance	VI/O=0V	12	pF

1. This parameter is guaranteed and not tested.

DC ELECTRICAL CHARACTERISTICS (TA = 0 to + 70°C)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MIN.	TYP. ⁽¹⁾	MAX.	UNITS
V _{IL}	Guaranteed Input Low Voltage ⁽²⁾	V _{CC} =2V	-0.5	--	0.6	V
V _{IH}	Guaranteed Input High Voltage ⁽²⁾	V _{CC} =2V	1.4	--	V _{CC} +0.2	V
I _{IL}	Input Leakage Current	V _{CC} = Max, V _{IN} = 0V to V _{CC}	--	--	1	uA
I _{OL}	Output Leakage Current	V _{CC} = Max, $\overline{CE1} = V_{IH}$, or CE2 = V _{IL} , or $\overline{OE} = V_{IH}$, V _{IO} = 0V to V _{CC}	--	--	1	uA
V _{OL}	Output Low Voltage	V _{CC} = Max, I _{OL} = 1mA	--	--	0.4	V
V _{OH}	Output High Voltage	V _{CC} = Min, I _{OH} = -0.5mA	1.6	--	--	V
I _{CC}	Operating Power Supply Current	V _{CC} =max, $\overline{CE1}=V_{IL}$ and CE2=V _{IH} , I _{OQ} = 0mA, F = Fmax ⁽³⁾	--	--	20	mA
I _{CCSB}	Standby Current -TTL	V _{CC} = max, $\overline{CE1} = V_{IH}$ or CE2 = V _{IL} , I _{OQ} = 0mA	--	--	0.6	mA
I _{CCSB1}	Standby Current -CMOS	V _{CC} = max, $\overline{CE1} \geq V_{CC}-0.2V$, or CE2 $\leq 0.2V$, V _{IN} $\geq V_{CC} - 0.2V$ or V _{IN} $\leq 0.2V$	--	0.6	15	uA

1. Typical characteristics are at TA = 25°C.

2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.

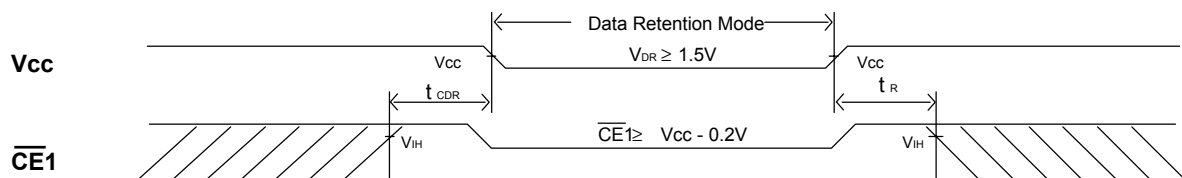
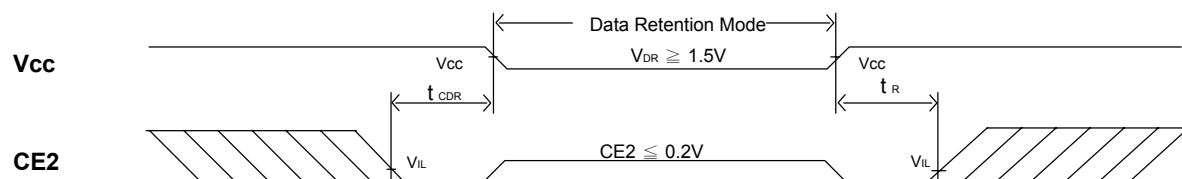
3. Fmax = 1/t_{RC}.

DATA RETENTION CHARACTERISTICS (TA = 0 to + 70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP. (1)	MAX.	UNITS
V _{DR}	V _{CC} for Data Retention	$\overline{CE1} \geq V_{CC} - 0.2V$ or CE2 $\leq 0.2V$ V _{IN} $\geq V_{CC} - 0.2V$ or V _{IN} $\leq 0.2V$	1.5	--	--	V
I _{CCDR}	Data Retention Current	$\overline{CE1} \geq V_{CC} - 0.2V$ or CE2 $\leq 0.2V$ V _{IN} $\geq V_{CC} - 0.2V$ or V _{IN} $\leq 0.2V$	--	0.4	10	uA
t _{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	--	--	ns
t _R	Operation Recovery Time		T _{RC} ⁽²⁾	--	--	ns

1. V_{CC} = 1.5V, T_A = + 25°C



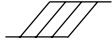


2. t_{RC} = Read Cycle Time

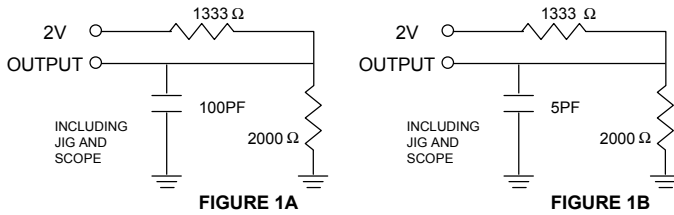
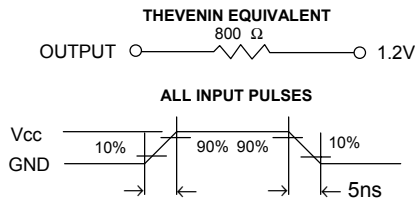
LOW V_{CC} DATA RETENTION WAVEFORM (1) ($\overline{CE1}$ Controlled)

LOW V_{CC} DATA RETENTION WAVEFORM (2) (CE2 Controlled)


AC TEST CONDITIONS

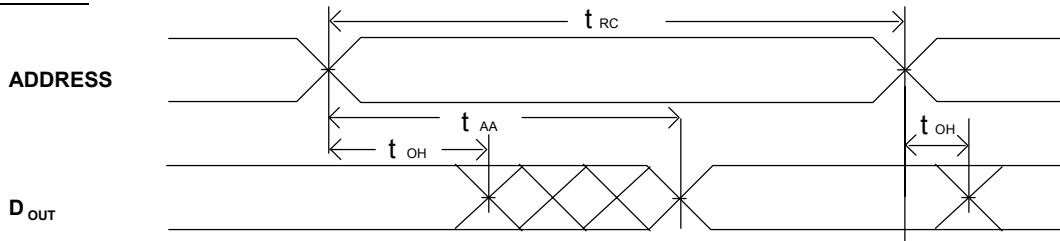
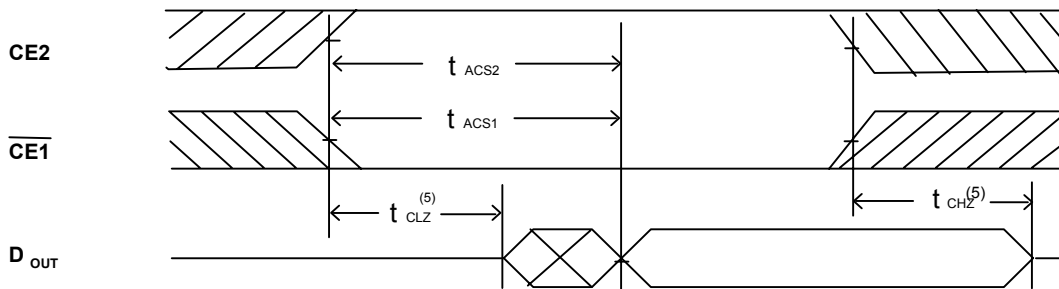
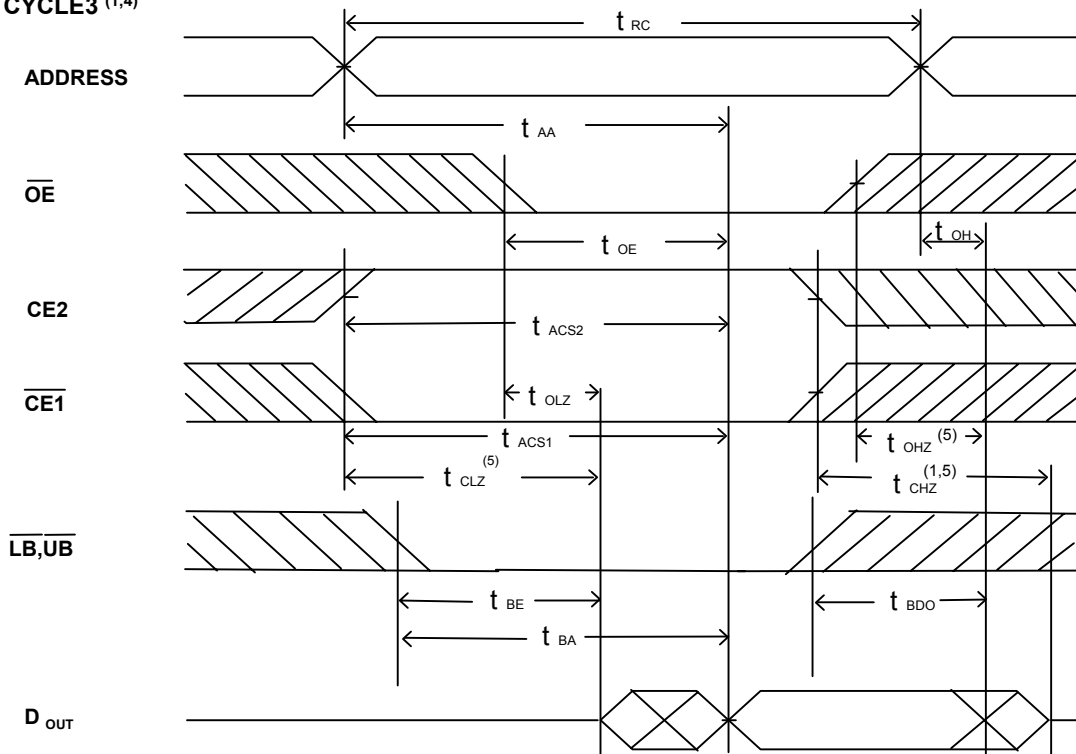
Input Pulse Levels	V _{CC} /0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	0.5V _{CC}

KEY TO SWITCHING WAVEFORMS

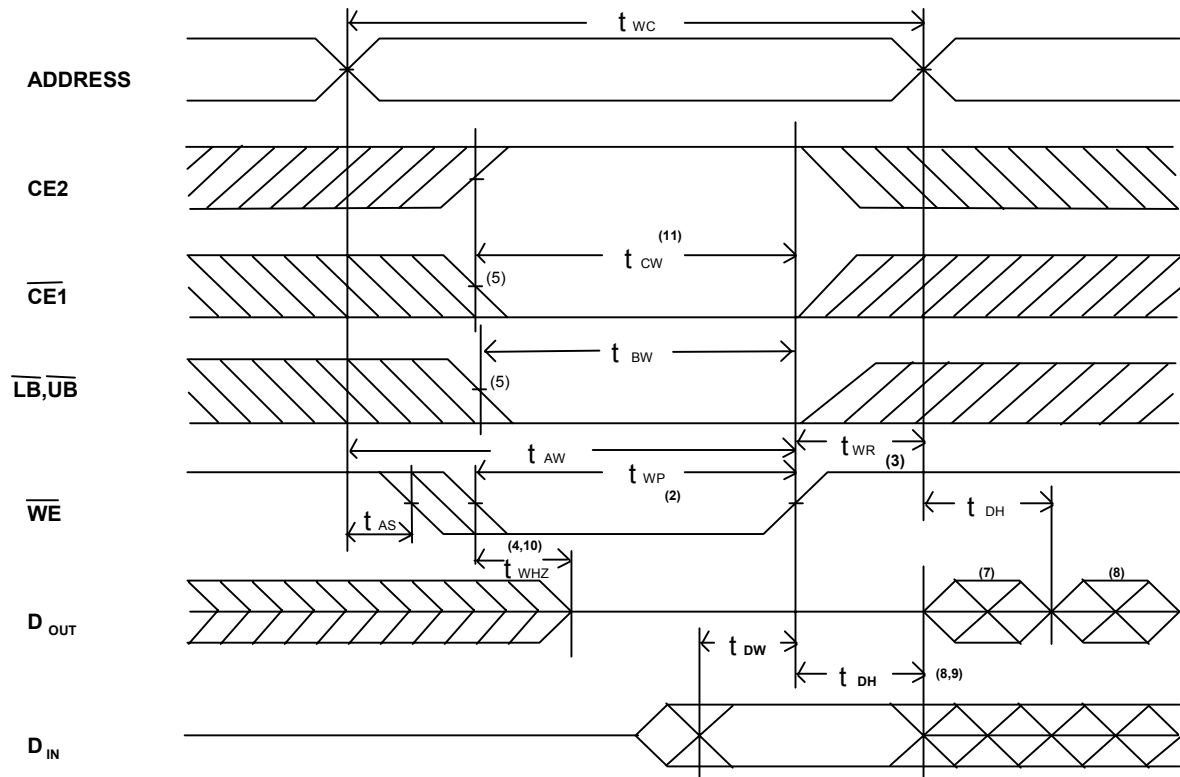
WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGE FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGE: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC TEST LOADS AND WAVEFORMS

FIGURE 1A
FIGURE 1B

FIGURE 2
AC ELECTRICAL CHARACTERISTICS (T_A = 0 to + 70°C, V_{CC}=2V)
READ CYCLE

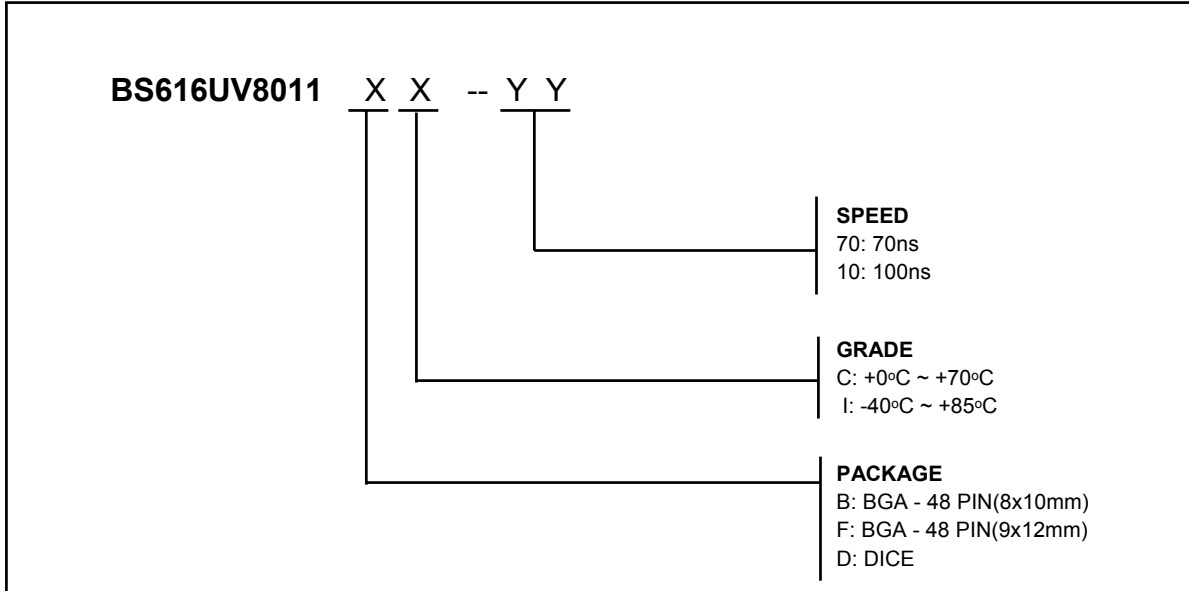
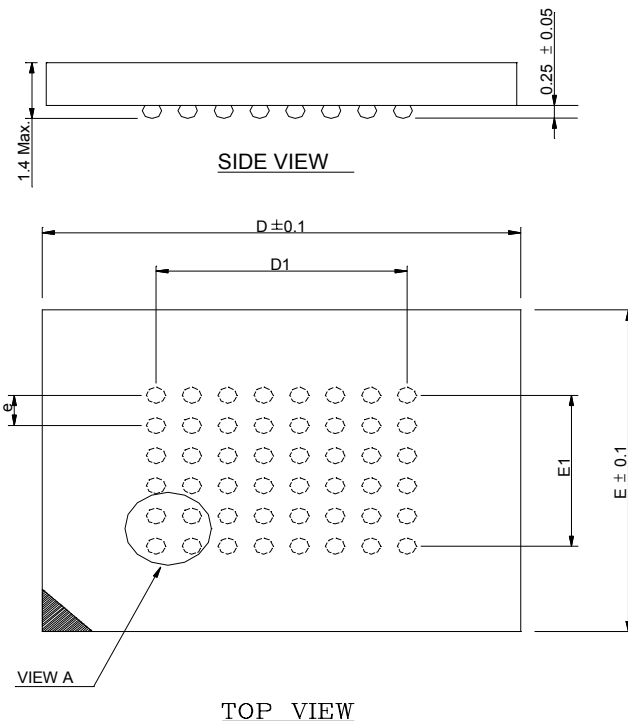
JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	BS616UV8011-70			BS616UV8011-10			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
t _{AVAX}	t _{RC}	Read Cycle Time	70	--	--	100	--	--	ns
t _{AVQV}	t _{AA}	Address Access Time	--	--	70	--	--	100	ns
t _{ELQV}	t _{ACS1}	Chip Select Access Time (CE1)	--	--	70	--	--	100	ns
t _{ELQV}	t _{ACS2}	Chip Select Access Time (CE2)	--	--	70	--	--	100	ns
t _{BA}	t _{BA}	Data Byte Control Access Time (LB,UB)	--	--	50	--	--	60	ns
t _{GLQV}	t _{OE}	Output Enable to Output Valid	--	--	50	--	--	60	ns
t _{ELQX}	t _{CLZ}	Chip Select to Output Low Z (CE2,CE1)	10	--	--	15	--	--	ns
t _{BE}	t _{BE}	Data Byte Control to Output Low Z (LB,UB)	10	--	--	15	--	--	ns
t _{GLQX}	t _{OLZ}	Output Enable to Output in Low Z	10	--	--	15	--	--	ns
t _{EHQZ}	t _{CHZ}	Chip Deselect to Output in High Z (CE2,CE1)	0	--	35	0	--	40	ns
t _{BDO}	t _{BDO}	Data Byte Control to Output High Z (LB,UB)	0	--	30	0	--	35	ns
t _{GHQZ}	t _{OHZ}	Output Disable to Output in High Z	0	--	30	0	--	35	ns
t _{AXOX}	t _{OH}	Output Disable to Address Change	10	--	--	15	--	--	ns

SWITCHING WAVEFORMS (READ CYCLE)
READ CYCLE1 (1,2,4)

READ CYCLE2 (1,3,4)

READ CYCLE3 (1,4)

NOTES:

1. \overline{WE} is high in read Cycle.
2. Device is continuously selected when $\overline{CE1} = V_{IL}$ and $CE2 = V_{IH}$.
3. Address valid prior to or coincident with CE transition low.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured $\pm 500\text{mV}$ from steady state with $C_L = 5\text{pF}$ as shown in Figure 1B. The parameter is guaranteed but not 100% tested.

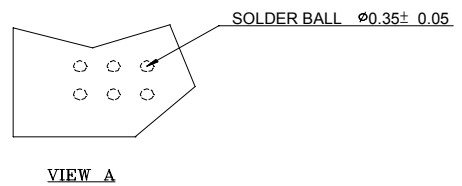
WRITE CYCLE2 (1,6)

NOTES:

1. \overline{WE} must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of CE2, $\overline{CE1}$ and \overline{WE} low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. t_{wr} is measured from the earlier of CE2 going low, or $\overline{CE1}$ or \overline{WE} going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the CE2 high transition or $\overline{CE1}$ low transition occurs simultaneously with the \overline{WE} low transitions or after the \overline{WE} transition, output remain in a high impedance state.
6. \overline{OE} is continuously low ($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If CE2 is high or $\overline{CE1}$ is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured $\pm 500mV$ from steady state with $C_L = 5pF$ as shown in Figure 1B. The parameter is guaranteed but not 100% tested.
11. t_{cw} is measured from the later of CE2 going high or $\overline{CE1}$ going low to the end of write.

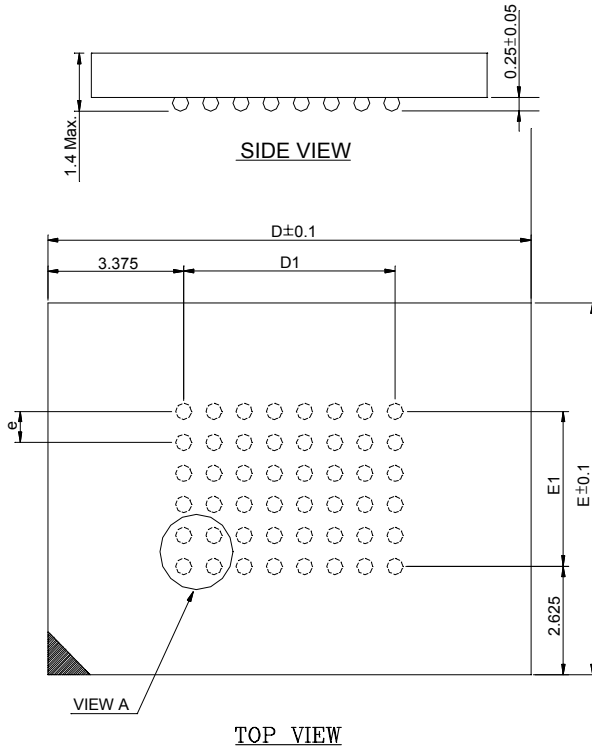
ORDERING INFORMATION

PACKAGE DIMENSIONS

NOTES:

- 1: CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
- 2: PIN#1 DOT MARKING BY LASER OR PAD PRINT.
- 3: SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.

N	D	E	D1	E1	e
48	10.0	8.0	5.25	3.75	0.75

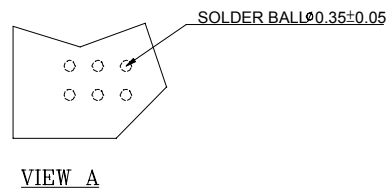


48 mini-BGA (8 x 10mm)

■ PACKAGE DIMENSIONS (continued)


- NOTES:
- 1: CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
 - 2: PIN#1 DOT MARKING BY LASER OR PAD PRINT.
 - 3: SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.

N	D	E	D1	E1	e
48	12.0	9.0	5.25	3.75	0.75



48 mini-BGA (9 x 12mm)

REVISION HISTORY

Revision	Description	Date	Note
2.2	2001 Data Sheet release	Apr. 15, 2001	