

DATA SHEET

BSP304; BSP304A P-channel enhancement mode vertical D-MOS transistors

Product specification
File under Discrete Semiconductors, SC07

1995 Apr 07

Philips Semiconductors



PHILIPS

P-channel enhancement mode vertical D-MOS transistors

BSP304; BSP304A

FEATURES

- Direct interface to C-MOS, TTL etc.
- High speed switching
- No secondary breakdown.

APPLICATIONS

- Intended for use as a Line current interruptor in telephone sets and for applications in relay, high speed and line transformer drivers.

PINNING - TO-92 variant

PIN	SYMBOL	DESCRIPTION
BSP304		
1	g	gate
2	d	drain
3	s	source
BSP304A		
1	s	source
2	g	gate
3	d	drain

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a TO-92 variant package.

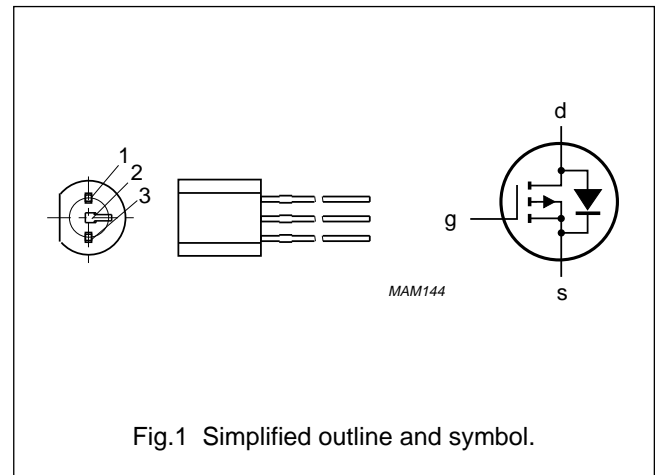


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		-	-300	V
V_{GS0}	gate-source voltage (DC)	open drain	-	± 20	V
V_{GSth}	gate-source threshold voltage	$I_D = -1 \text{ mA}; V_{DS} = V_{GS}$	-1.7	-2.55	V
I_D	drain current (DC)		-	-170	mA
R_{DSon}	drain-source on-state resistance	$I_D = -170 \text{ mA}; V_{GS} = -10 \text{ V}$	-	17	Ω
P_{tot}	total power dissipation	up to $T_{amb} = 25 \text{ }^\circ\text{C}$	-	1	W

P-channel enhancement mode vertical D-MOS transistors

BSP304; BSP304A

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–300	V
V_{GSO}	gate-source voltage (DC)	open drain	–	± 20	V
I_D	drain current (DC)		–	–170	mA
I_{DM}	peak drain current		–	–0.75	A
P_{tot}	total power dissipation	up to $T_{amb} = 25\text{ }^\circ\text{C}$; note 1	–	1	W
T_{stg}	storage temperature		–65	+150	$^\circ\text{C}$
T_j	operating junction temperature		–	150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	125	K/W

Note to the “Limiting values” and “Thermal characteristics”

1. Device mounted on a printed-circuit board, maximum lead length 4 mm; mounting pad for drain lead minimum 1 cm².

CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$; $I_D = -10\text{ }\mu\text{A}$	–300	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = V_{GS}$; $I_D = -1\text{ mA}$	–1.7	–	–2.55	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0$; $V_{DS} = -240\text{ V}$	–	–	–100	nA
I_{GSS}	gate leakage current	$V_{GS} = \pm 20\text{ V}$; $V_{DS} = 0$	–	–	± 100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = -10\text{ V}$; $I_D = -170\text{ mA}$	–	–	17	Ω
$ y_{fs} $	forward transfer admittance	$V_{DS} = -25\text{ V}$; $I_D = -170\text{ mA}$	100	–	–	mS
C_{iss}	input capacitance	$V_{GS} = 0$; $V_{DS} = -25\text{ V}$; $f = 1\text{ MHz}$	–	60	90	pF
C_{oss}	output capacitance	$V_{GS} = 0$; $V_{DS} = -25\text{ V}$; $f = 1\text{ MHz}$	–	15	30	pF
C_{rss}	reverse transfer capacitance	$V_{GS} = 0$; $V_{DS} = -20\text{ V}$; $f = 1\text{ MHz}$	–	5	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$V_{GS} = 0$ to -10 V ; $V_{DD} = -50\text{ V}$; $I_D = -250\text{ mA}$	–	5	10	ns
t_{off}	turn-off time	$V_{GS} = -10$ to 0 V ; $V_{DD} = -50\text{ V}$; $I_D = -250\text{ mA}$	–	15	30	ns

P-channel enhancement mode vertical D-MOS transistors

BSP304; BSP304A

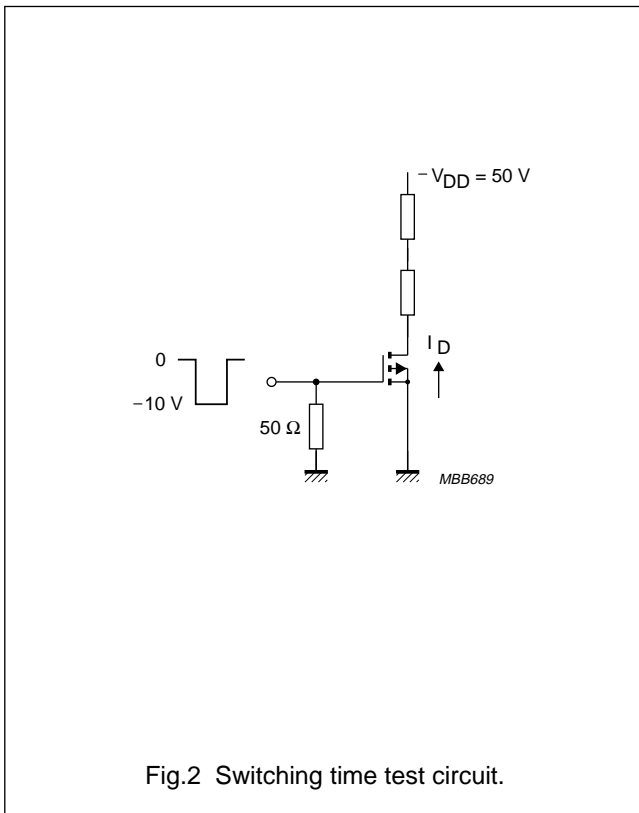


Fig.2 Switching time test circuit.

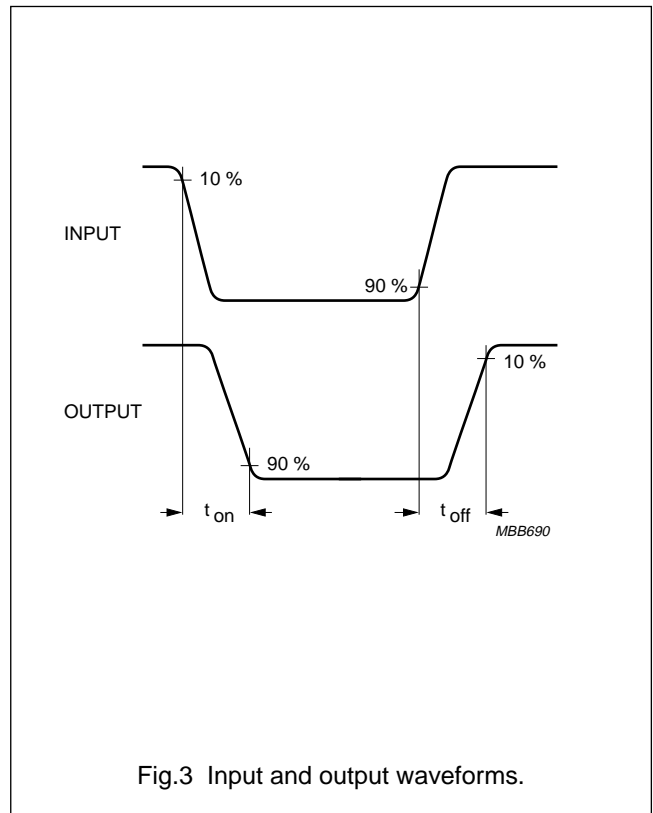


Fig.3 Input and output waveforms.

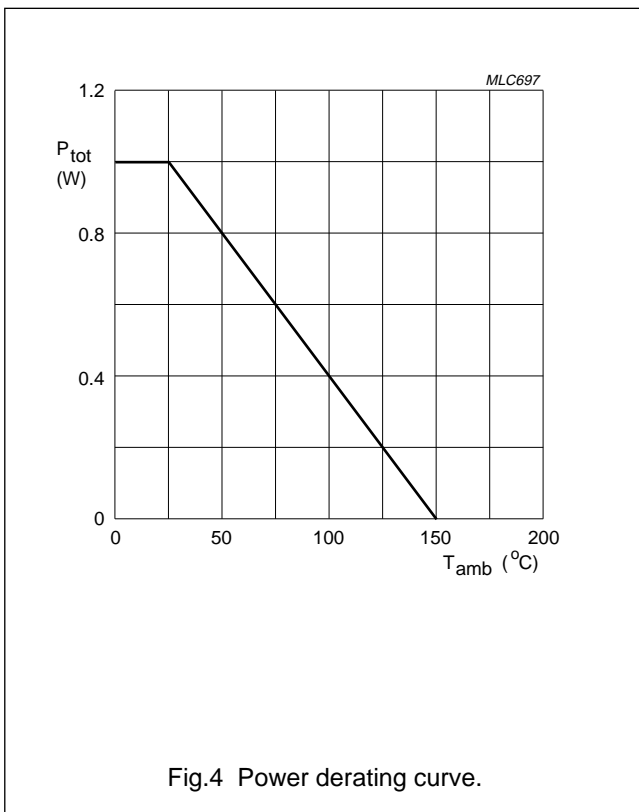
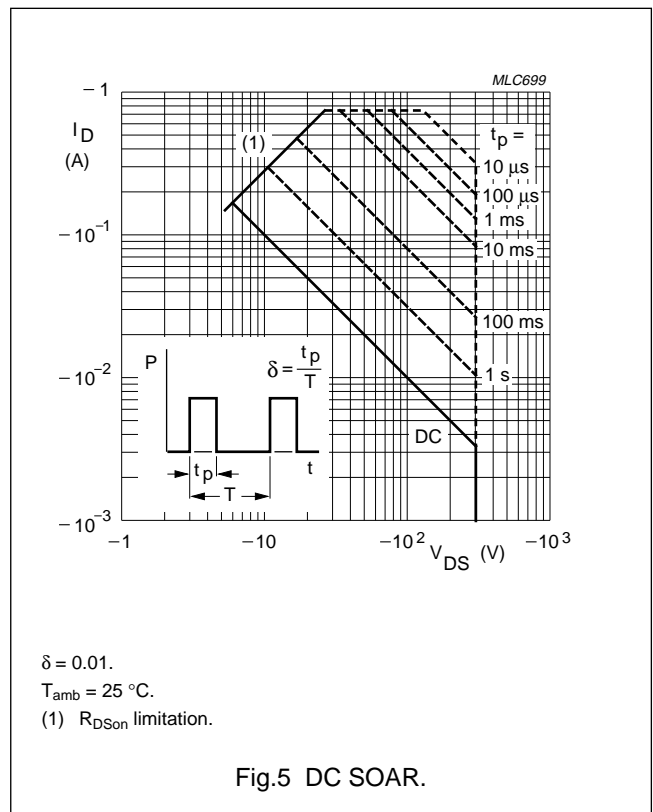


Fig.4 Power derating curve.

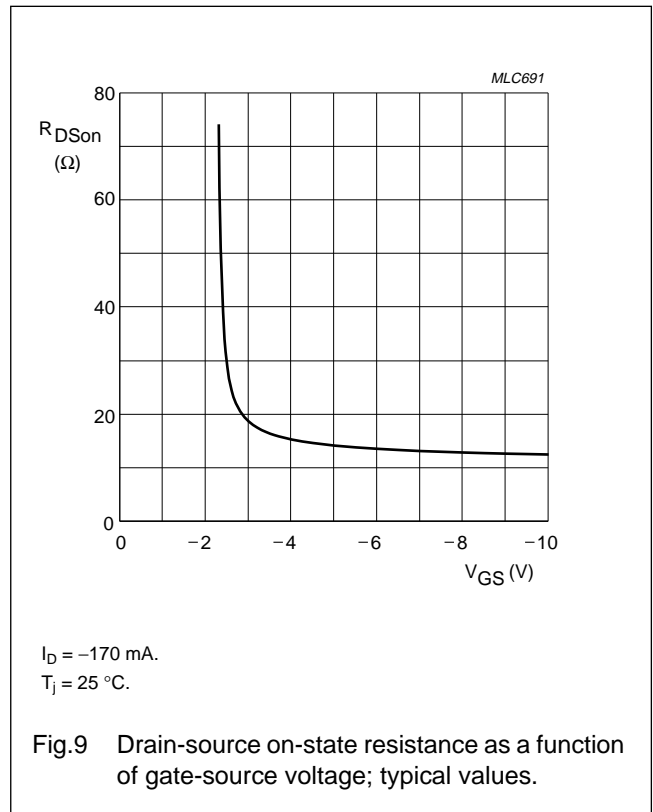
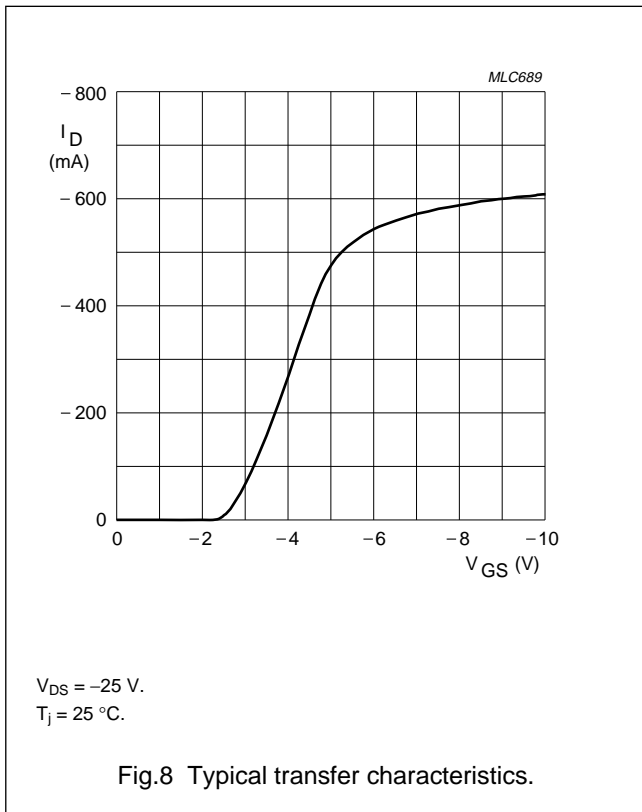
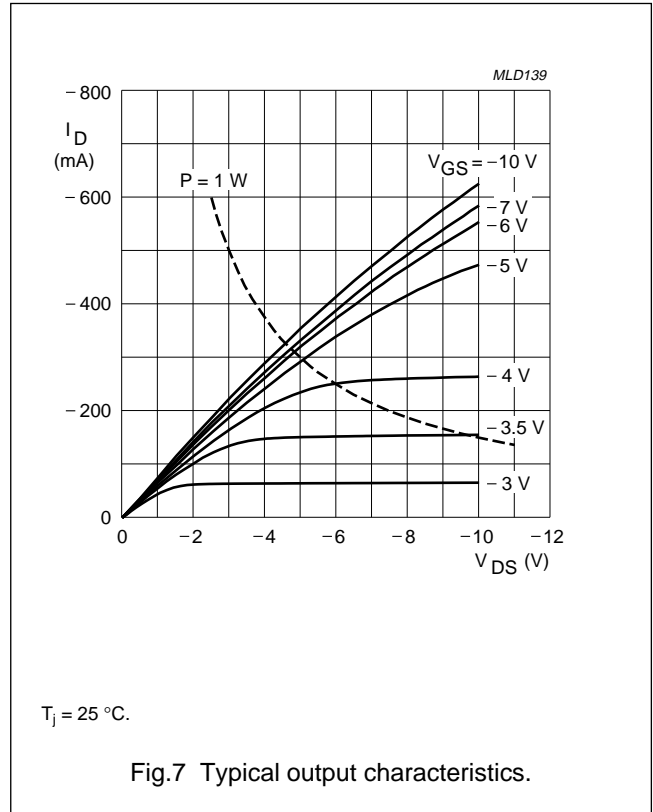
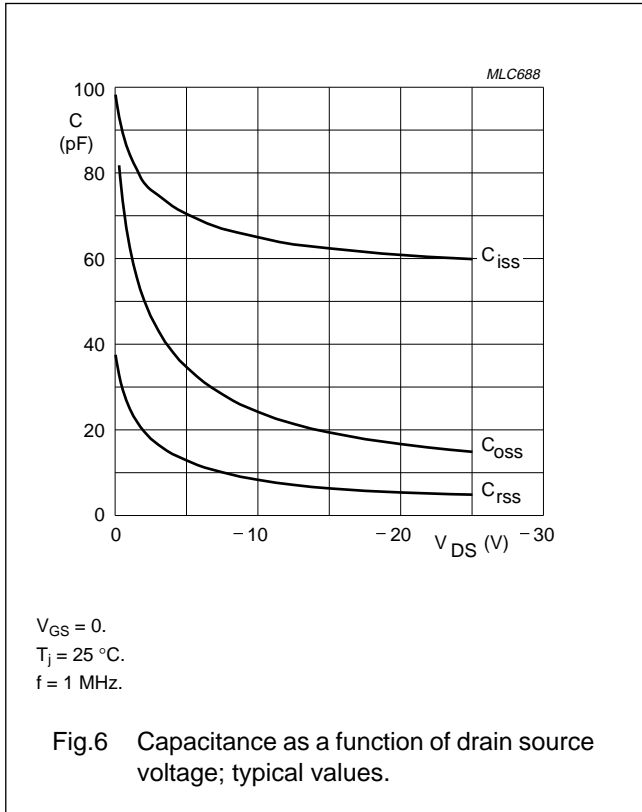


$\delta = 0.01$.
 $T_{amb} = 25\text{ }^{\circ}\text{C}$.
 (1) R_{DSon} limitation.

Fig.5 DC SOAR.

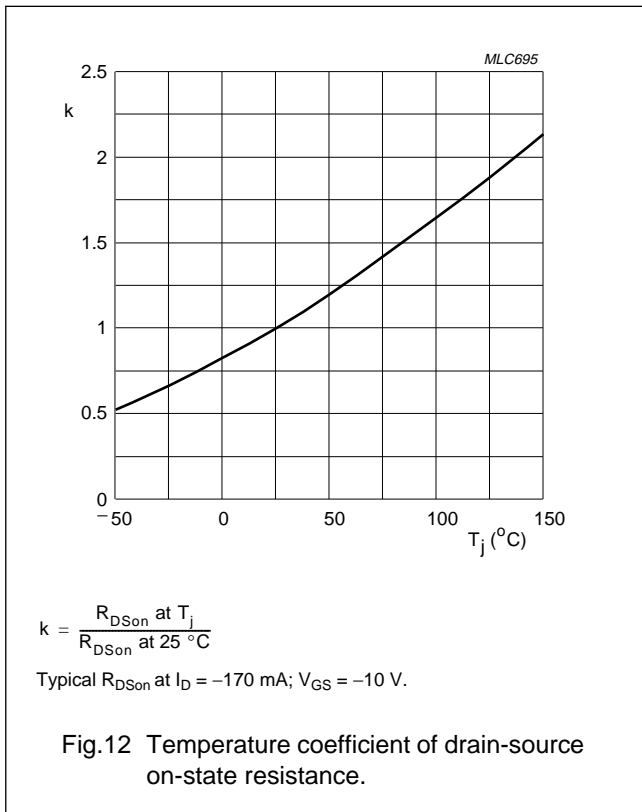
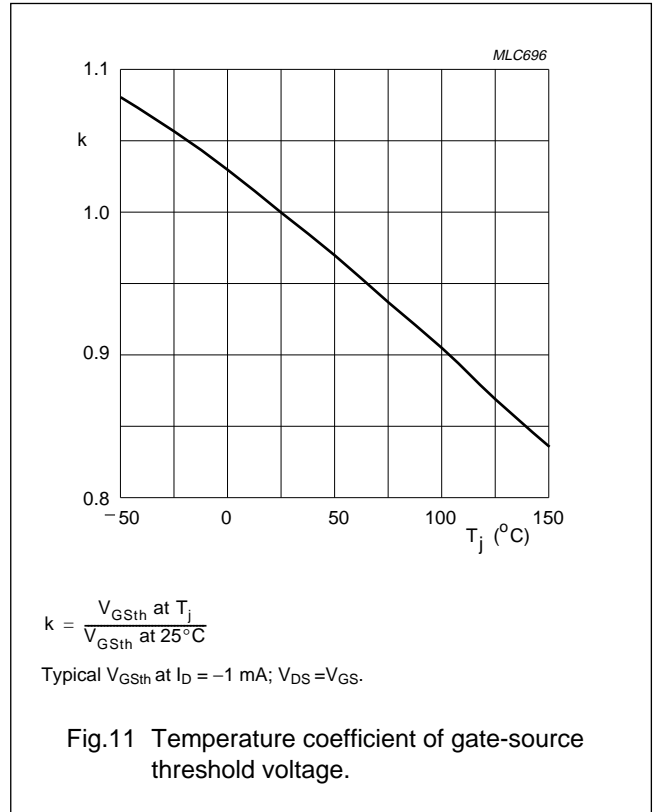
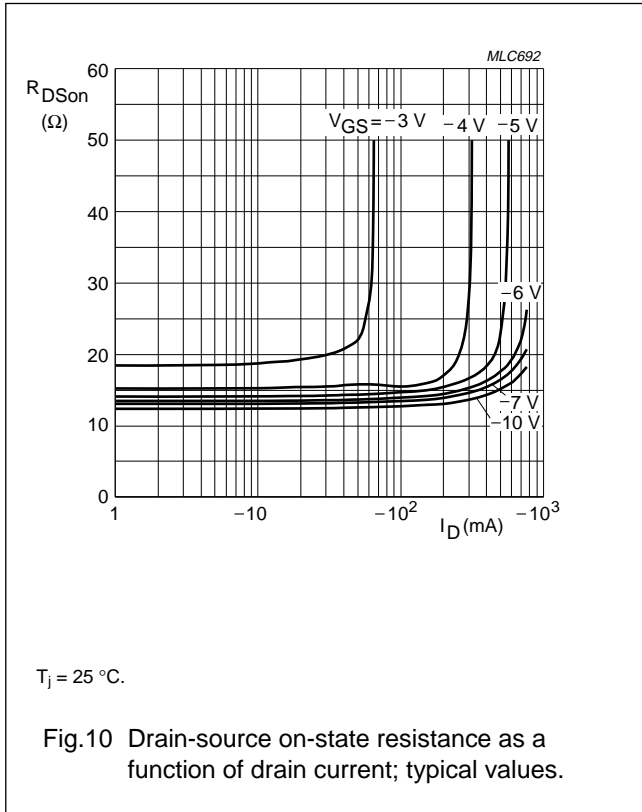
P-channel enhancement mode vertical D-MOS transistors

BSP304; BSP304A



P-channel enhancement mode vertical D-MOS transistors

BSP304; BSP304A



P-channel enhancement mode
vertical D-MOS transistors

BSP304; BSP304A

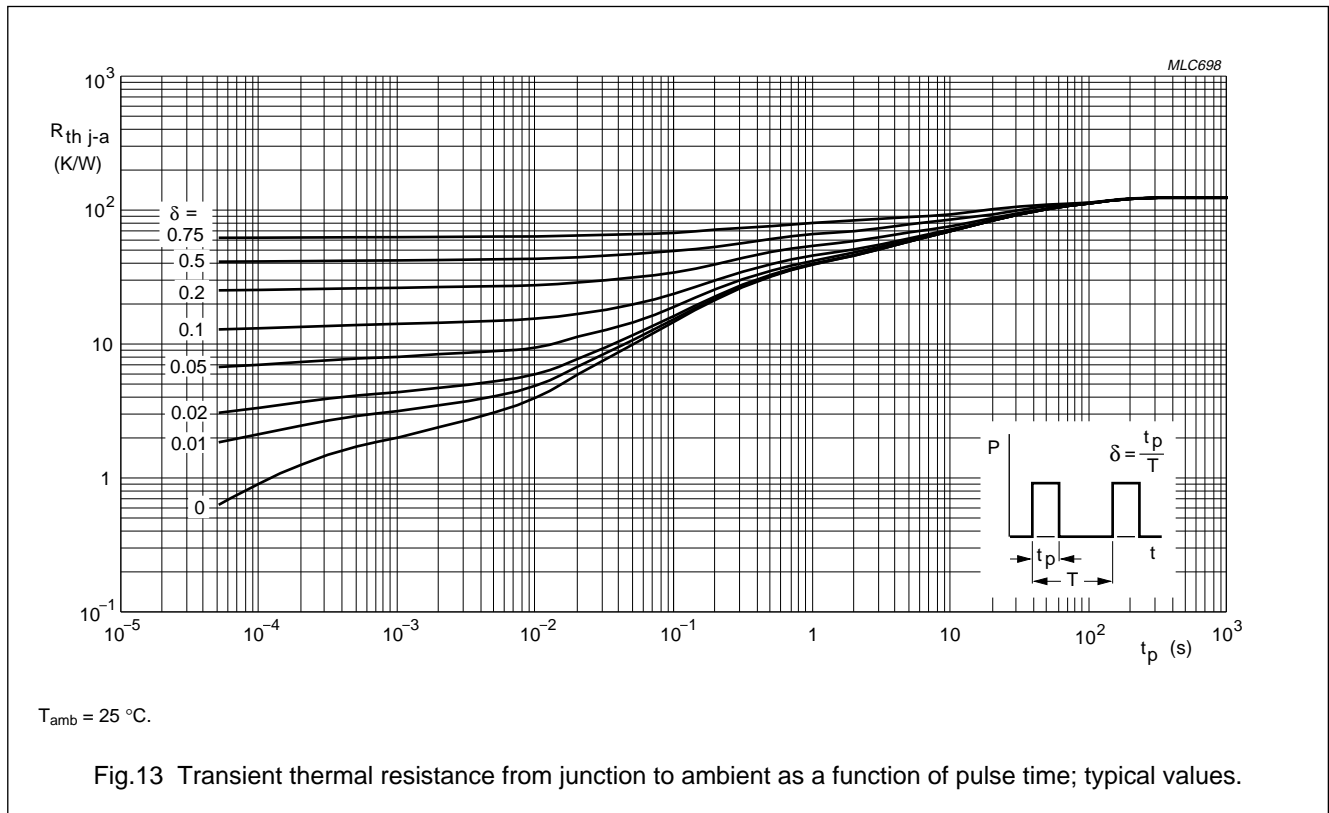
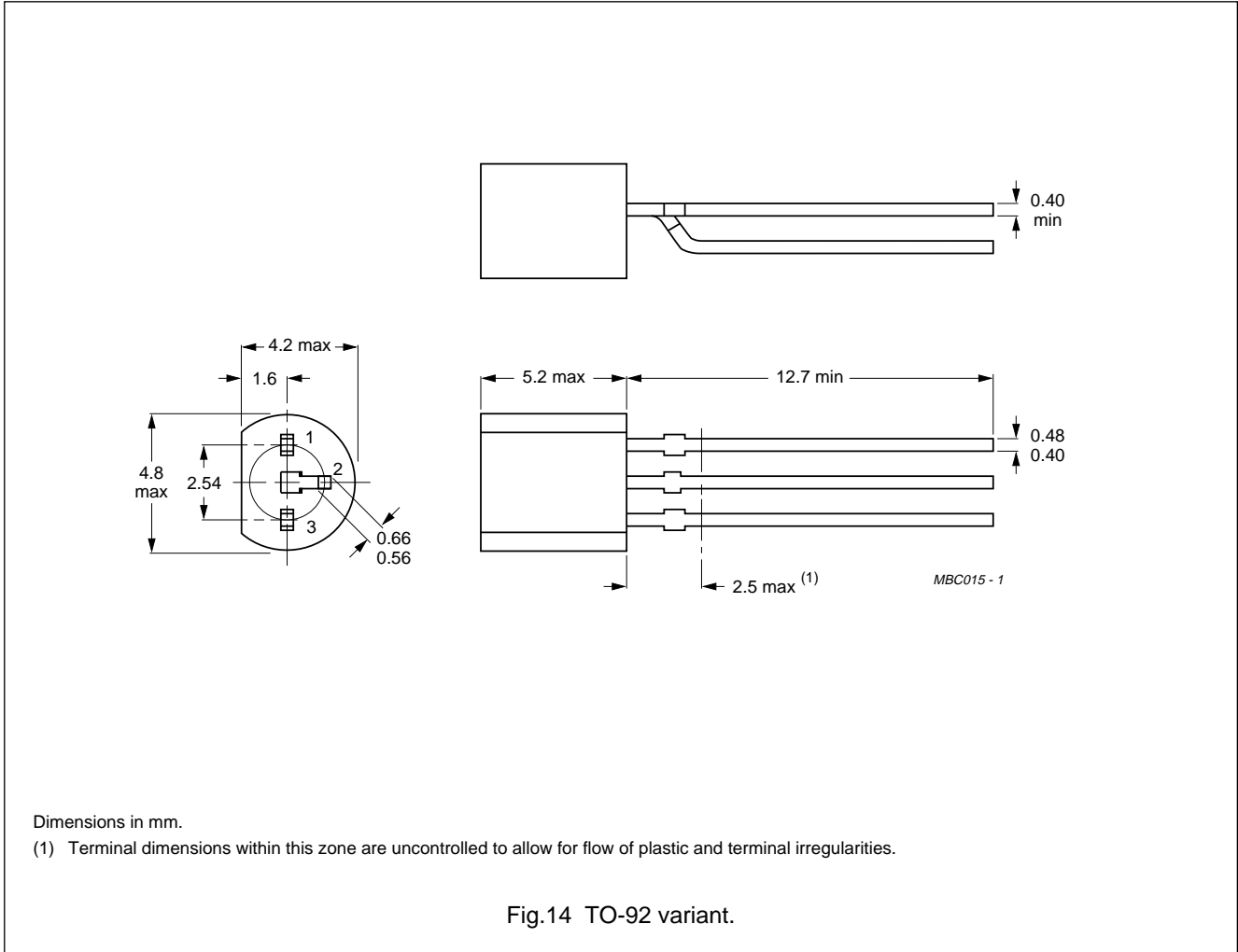


Fig.13 Transient thermal resistance from junction to ambient as a function of pulse time; typical values.

P-channel enhancement mode
vertical D-MOS transistors

BSP304; BSP304A

PACKAGE OUTLINE



P-channel enhancement mode vertical D-MOS transistors

BSP304; BSP304A

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.