# BT169H

## Thyristor, logic level, high voltage

Rev. 01 — 31 March 2008 Product data sheet

## 1. Product profile

### 1.1 General description

Passivated sensitive gate thyristor in a SOT54 plastic package.

### 1.2 Features

- Very sensitive gate
- Direct interfacing to logic level ICs
- High blocking voltage
- Direct interfacing to low power gate drive circuits

### 1.3 Applications

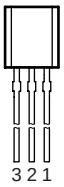
- General purpose switching and phase control
- Earth leakage circuit breakers or Ground Fault Circuit Interrupters (GFCI)

### 1.4 Quick reference data

- $V_{RRM}$, $V_{DRM} \leq 800$ V
- $I_{T(RMS)} \leq 0.8$ A
- $I_{T(AV)} \leq 0.5$ A
- $I_{GT} \leq 100$ µA
- $I_{TSM} \leq 9$ A (t = 10 ms)

## 2. Pinning information

**Table 1. Pinning**

| Pin | Description | Simplified outline | Graphic symbol |
|---|---|---|---|
| 1 | anode (A) |   SOT54 (TO-92) |   |
| 2 | gate (G) | | |
| 3 | cathode (K) | | |

## 3. Ordering information

**Table 2. Ordering information**

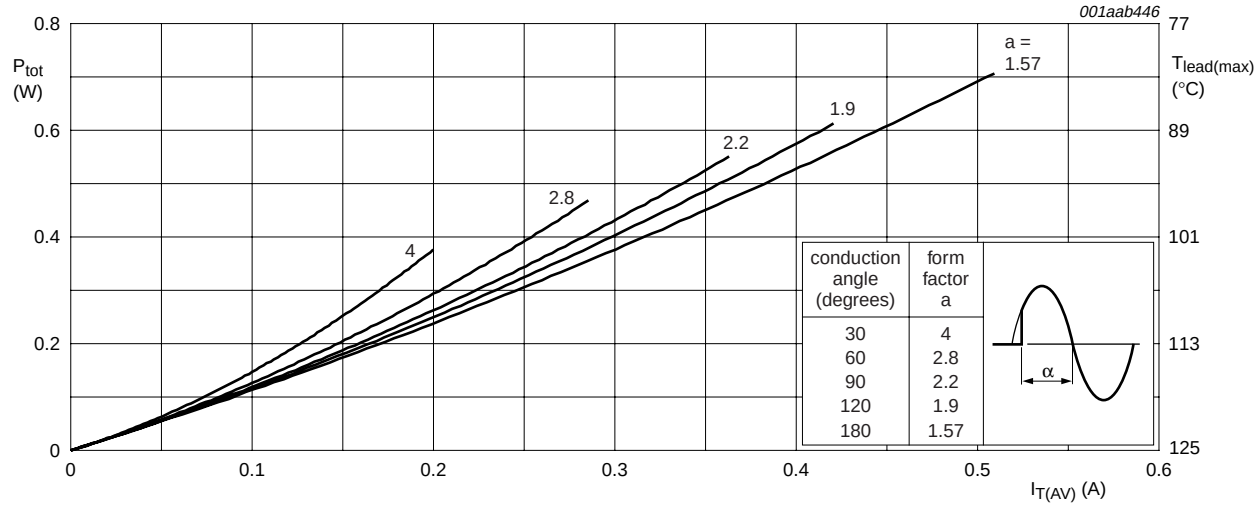
| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| BT169H | TO-92 | plastic single-ended leaded (through hole) package; 3 leads | SOT54 |

## 4. Limiting values

**Table 3. Limiting values**

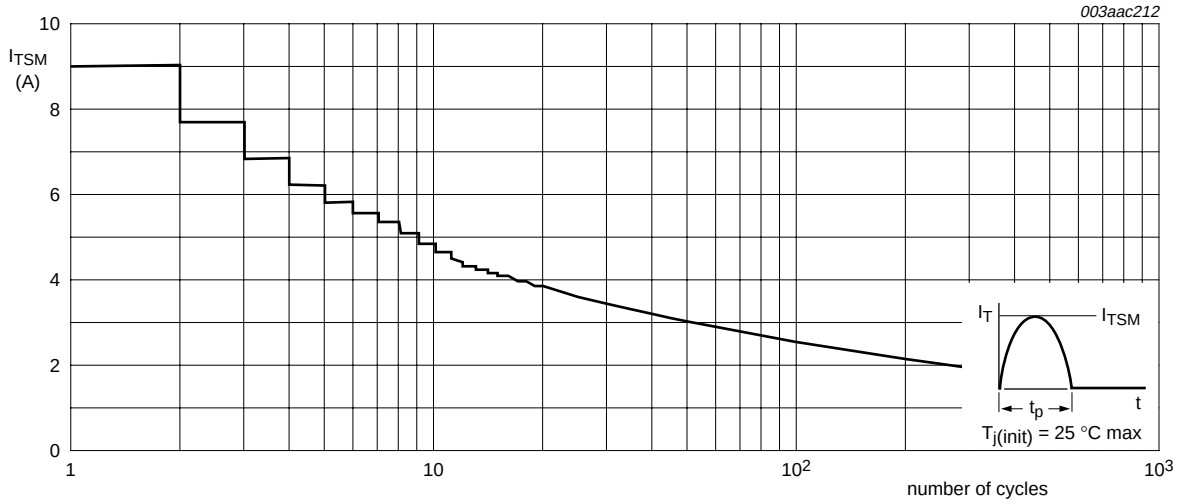
*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DRM}$ | repetitive peak off-state voltage | | - | 800 | V |
| $V_{RRM}$ | repetitive peak reverse voltage | | - | 800 | V |
| $I_{T(AV)}$ | average on-state current | half sine wave; $T_{lead} \leq 83$ °C; see Figure 1 | - | 0.5 | A |
| $I_{T(RMS)}$ | RMS on-state current | all conduction angles; see Figure 4 and 5 | - | 0.8 | A |
| $I_{TSM}$ | non-repetitive peak on-state current | half sine wave; $T_j = 25$ °C prior to surge; see Figure 2 and 3 | | | |
| | | t = 10 ms | - | 9 | A |
| | | t = 8.3 ms | - | 10 | A |
| $I^2t$ | $I^2t$ for fusing | $t_p = 10$ ms | - | 0.41 | $A^2s$ |
| $dI_T/dt$ | rate of rise of on-state current | $I_{TM} = 2$ A; $I_G = 10$ mA; $dI_G/dt = 100$ mA/µs | - | 50 | A/µs |
| $I_{GM}$ | peak gate current | | - | 1 | A |
| $V_{RGM}$ | peak reverse gate voltage | | - | 5 | V |
| $P_{GM}$ | peak gate power | | - | 2 | W |
| $P_{G(AV)}$ | average gate power | over any 20 ms period | - | 0.1 | W |
| $T_{stg}$ | storage temperature | | –40 | +150 | °C |
| $T_j$ | junction temperature | | - | 125 | °C |



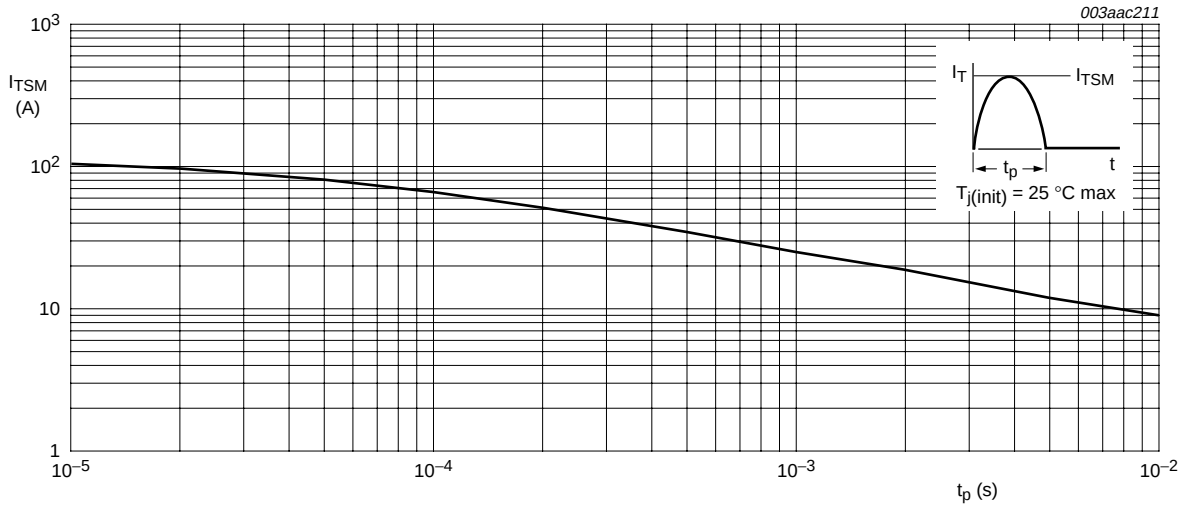

α = conduction angle

**Fig 1. Total power dissipation as a function of average on-state current; maximum values**



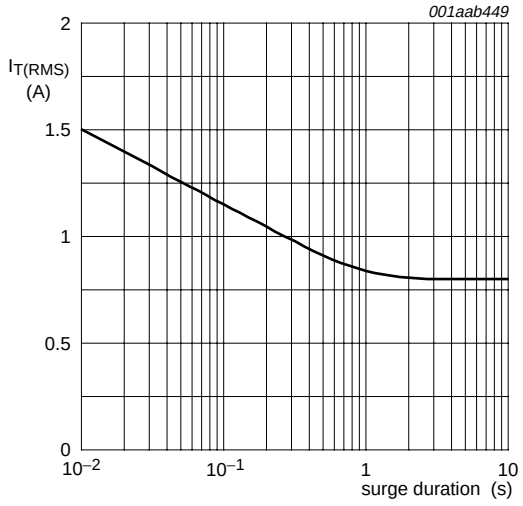

f = 50 Hz

**Fig 2. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values**




$t_p \leq 10$ ms

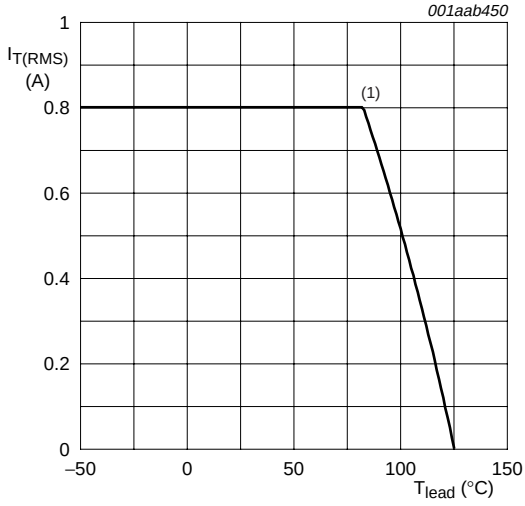
**Fig 3. Non-repetitive peak on-state current as a function of pulse width; maximum values**




f = 50 Hz

$T_{lead}$ = 83 °C

**Fig 4. RMS on-state current as a function of surge duration; maximum values**




(1) $T_{lead}$ = 83 °C

**Fig 5. RMS on-state current as a function of lead temperature; maximum values**

## 5. Thermal characteristics

**Table 4. Thermal characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{th(j\text{-}lead)}$ | thermal resistance from junction to lead | see Figure 6 | - | - | 60 | K/W |
| $R_{th(j\text{-}a)}$ | thermal resistance from junction to ambient | printed circuit board mounted; lead length 4 mm | - | 150 | - | K/W |

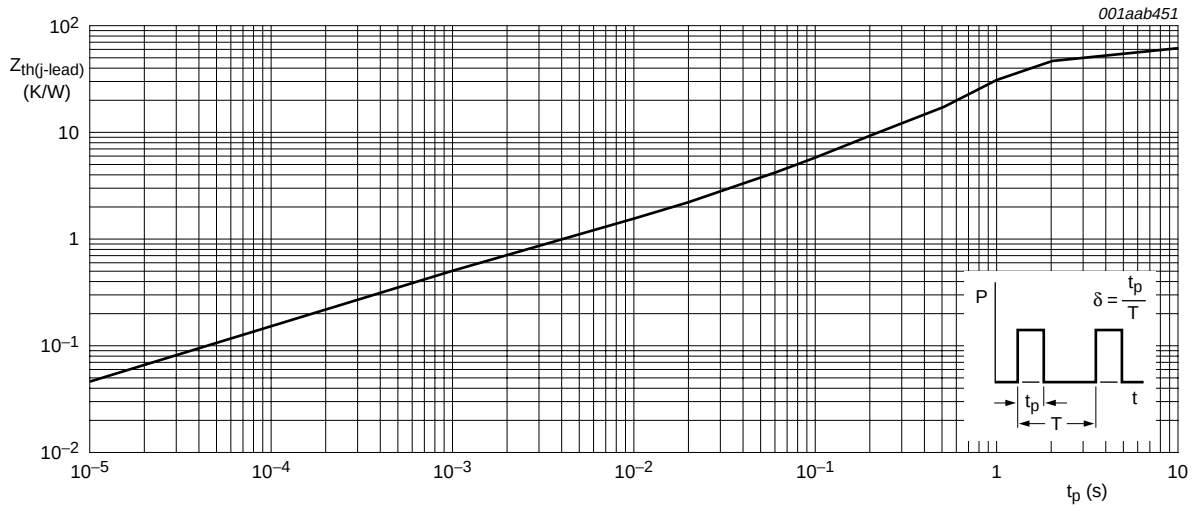



**Fig 6. Transient thermal impedance from junction to lead as a function of pulse width**

## 6. Characteristics

**Table 5. Characteristics**

*$T_j$ = 25 °C unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | |
| $I_{GT}$ | gate trigger current | $V_D$ 4= 12 V; $I_T$ = 10 mA; see Figure 8 | 1 | 50 | 100 | µA |
| $I_L$ | latching current | $V_D$ = 12 V; $I_G$ = 0.5 mA; $R_{GK}$ = 1 kΩ; see Figure 10 | - | 2 | 6 | mA |
| $I_H$ | holding current | $V_D$ = 12 V; $I_G$ = 0.5 mA; $R_{GK}$ = 1 kΩ; see Figure 11 | - | 1.5 | 3 | mA |
| $V_T$ | on-state voltage | $I_T$ = 1.2 A; see Figure 9 | - | 1.25 | 1.7 | V |
| $V_{GT}$ | gate trigger voltage | $I_T$ = 10 mA; see Figure 7 | | | | |
| | | $V_D$ = 12 V | - | 0.5 | 0.8 | V |
| | | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | 0.2 | 0.3 | - | V |
| $I_D$ | off-state current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C; $R_{GK}$ = 1 kΩ | - | 0.05 | 0.1 | mA |
| $I_R$ | reverse current | $V_R = V_{RRM(max)}$; $T_j$ = 125 °C; $R_{GK}$ = 1 kΩ | - | 0.05 | 0.1 | mA |
| **Dynamic characteristics** | | | | | | |
| $dV_D/dt$ | rate of rise of off-state voltage | $V_{DM} = 0.67 \times V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; see Figure 12 | | | | |
| | | $R_{GK}$ = 1 kΩ | 150 | 350 | - | V/µs |
| $t_{gt}$ | gate-controlled turn-on time | $I_{TM}$ = 2 A; $V_D = V_{DRM(max)}$; $I_G$ = 10 mA; $dI_G/dt$ = 0.1 A/µs | - | 2 | - | µs |
| $t_q$ | commutated turn-off time | $V_D = 0.67 \times V_{DRM(max)}$; $T_j$ = 125 °C; $I_{TM}$ = 1.6 A; $V_R$ = 35 V; $(dI_T/dt)_M$ = 30 A/µs; $dV_D/dt$ = 2 V/µs; $R_{GK}$ = 1 kΩ | - | 100 | - | µs |

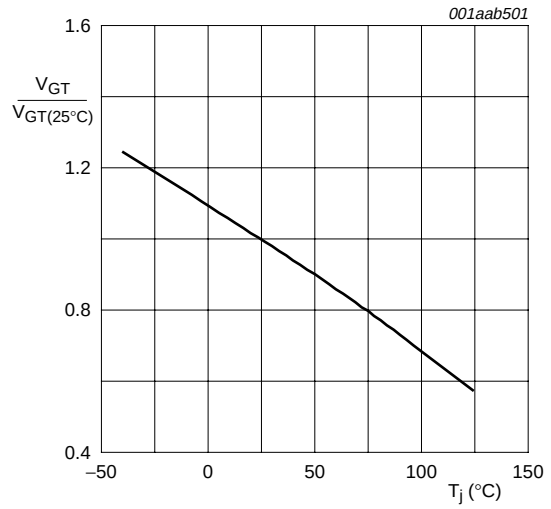



**Fig 7. Normalized gate trigger voltage as a function of junction temperature**

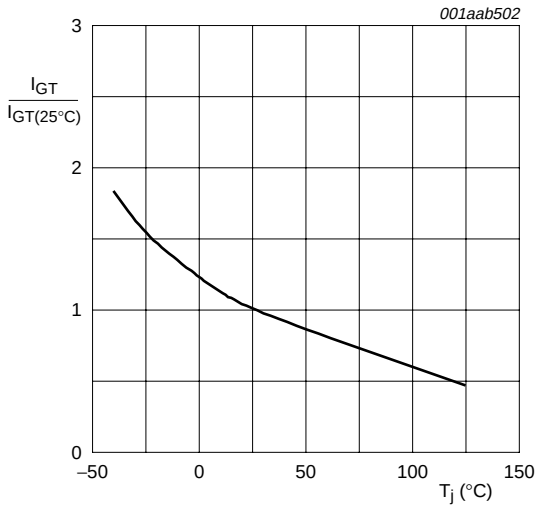
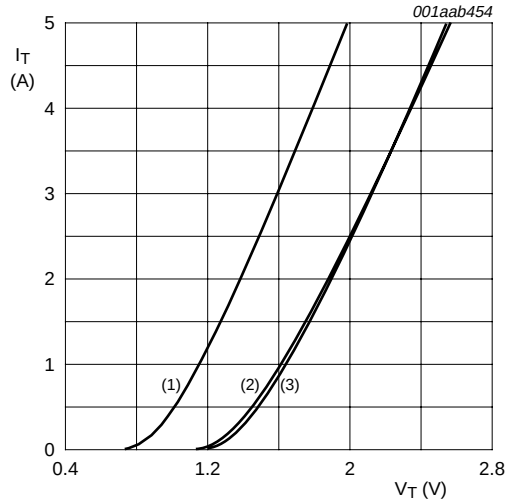



**Fig 8. Normalized gate trigger current as a function of junction temperature**




$V_o$ = 1.067 V

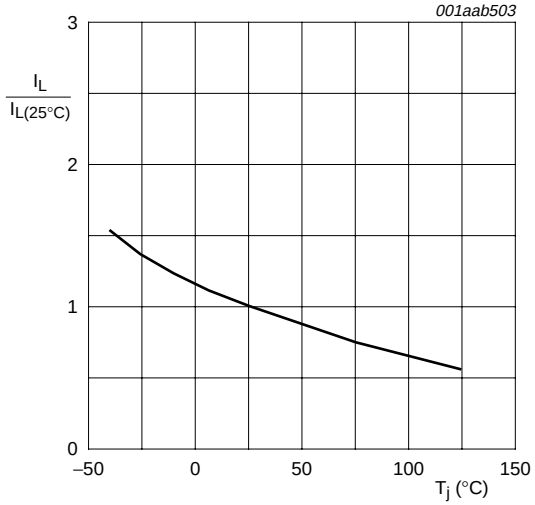
$R_s$ = 0.187 Ω

(1) $T_j$ = 125 °C; typical values

(2) $T_j$ = 125 °C; maximum values

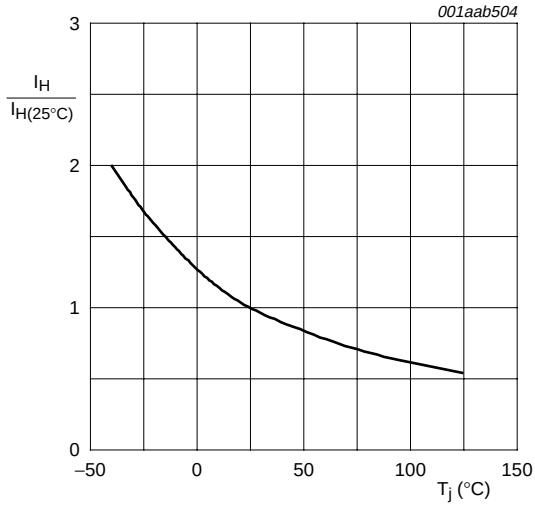
(3) $T_j$ = 25 °C; maximum values

**Fig 9. On-state current as a function of on-state voltage**



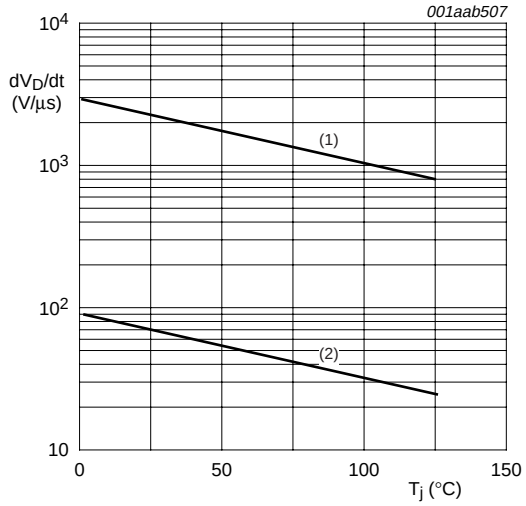

$R_{GK}$ = 1 kΩ

**Fig 10. Normalized latching current as a function of junction temperature**




$R_{GK}$ = 1 kΩ

**Fig 11. Normalized holding current as a function of junction temperature**



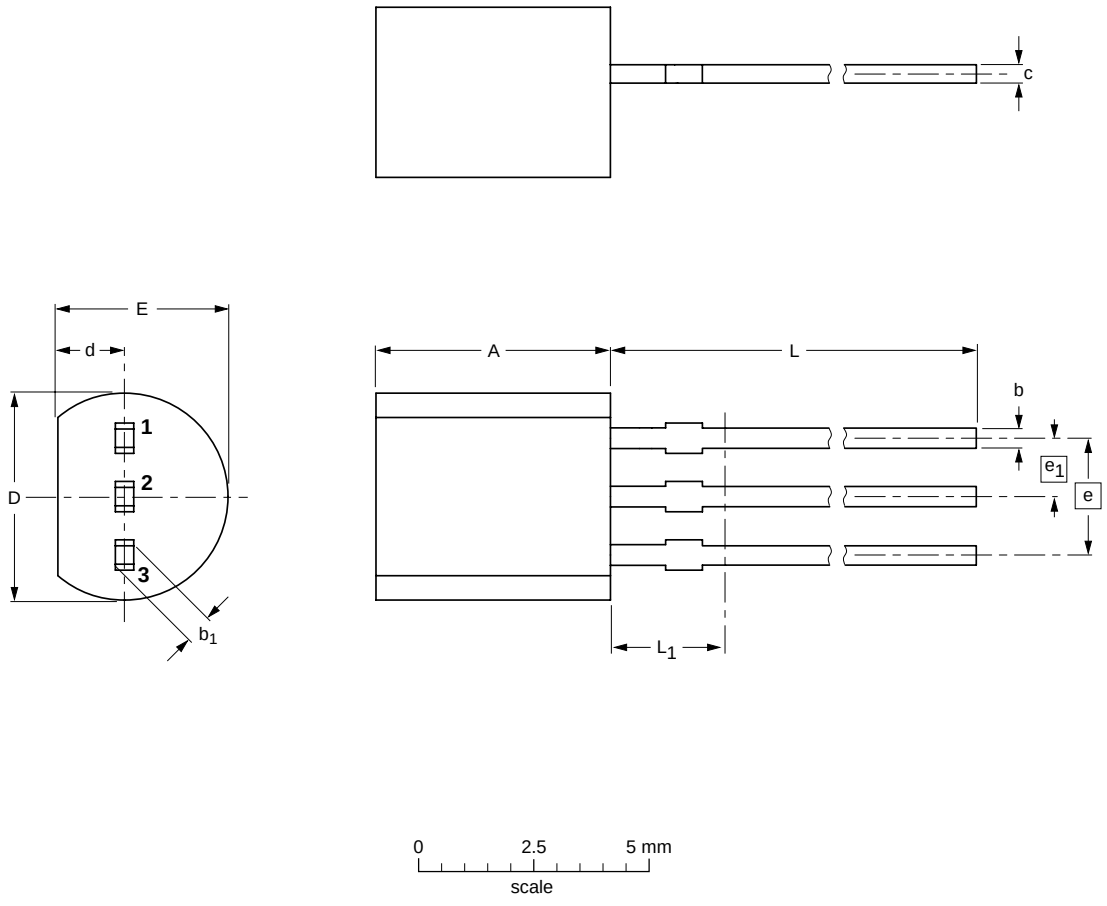

(1) $R_{GK}$ = 1 kΩ

(2) Gate open circuit

**Fig 12. Critical rate of rise of off-state voltage as a function of junction temperature; typical values**

## 7. Package outline

**Plastic single-ended leaded (through hole) package; 3 leads** **SOT54**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | b | $b_1$ | c | D | d | E | e | $e_1$ | L | $L_1$ (1) max. |
|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 5.2<br>5.0 | 0.48<br>0.40 | 0.66<br>0.55 | 0.45<br>0.38 | 4.8<br>4.4 | 1.7<br>1.4 | 4.2<br>3.6 | 2.54 | 1.27 | 14.5<br>12.7 | 2.5 |

**Note**

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT54 | | TO-92 | SC-43A | | | ~~04-06-28~~<br>04-11-16 |

**Fig 13. Package outline SOT54 (TO-92)**

## 8. Revision history

Table 6. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| BT169H_1 | 20080331 | Product data sheet | - | - |

# 9. Legal information

## 9.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
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| Product [short] data sheet | Production | This document contains the product specification. |

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[2] The term 'short data sheet' is explained in section "Definitions".

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## 11. Contents





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