Single-chip 4-bit microcontroller for CD-DA

BU34381

The BU34381 is a 4-bit microcomputer designed for CD-DA players, and has a wide array of internal I / O components, including an 8-bit, 8-channel AD converter, pulse width counter (PWC), two serial I / O, and an LCD controller / driver capable of displaying up to 80 segments. All LCD segments are programmable for CMOS output. These I / O components allow for multifunction applications with a low number of pins.

●Applications
Portable CD-DA players, portable CD stereos

●Features
1) High speed operations and low voltage. (V_{DD} = 2.7 ～ 5.5V at 4.4MHz)
2) Internal 8-bit, 8-channel AD converter.
3) Internal pulse width counter.
4) Two internal serial input / outputs.
5) Internal 20-segment, 4-common LCD controller / driver. (usable with 3 commons)
6) All segments output by the LCD controller / driver are programmable for CMOS output.

●Absolute maximum ratings (Ta = 25°C)

| Parameter	Symbol	Limits	Unit
Applied voltage	V_{DD}	－0.3～＋7.0	V
Power dissipation	Pd	500＊	mW
Operating temperature	Topr	－25～＋75	℃
Storage temperature	Tstg	－55～＋125	℃

＊ Reduced by 5.0 mW for each increase in Ta of 1℃ over 25℃.

●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	2.7	—	5.5	V
Input high level voltage (without hysteresis)	V_{IH}	$0.7V_{DD}$	—	V_{DD}	V
Input low level voltage (without hysteresis)	V_{IL}	0	—	$0.3V_{DD}$	V
Input high level voltage (with hysteresis)	V_{IHS}	$0.75V_{DD}$	—	V_{DD}	V
Input low level voltage (with hysteresis)	V_{ILS}	0	—	$0.25V_{DD}$	V

●Block diagram
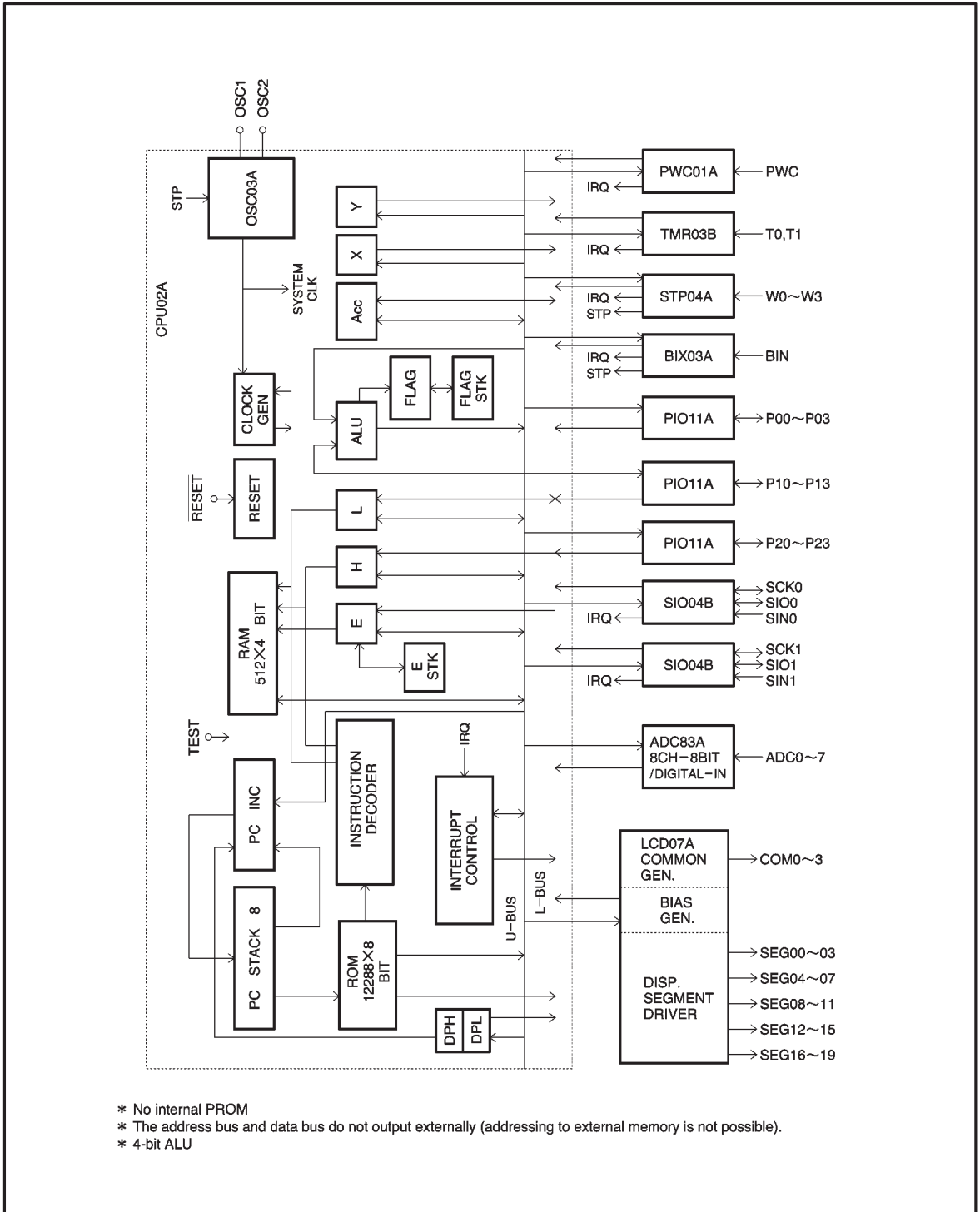
* No internal PROM
* The address bus and data bus do not output externally (addressing to external memory is not possible).
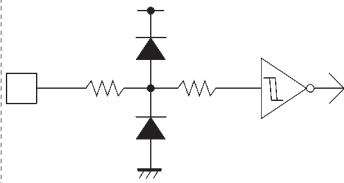* 4-bit ALU

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● Pin assignments

Pins (top, left to right, 48–33): GND, RESET, W3, W2, W1, W0, BIN, SCK1, SIO1, SIN1, P23, P22, P21, P20, T1, T0

Left side (top to bottom, 49–64): OSC1 49, OSC2 50, VDD 51, ADC0 52, ADC1 53, ADC2 54, ADC3 55, ADC4 56, ADC5 57, ADC6 58, ADC7 59, TEST 60, COM0 61, COM1 62, COM2 63, COM3 64

Center: **BU34381**

Right side (top to bottom, 32–17): 32 PWC, 31 P13, 30 P12, 29 P11, 28 P10, 27 P03, 26 P02, 25 P01, 24 P00, 23 SCK0, 22 SIO0, 21 SIN0, 20 SEG19, 19 SEG18, 18 SEG17, 17 SEG16

Bottom (left to right, 1–16): SEG00, SEG01, SEG02, SEG03, SEG04, SEG05, SEG06, SEG07, SEG08, SEG09, SEG10, SEG11, SEG12, SEG13, SEG14, SEG15

● Pin descriptions

Pin No.	Pin name	I / O	Function	Type
24～27 28～31 35～38	P00～P03 P10～P13 P20～P23 （PI011A block）	I／O	• 4-bit input and output • Each bit is programmable for input or output (open drain output N-channel) • Pull-up resistor ON/OFF operation is programmable (each bit can be set separately). • Resetting turns the pull-up resistors off via input. [*1]	D
43～46	W0～W3 （STP04A block）	I	• Standard 4-bit input • Programmable for stop cancel input or interrupt request signal output (each bit can be set separately). • Pull-up resistor ON/OFF operation is programmable (each bit can be set separately). • Resetting turns the pull-up resistors off.	C
42	BIN （BIX03A block）	I	• Standard 1-bit input • Programmable for stop cancel input or interrupt request signal output. • Pull-up resistor ON/OFF operation is programmable. • Resetting turns the pull-up resistors off.	C

*1 Because these pins reach high impedance immediately after resetting, some applications may require pin processing.

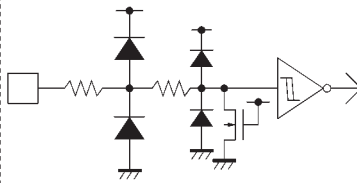| Pin No.	Pin name	I / O	Function	Type
21, 39	SIN0, SIN1	I	• 8-bit serial data input	A
22, 40	SIO0, SIO1	I / O	• 8-bit serial data input/output • Programmable for input or output	E
23, 41	SCK0, SCK1 （SIO04B block）	I / O	• Clock input/output for serial data transmission and reception • Programmable selection from among 3 internal clocks and 1 external clock	E
52～59	ADC0～ADC7 （ADC83A block）	I	• Analog data input • Each bit programmable for digital data input • Resetting returns all pins to analog input.	G
1～4 5～8 9～12 13～16 17～20	SEG00～03 SEG04～07 SEG08～11 SEG12～15 SEG16～19	O	• Programmable for LCD segment output or CMOS small-current output (set in 4-pin groups) • Resetting returns all pins to CMOS small-current output (LOW polarity output)	F
61～64	COM0～COM3 （LCD07A block）	O	• LCD common output • During 1/3 duty, COM3 outputs the ground level	F
32	PWC （PWC01A block）	I	• Pulse input	A
33, 34	T0, T1 （TMR03B block）	I	• External count clock input • Usable for 1-bit input	J
49	OSC1	I	• Oscillator input • External clock input	H
50	OSC2 （OSC03A block）	O	• Oscillator output	I
60	TEST	I	• Test input (This is a chip test pin that contains an internal pull-down resistor and so should normally remain open.)	B
47	$\overline{\text{RESET}}$	I	• Reset input (Setting this pin to LOW resets the CPU.)	A
51	V_{DD}	—	• Power supply	—
48	GND	—	• Ground	—

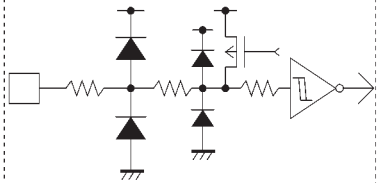**ROHM**

●Input / output circuits
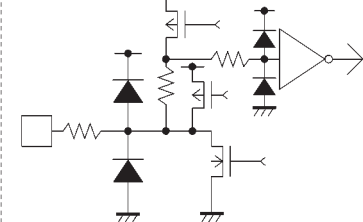
TYPE A

· Hysteresis input

TYPE B

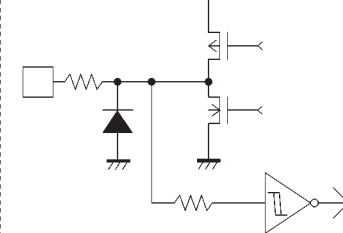· Hysteresis input of internal pull-down resistor

TYPE C

· Hysteresis input for programmable ON/OFF operation of pull-up resistor
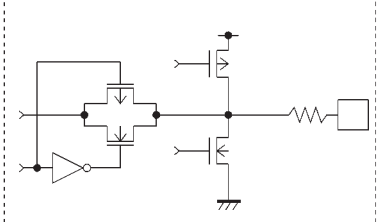
TYPE D

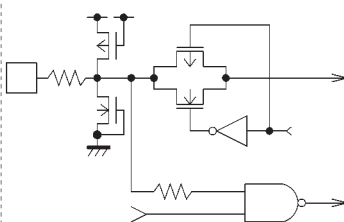· Pull-up resistor with programmable ON/OFF operation and normal input/output with Nch open drain output

TYPE E

· Hysteresis input with programmable control of CMOS output
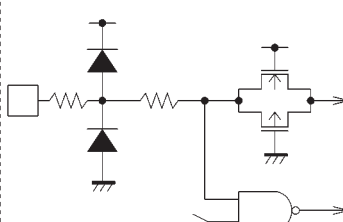
TYPE F

· LCD driver output
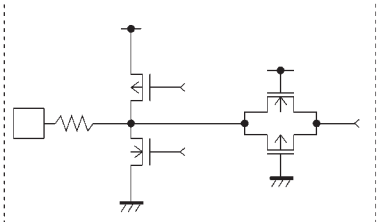 (CMOS output possible for SEG only)

TYPE G

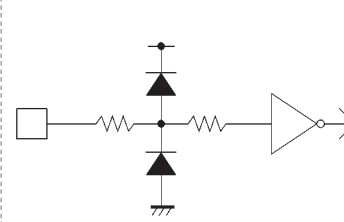· Programmable control of AD input with digital input

TYPE H

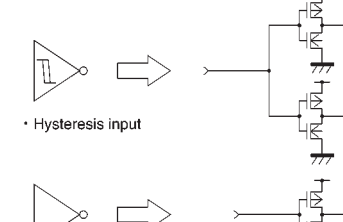· Input in feedback resistor with STOP control

TYPE I

· CMOS output in feedback resistor

TYPE J

· Hysteresis input

· Normal input

· Normal input

●Electrical characteristics (at 5V) (unless otherwise noted, Ta = 25°C, V_{DD} = 5V)

Parameter	Symbol	Pin	Min.	Typ.	Max.	Unit	Conditions
STOP circuit current	I_{DDST}		—	—	1	μA	• STOP mode
HALT circuit current	I_{DDHT}		—	1	—	mA	• HALT mode • f_{OSC} = 4.4MHz
Operating supply current	I_{DDOP}		—	4	—	mA	• f_{OSC} = 4.4MHz
Clock frequency	f_{OSC}	OSC1，OSC2	2	—	4.4	MHz	
Input high level voltage 1	V_{IH1}	P00~P03, P10~P13, P20~P23, T0, T1, ADC0~ADC7	3.5	—	—	V	• P = input • ADC = digital input
Input high level voltage 2	V_{IH2}	W0~W3, BIN, SIN0, SIN1, SIO0, SIO1, SCK0, SCK1, PWC, TEST, $\overline{RESET}$	3.75	—	—	V	• Hysteresis input • SIO, SCK = input
Input high level voltage 3	V_{IH3}	OSC1	3.9	—	—	V	• External clock input
Input low level voltage 1	V_{IL1}	P00~P03, P10~P13, P20~P23, T0, T1, ADC0~ADC7	—	—	1.5	V	• P = input • ADC = digital input
Input low level voltage 2	V_{IL2}	W0~W3, BIN, SIN0, SIN1, SIO0, SIO1, SCK0, SCK1, PWC, TEST, $\overline{RESET}$	—	—	1.25	V	• Hysteresis input • SIO, SCK = input
Input low level voltage 3	V_{IL3}	OSC1	—	—	1.1	V	• External clock input
Input high level current 1	I_{IH1}	P00~P03, P10~P13, P20~P23, W0~W3, BIN, SIN0, SIN1, SIO0, SIO1, SCK0, SCK1, ADC0~ADC7, PWC, T0, T1, $\overline{RESET}$	—	—	1	μA	• No pull-down resistor • P, SIO, SCK = input • V_{IN} = V_{DD}
Input high level current 2	I_{IH2}	TEST	35	70	140	μA	• Internal pull-down resistor • V_{IN} = V_{DD}
Input low level current 1	I_{IL1}	P00~P03, P10~P13, P20~P23, W0~W3, BIN, SIN0, SIN1, SIO0, SIO1, SCK0, SCK1, ADC0~ADC7, PWC, T0, T1, $\overline{RESET}$, TEST	—	—	−1	μA	• No pull-down resistor • P, SIO, SCK = input • V_{IN} = GND
Input low level current 2	I_{IL2}	P00~P03, P10~P13, P20~P23, W0~W3, BIN	−90	−125	−160	μA	• Internal pull-down resistor • V_{IN} = GND
Output high level voltage 1	V_{OH1}	SIO0, SIO1, SCK0, SCK1	4.5	—	—	V	• SIO, SCK = output • I_{OH} = −500μA
Output high level voltage 2	V_{OH2}	SEG00~SEG19, COM0~COM3	4.5	—	—	V	• I_{OH} = −250μA
Output low level voltage 1	V_{OL1}	P00~P03, P10~P13, P20~P23, SIO0, SIO1, SCK0, SCK1	—	—	0.4	V	• P,SIO,SCK = output • I_{OL} = 1.6mA
Output low level voltage 2	V_{OL2}	SEG00~SEG19, COM0~COM3	—	—	0.7	V	• I_{OL} = 1.0mA
Output leakage current	I_L	P00~P03, P10~P13, P20~P23	—	—	1	μA	• P = high -impedance output
OSC feedback current	I_{FO}	OSC1，OSC2	−4.0	−10	−14	μA	• Approx. 500 kΩ

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Parameter	Symbol	Pin	Min.	Typ.	Max.	Unit	Conditions
A/D conversion resolution	RES	ADC0~ADC7	—	8	—	bits	MC: machine cycle ✽
A/D conversion settling time	t_S	ADC0~ADC7	—	25	—	MC	
A/D conversion linearity error	E_L	ADC0~ADC7	—	—	±3	LSB	
LCD 2 / 3 level output voltage	V_1	COM0~COM3 SEG00~SEG19	—	2	—	V	
LCD 2 / 3 level output voltage	V_2	COM0~COM3 SEG00~SEG19	—	1	—	V	

✽ 1 machine cycle = 1/6 oscillation frequency

●Electrical characteristics (at 3V) (unless otherwise noted, Ta = 25°C, V_{DD} = 3V)

Parameter	Symbol	Pin	Min.	Typ.	Max.	Unit	Conditions
STOP circuit current	I_{DDST}		—	—	1	μA	• STOP mode
HALT circuit current	I_{DDHT}		—	0.4	—	mA	• HALT mode • f_{OSC} = 4.4MHz
Operating supply current	I_{DDOP}		—	1.5	—	mA	• f_{OSC} = 4.4MHz
Clock frequency	f_{OSC}	OSC1, OSC2	2	—	4.4	MHz	
Input high level voltage 1	V_{IH1}	P00~P03, P10~P13, P20~P23, T0, T1, ADC0~ADC7	2.1			V	• P = input • ADC = digital input
Input high level voltage 2	V_{IH2}	W0~W3, BIN, SIN0, SIN1, SIO0, SIO1, SCK0, SCK1, PWC, TEST, $\overline{RESET}$	2.25	—	—	V	• Hysteresis input • SIO, SCK = input
Input high level voltage 3	V_{IH3}	OSC1	2.4	—	—	V	• External clock input
Input low level voltage 1	V_{IL1}	P00~P03, P10~P13, P20~P23, T0, T1, ADC0~ADC7	—	—	0.9	V	• P = input • ADC = digital input
Input low level voltage 2	V_{IL2}	W0~W3, BIN, SIN0, SIN1, SIO0, SIO1, SCK0, SCK1, PWC, TEST, $\overline{RESET}$	—	—	0.75	V	• Hysteresis input • SIO, SCK = input
Input low level voltage 3	V_{IL3}	OSC1	—	—	0.65	V	• External clock input
Input high level current 1	I_{IH1}	P00~P03, P10~P13, P20~P23, W0~W3, BIN, SIN0, SIN1, SIO0 SIO1, SCK0, SCK1, ADC0~ADC7, PWC, T0 T1, $\overline{RESET}$	—	—	1	μA	• No pull-down resistor • P, SIO, SCK = input • V_{IN} = V_{DD}
Input high level current 2	I_{IH2}	TEST	10	20	35	μA	• Internal pull-down resistor • V_{IN} = V_{DD}
Input low level current 1	I_{IL1}	P00~P03, P10~P13, P20~P23, W0~W3, BIN, SIN0, SIN1, SIO0 SIO1, SCK0, SCK1, ADC0~ADC7, PWC, T0 T1, $\overline{RESET}$, TEST	—	—	−1	μA	• No pull-down resistor • P, SIO, SCK = input • V_{IN} = GND
Input low level current 2	I_{IL2}	P00~P03, P10~P13, P20~P23, W0~W3, BIN	−20	−40	−60	μA	• Internal pull-up resistor • V_{IN} = GND
Output high level voltage 1	V_{OH1}	SIO0, SIO1, SCK0, SCK1	2.5	—	—	V	• SIO, SCK = output • I_{OH} = −500μA
Output high level voltage 2	V_{OH2}	SEG00~SEG19, COM0~COM3	2.5	—	—	V	• I_{OH} = −250μA
Output low level voltage 1	V_{OL1}	P00~P03, P10~P13, P20~P23, SIO0, SIO1, SCK0, SCK1	—	—	0.6	V	• P,SIO,SCK = output • I_{OL} = 1.6mA
Output low level voltage 2	V_{OL2}	SEG00~SEG19, COM0~COM3	—	—	0.7	V	• I_{OL} = 0.8mA
Output leakage current	I_L	P00~P03, P10~P13, P20~P23	—	—	1	μA	• P = high-impedance output
OSC feedback current	I_{FO}	OSC1, OSC2	−1.5	−3	−5	μA	• Approx. 1 MΩ

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Parameter	Symbol	Pin	Min.	Typ.	Max.	Unit	Conditions
A/D conversion resolution	RES	ADC0~ADC7	—	8	—	bits	
A/D conversion settling time	t_s	ADC0~ADC7	—	25	—	MC	MC: machine cycle ∗
A/D conversion linearity error	E_L	ADC0~ADC7	—	—	±3	LSB	
LCD 2 / 3 level output voltage	V_1	COM0~COM3 SEG00~SEG19	—	2	—	V	
LCD 2 / 3 level output voltage	V_2	COM0~COM3 SEG00~SEG19	—	1	—	V	

∗ 1 machine cycle = 1/6 oscillation frequency

●Hardware descriptions

(1) Operates on a single power supply (V_{DD} = 2.7 ~ 5.5V)

(2) Memory size
ROM : 12288 × 8 bits
RAM : 512 × 4 bits
LCD display RAM : 20 × 4 bits

(3) Instruction execution time (1 cycle instruction)
1.5μsec: (at 4MHz)

(4) Subroutine nesting : 8 levels

(5) Interrupts : 6 factors
External : 3 factors
Internal (time counter, serial I / O) : 3 factors

(6) ROM data table function (data table area: 12KB)

(7) Two energy-saving modes (STOP / HALT)

(8) Internal 20-segment LCD driver adaptable for various types of displays
Bias : 1 / 3
Duty settings : 1 / 3, 1 / 4 (programmable)
Internal bias resistor (3 stages, approx. 50kΩ)

(9) LCD segment output is program-switchable to CMOS output
All 20 segments can be selected in 4-bit groups
Resetting: CMOS small-current output port, LOW polarity

(10) Internal remote control receiver (pulse width counter)

(11) Internal 8-channel, 8-bit A / D converter

(12) A / D input is programmable in 1-bit units as digital input

(13) Internal 8-bit timer counter (also used as event counter)

(14) Two internal serial input / outputs (LSB fast) that simplify interface with external LSI chips

(15) 12 input / outputs (programmable pull-up)

(16) 5 inputs (programmable pull-up)

●External dimensions (Units: mm)

QFP-A64