BUJ103A

Silicon diffused power transistor

Rev. 4 — 8 November 2011 **Product data sheet**

1. Product profile

1.1 General description

High-voltage, high-speed planar-passivated NPN power switching transistor in a SOT78 (TO-220AB) plastic package.

1.2 Features and benefits

- Low thermal resistance
- Fast switching

1.3 Applications

- Electronic lighting ballasts
- Inverters
- DC-to-DC converters
- Motor control systems

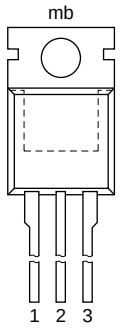
1.4 Quick reference data

- $V_{CESM} \leq 700$ V
- $P_{tot} \leq 80$ W
- $I_C \leq 4$ A
- $h_{FEsat} = 12.5$ (typ)

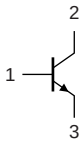
2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Symbol
1	base		
2	collector		
3	emitter		
mb	mounting base; connected to collector		



SOT78 (TO-220AB)



sym056

3. Ordering information

Table 2. Ordering information

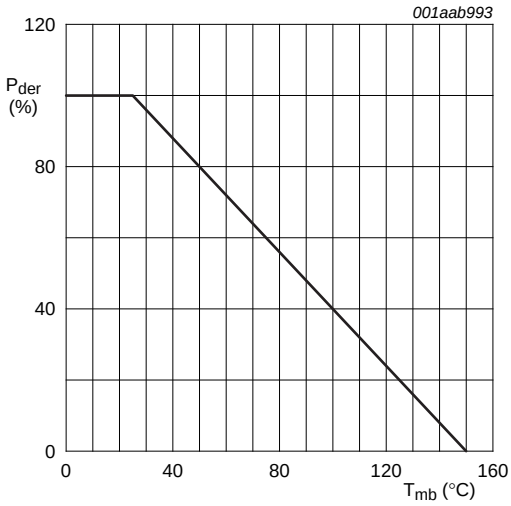
Type number	Package		
	Name	Description	Version
BUJ103A	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-leads	SOT78

4. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CESM}	peak collector-emitter voltage	V_{BE} = 0 V	-	700	V
V_{CBO}	collector-base voltage	open emitter	-	700	V
V_{CEO}	collector-emitter voltage	open base	-	400	V
I_C	collector current (DC)		-	4	A
I_{CM}	peak collector current		-	8	A
I_B	base current (DC)		-	2	A
I_{BM}	peak base current		-	4	A
P_{tot}	total power dissipation	$T_{mb} \leq 25$ °C; see Figure 1	-	80	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	150	°C



$$P_{der}(\%) = \frac{P_{tot}}{P_{tot(25\ °C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature

5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	see Figure 2	-	-	1.56	K/W
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient	in free air	-	60	-	K/W

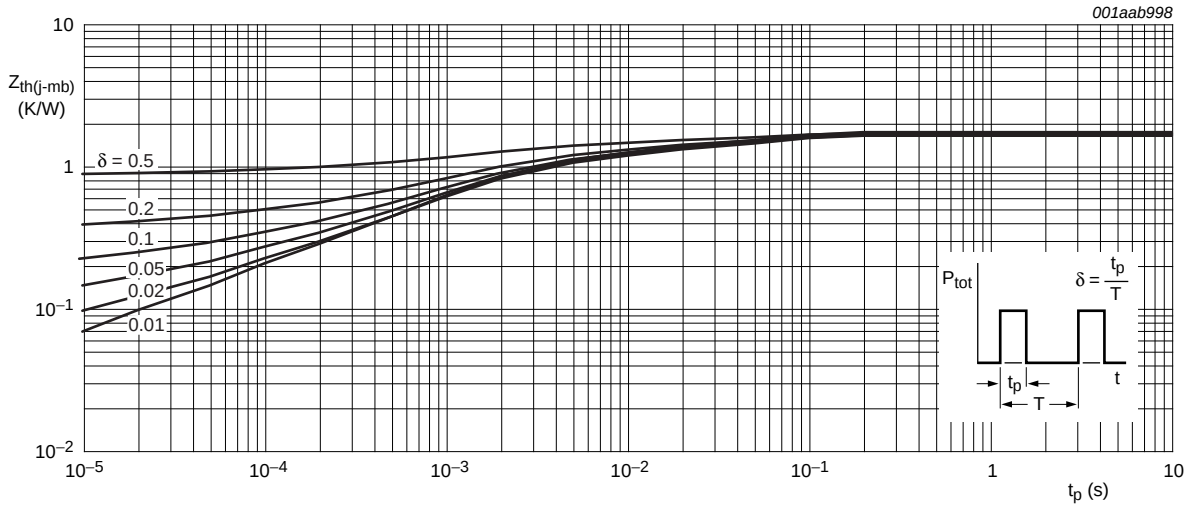


Fig 2. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 5. Characteristics

T_{mb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{CES}	collector-emitter cut-off current	V_{BE} = 0 V; V_{CE} = $V_{CESMmax}$	[1]	-	-	1	mA
		V_{BE} = 0 V; V_{CE} = $V_{CESMmax}$; T_j = 125 °C	[1]	-	-	2	mA
I_{CBO}	collector-base cut-off current	V_{BE} = 0 V; V_{CE} = $V_{CESMmax}$	[1]	-	-	1	mA
I_{CEO}	collector-emitter cut-off current	V_{CEO} = $V_{CEOMmax}$ = 400 V	[1]	-	-	0.1	mA
I_{EBO}	emitter-base cut-off current	V_{EB} = 7 V; I_C = 0 A		-	-	0.1	mA
V_{CEOsus}	collector-emitter sustaining voltage	I_B = 0 A; I_C = 10 mA; L = 25 mH; see Figure 3 and 4		400	-	-	V
V_{CEsat}	collector-emitter saturation voltage	I_C = 3.0 A; I_B = 0.6 A; see Figure 10		-	0.25	1	V
V_{BEsat}	base-emitter saturation voltage	I_C = 3.0 A; I_B = 0.6 A; see Figure 11		-	0.97	1.5	V
h_{FE}	DC current gain	I_C = 1 mA; V_{CE} = 5 V; see Figure 9		10	17	32	
		I_C = 500 mA; V_{CE} = 5 V		13	22	32	
h_{FEsat}	DC saturation current gain	I_C = 2.0 A; V_{CE} = 5 V		11	16	22	
		I_C = 3.0 A; V_{CE} = 5 V		-	12.5	-	
Dynamic characteristics							
Switching times (resistive load); see Figure 5 and 6							
t_{on}	turn-on time	I_{Con} = 2.5 A; I_{Bon} = $-I_{Boff}$ = 0.5 A; R_L = 75 Ω		-	0.52	0.6	µs
t_{stg}	storage time			-	2.7	3.3	µs
t_f	fall time			-	0.3	0.35	µs
Switching times (inductive load); see Figure 7 and 8							
t_{stg}	storage time	I_{Con} = 2 A; I_{Bon} = 0.4 A; L_B = 1 µH; V_{BB} = −5 V		-	1.2	1.4	µs
t_f	fall time			-	30	60	ns
Switching times (inductive load); see Figure 7 and 8							
t_{stg}	storage time	I_{Con} = 2 A; I_{Bon} = 0.4 A; L_B = 1 µH; V_{BB} = −5 V; T_j = 100 °C		-	-	1.8	µs
t_f	fall time			-	-	120	ns

[1] Measured with half sine-wave voltage (curve tracer).

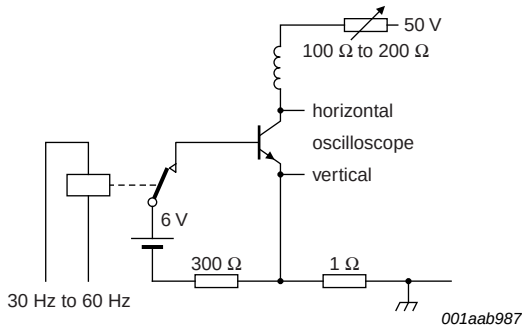


Fig 3. Test circuit for collector-emitter sustaining voltage

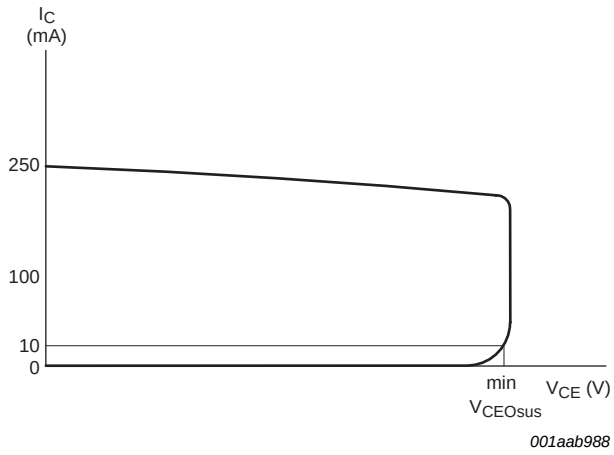
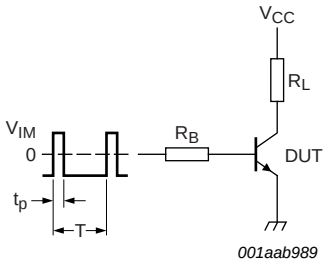


Fig 4. Oscilloscope display for collector-emitter sustaining voltage test waveform



V_{IM} = −6 V to +8 V; V_{CC} = 250 V; t_p = 20 μs;
$\delta = t_p/T = 0.01$.

R_B and R_L calculated from I_{Con} and I_{Bon} requirements.

Fig 5. Test circuit for resistive load switching

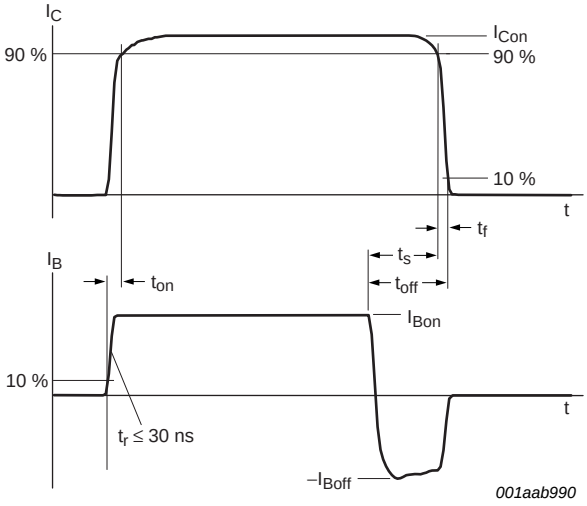
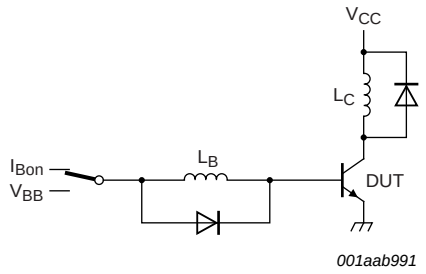


Fig 6. Switching times waveforms for resistive load



V_{CC} = 300 V; V_{BB} = −5 V; L_C = 200 μH; L_B = 1 μH.

Fig 7. Test circuit for inductive load switching

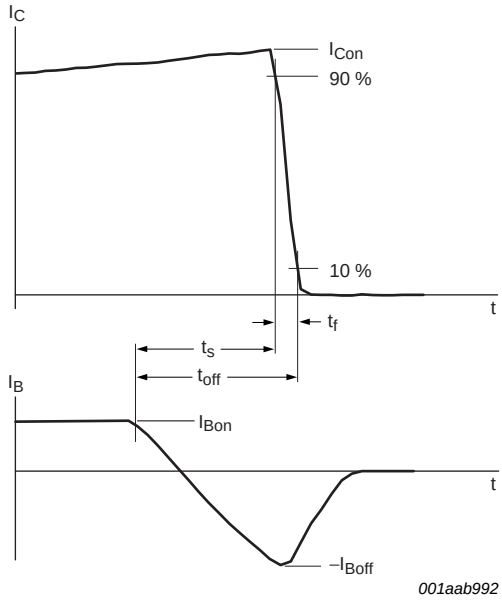


Fig 8. Switching times waveforms for inductive load

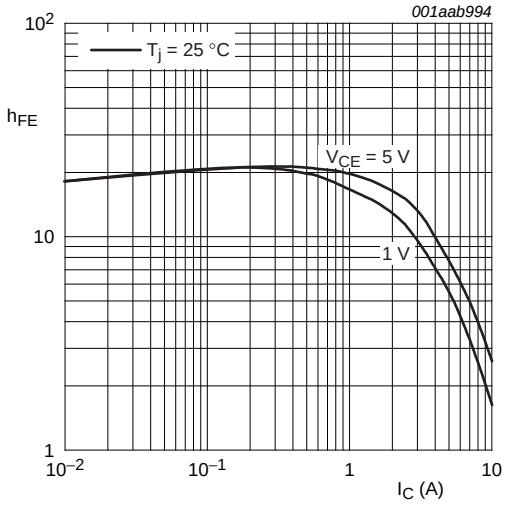
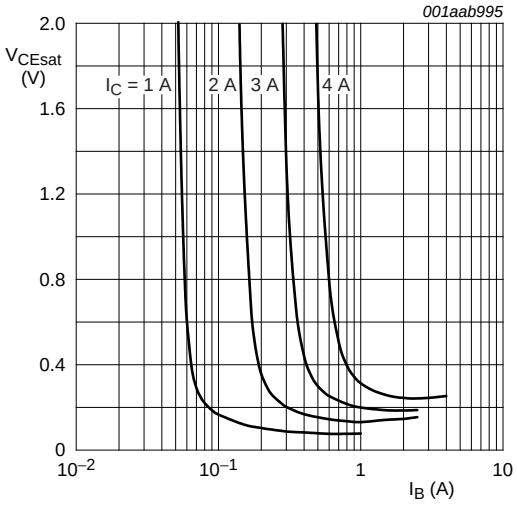
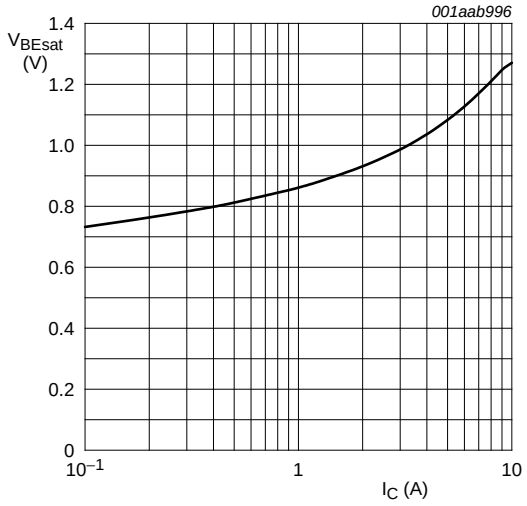


Fig 9. DC current gain as a function of collector current; typical values



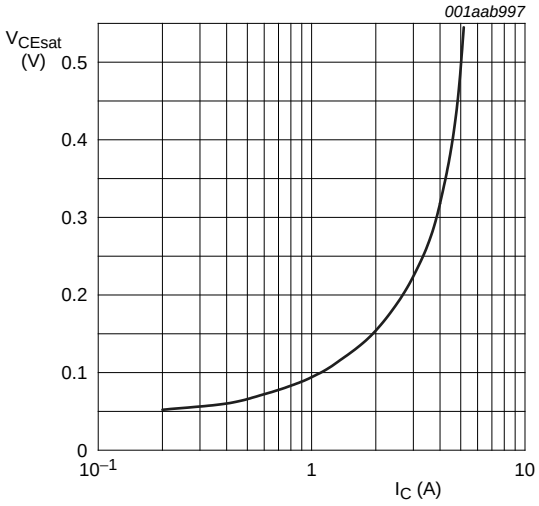
T_j = 25 °C.

Fig 10. Collector-emitter saturation voltage as a function of base current; typical values



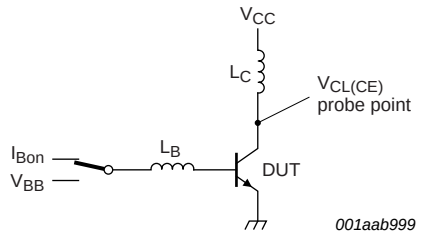
$I_C/I_B = 4$.

Fig 11. Base-emitter saturation voltage as a function of collector current; typical values



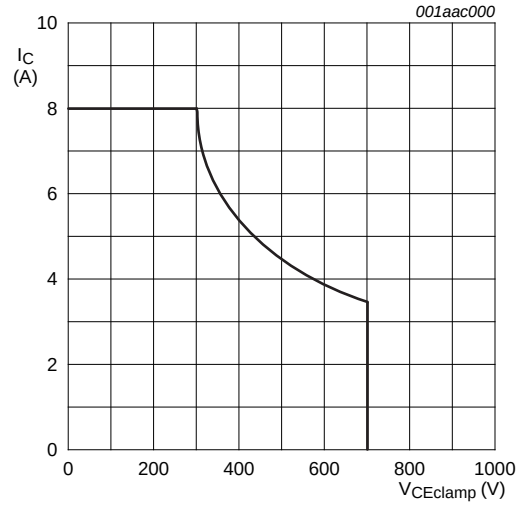
$I_C/I_B = 4$.

Fig 12. Collector-emitter saturation voltage as a function of collector current; typical values



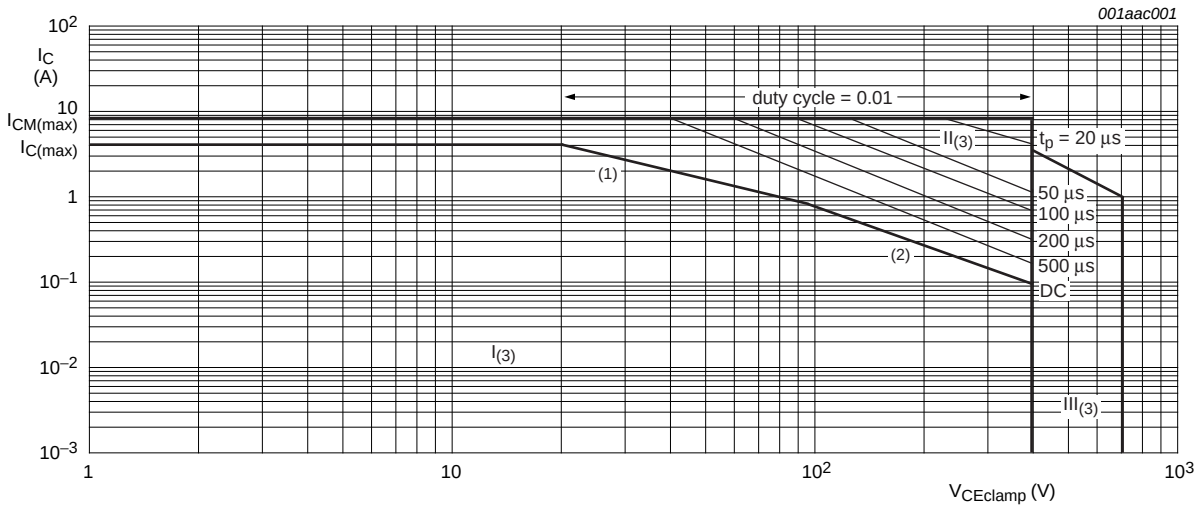
$V_{CEclamp} \leq 1000$ V; $V_{CC} = 150$ V; $V_{BB} = -5$ V; $L_B = 1$ μH; $L_C = 200$ μH.

Fig 13. Test circuit for reverse bias safe operating area



$T_j \leq T_{j(max)}$.

Fig 14. Reverse bias safe operating area



$T_{mb} \leq 25$ °C; Mounted with heatsink compound and 30 ± 5 Newton force on the center of the envelope.

(1) P_{tot} maximum and P_{tot} peak maximum lines.

(2) Second breakdown limits.

(3) I = Region of permissible DC operation.

II = Extension for repetitive pulse operation.

III = Extension during turn-on in single transistor converters provided that $R_{BE} \leq 100\ \Omega$ and $t_p \leq 0.6\ \mu s$.

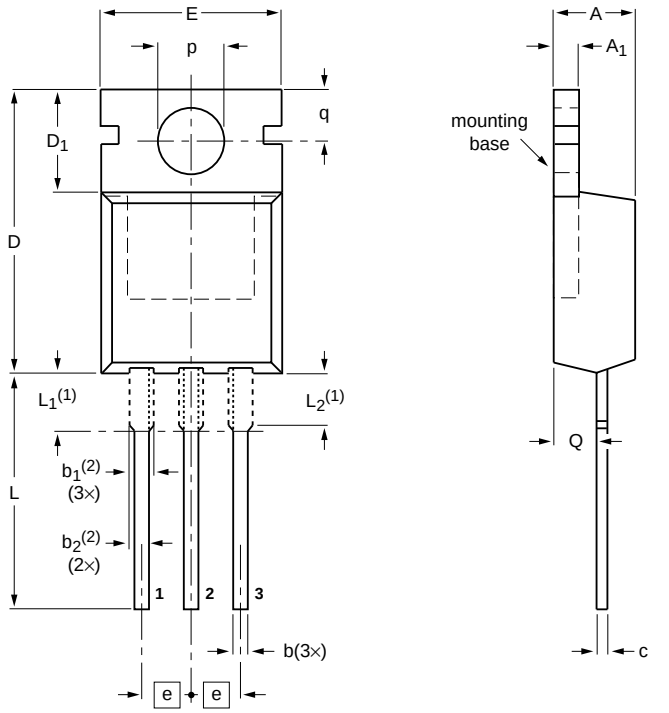
Fig 15. Forward bias safe operating area

7. Package information

Epoxy meets requirements of UL94 V-0 at $^1/_8$ inch.

8. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB **SOT78**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1(2)	b_2(2)	c	D	D_1	E	e	L	L_1(1)	L_2(1) max.	p	q	Q
mm	4.7 4.1	1.40 1.25	0.9 0.6	1.6 1.0	1.3 1.0	0.7 0.4	16.0 15.2	6.6 5.9	10.3 9.7	2.54	15.0 12.8	3.30 2.79	3.0	3.8 3.5	3.0 2.7	2.6 2.2

Notes

1. Lead shoulder designs may vary.
2. Dimension includes excess dambar.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT78		3-lead TO-220AB	SC-46			~~08-04-23~~ 08-06-13

Fig 16. Package outline SOT78 (TO-220AB)

9. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUJ103A v.4	20111108	Product data sheet	-	BUJ103A v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
BUJ103A v.3	20050303	Product data sheet	-	BUJ103A_HG v.2
BUJ103A_HG v.2	19980918	Product data sheet	-	BUJ103A v.1
BUJ103A v.1	19980801	Product data sheet	-	-

10. Legal information

10.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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