BUJ302AX

NPN power transistor

9 October 2018 | Product data sheet

1. General description

High voltage, high speed planar passivated NPN power switching transistor in a SOT186A (TO-220F) "full pack" plastic package.

2. Features and benefits

- Fast switching
- Isolated package
- Low thermal resistance
- Very high voltage capability
- Very low switching and conduction losses

3. Applications

- DC-to-DC converters
- High frequency electronic lighting ballasts
- Inverters
- Motor control systems

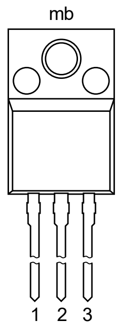
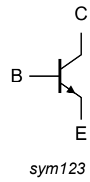
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{CM}	peak collector current	Fig. 1; Fig. 2; Fig. 3		-	-	8	A
P_{tot}	total power dissipation	$T_h \leq$ 25 °C; Fig. 4		-	-	26	W
V_{CESM}	collector-emitter peak voltage	V_{BE} = 0 V		-	-	1050	V
Static characteristics							
h_{FE}	DC current gain	I_C = 0.1 A; V_{CE} = 5 V; T_h = 25 °C; Fig. 11		48	66	100	
		I_C = 0.8 A; V_{CE} = 3 V; T_h = 25 °C; Fig. 12		25	42	50	

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	B	base	 TO-220F (SOT186A)	
2	C	collector		
3	E	emitter		
mb	n.c.	isolated		

6. Ordering information

Table 3. Ordering information

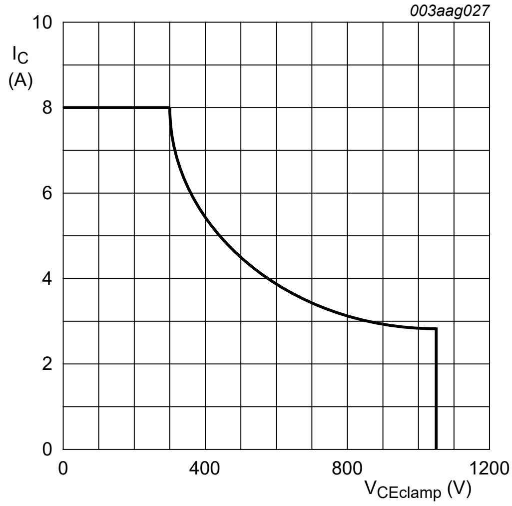
Type number	Package		
	Name	Description	Version
BUJ302AX	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A

7. Limiting values

Table 4. Limiting values

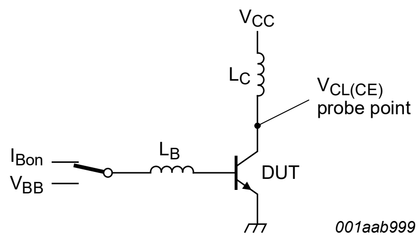
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CESM}	collector-emitter peak voltage	$V_{BE} = 0$ V		-	1050	V
V_{CEO}	collector-emitter voltage	$I_B = 0$ A		-	400	V
V_{EBO}	emitter-base voltage	$I_C = 0$ A; $I_E = 2$ A; $t_p < 10$ ms		-	24	V
I_C	collector current	Fig. 1; Fig. 2; Fig. 3		-	4	A
I_{CM}	peak collector current			-	8	A
I_B	base current	DC		-	2	A
I_{BM}	peak base current			-	4	A
P_{tot}	total power dissipation	$T_h \leq$ 25 °C; Fig. 4		-	26	W
T_{stg}	storage temperature			-65	150	°C
T_j	junction temperature			-	150	°C



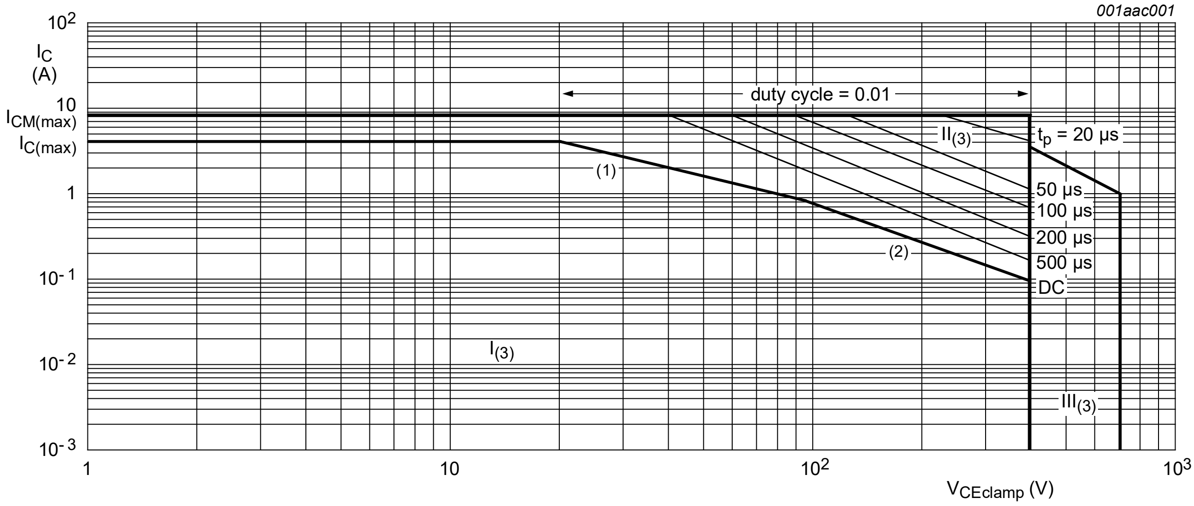
$T_j \leq T_{j(max)}$ °C

Fig. 1. Reverse bias safe operating area



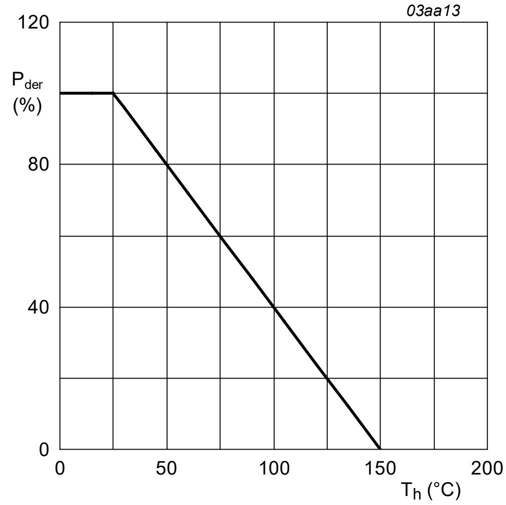
$V_{CL(CE)} \leq 1000$ V; $V_{CC} = 150$ V; $V_{BB} = -5$ V;
$L_B = 1$ µH; $L_C = 200$ µH

Fig. 2. Test circuit for reverse bias safe operating area



1) P_{tot} maximum and P_{tot} peak maximum lines
2) Second breakdown limits
3) I = Region of permissable DC operation
II = Extension for repetitive pulse operation
III = Extension during turn-on in single transistor converters provided that $R_{BE} \leq 100\ \Omega$ and $t_p \leq 0.6$ µs

Fig. 3. Forward bias safe operating area for $T_{mb} \leq 25$ °C



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 4. Normalized total power dissipation as a function of heatsink temperature

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	with heatsink compound; Fig. 5		-	-	4.8	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	in free air		-	55	-	K/W

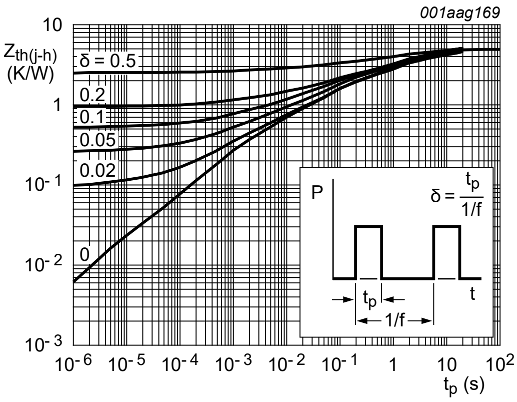


Fig. 5. Transient thermal impedance from junction to heatsink as a function of pulse duration

9. Isolation characteristics

Table 6. Isolation characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	50 Hz ≤ f ≤ 60 Hz; RH ≤ 65 %; T_h = 25 °C; from all terminals to external heatsink; clean and dust free		-	-	2500	V
C_{isol}	isolation capacitance	from collector to external heatsink; f = 1 MHz; T_h = 25 °C		-	10	-	pF

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{CES}	collector-emitter cut-off current (base shorted)	V_{BE} = 0 V; V_{CE} = 1050 V; T_j = 25 °C		-	0.2	10	µA
I_{CEO}	collector-emitter cut-off current (base open)	V_{CE} = 400 V; I_B = 0 A; T_h = 25 °C		-	10	250	µA
$V_{(BR)EBO}$	emitter-base breakdown voltage (collector open)	I_B = 1 mA; I_C = 0 A; T_h = 25 °C		15	19	-	V
V_{CEOsus}	collector-emitter sustaining voltage (base open)	I_B = 0 A; I_C = 10 mA; L_C = 25 mH; T_h = 25 °C; Fig. 6; Fig. 7		400	470	-	V
V_{CEsat}	collector-emitter saturation voltage	I_C = 1 A; I_B = 0.2 A; T_h = 25 °C; Fig. 8; Fig. 9		-	0.15	0.5	V
		I_C = 3.5 A; I_B = 1 A; T_h = 25 °C; Fig. 8; Fig. 9		-	0.6	1.5	V
V_{BEsat}	base-emitter saturation voltage	I_C = 3.5 A; I_B = 1 A; T_h = 25 °C; Fig. 10		-	1.1	1.5	V
h_{FE}	DC current gain	I_C = 0.1 A; V_{CE} = 5 V; T_h = 25 °C; Fig. 11		48	66	100	
		I_C = 0.8 A; V_{CE} = 3 V; T_h = 25 °C; Fig. 12		25	42	50	
Dynamic characteristics							
t_s	storage time	I_C = 2.5 A; I_{Bon} = 0.5 A; I_{Boff} = -0.5 A; R_L = 60 Ω; V_{BB} = -5 V; T_h = 25 °C; resistive load; t_p = 300 µs; Fig. 13; Fig. 14		-	-	3.5	µs
t_f	fall time			-	-	500	ns

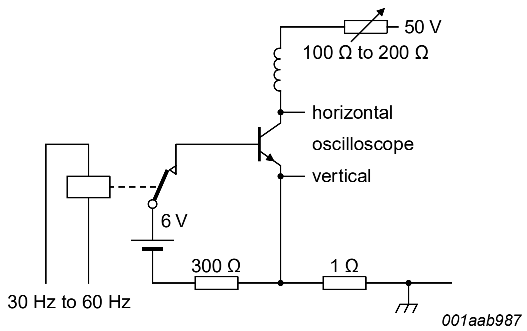


Fig. 6. Test circuit for collector-emitter sustaining voltage

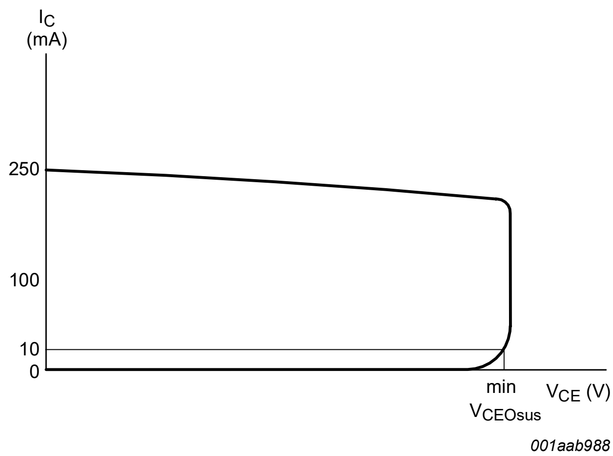


Fig. 7. Oscilloscope display for collector-emitter sustaining voltage test waveform

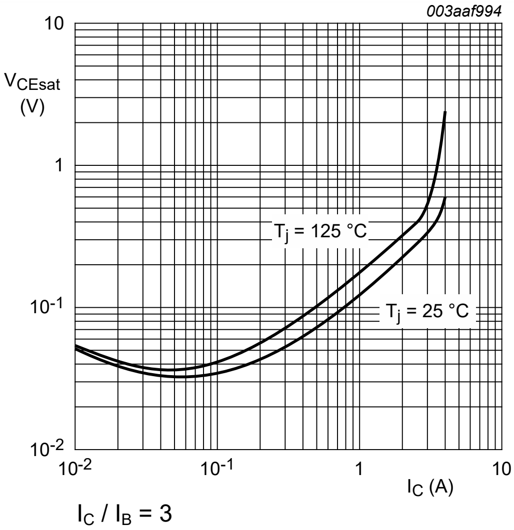


Fig. 8. Collector-emitter saturation voltage as a function of collector current; typical values

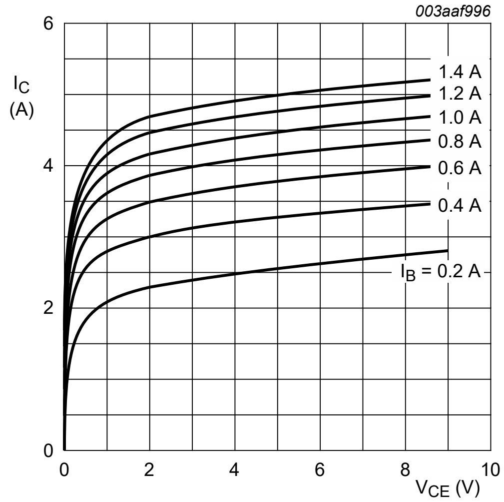


Fig. 9. Collector current as a function of collector-emitter voltage; typical values

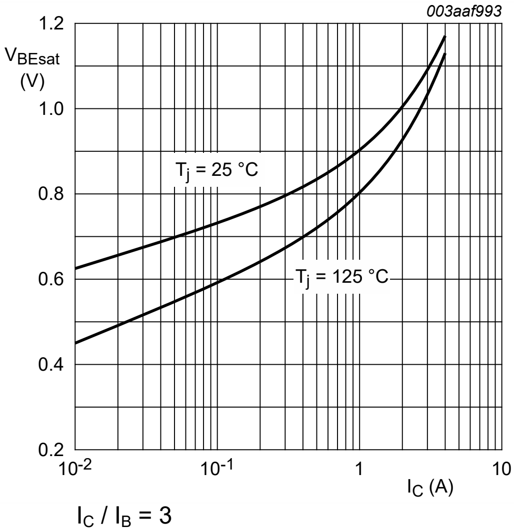


Fig. 10. Base-emitter saturation voltage as a function of collector current; typical values

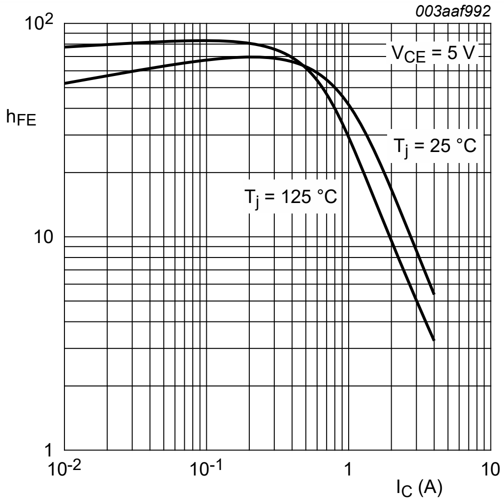


Fig. 11. DC current gain as a function of collector current; typical values

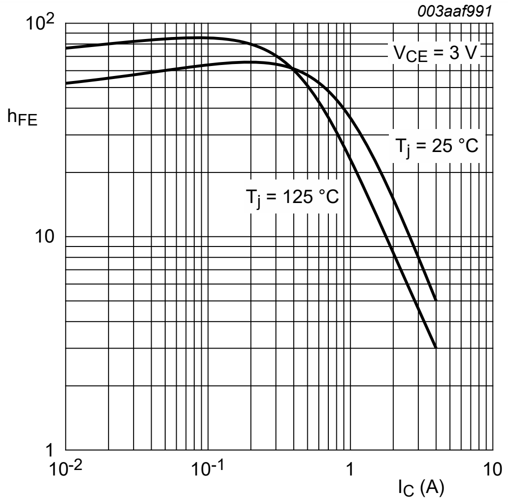
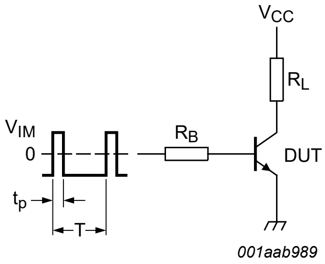


Fig. 12. DC current gain as a function of collector current; typical values



V_{IM}= - 6 to + 8 V; V_{CC} = 250 V; t_p = 20 us; δ = t_p/T = 0.01

R_B and R_L calculated from I_{Con} and I_{Bon} requirements.

Fig. 13. Test circuit for resistive load switching

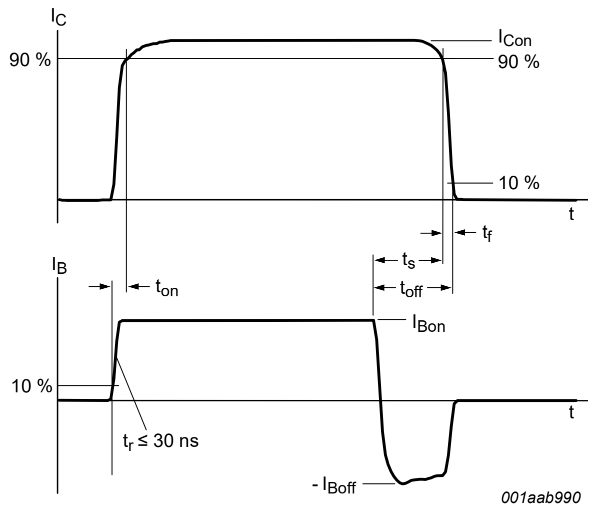
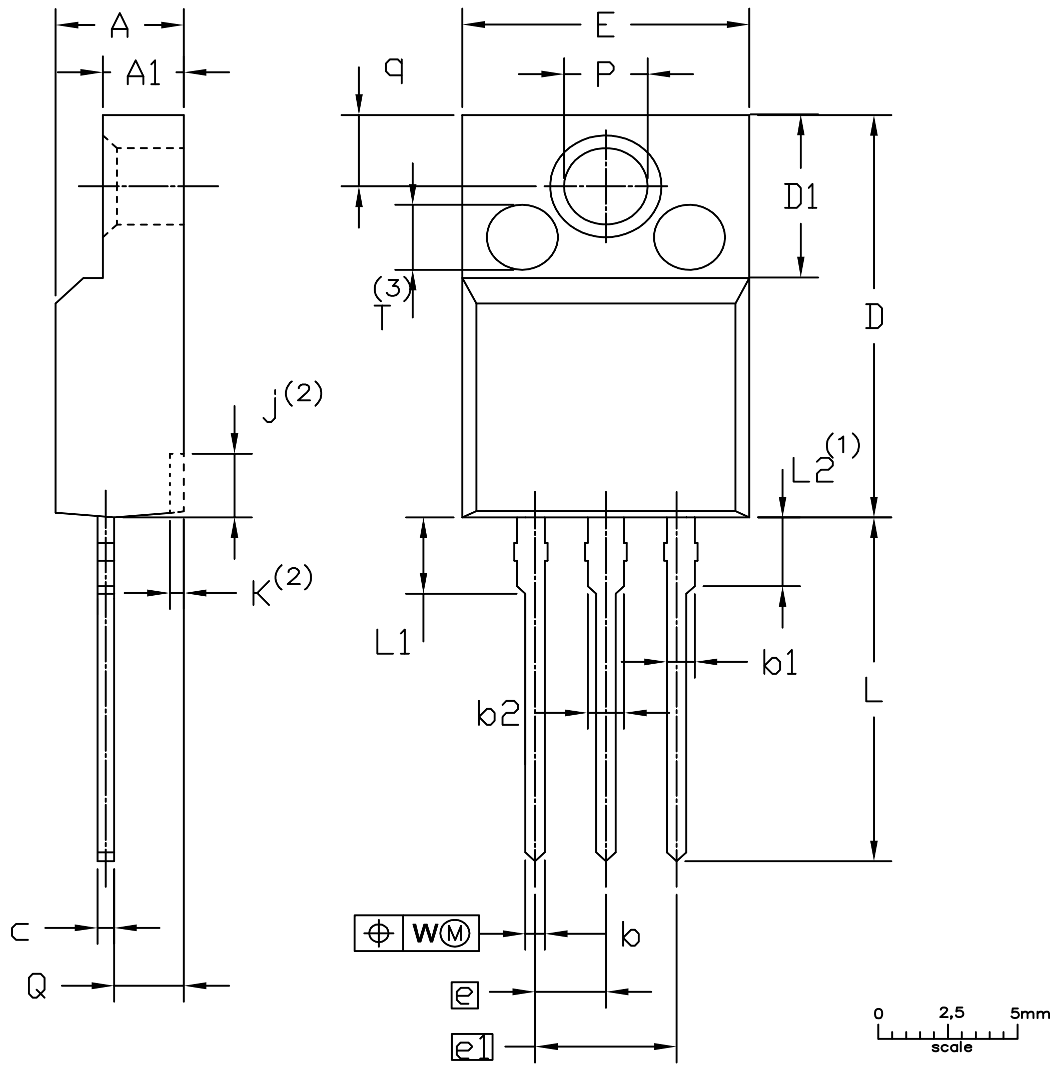


Fig. 14. Switching times waveforms for resistive load

11. Package outline

Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack" SOT186A



UNIT	A	A_1	b	b_1	b_2	c	D	D_1	E	e	e_1	j(2)	K(2)	L	L_1	L_2(1) max.	P	Q	q	W	T(3)
mm	4.6 4.0	2.9 2.5	0.9 0.7	1.1 0.9	1.4 1.0	0.7 0.4	15.8 15.2	6.5 6.3	10.3 9.7	2.54	5.08	2.7 1.7	0.6 0.4	14.4 13.5	3.30 2.79	3	3.2 3.0	2.6 2.3	3.0 2.6	0.4	2.5

Notes
1. Terminal dimensions within this zone are uncotrolled
2. Dot lines area designs may vary
3. Eject pin mark is for reference only

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT186A		3 LEADS TO220F				2013-11-14

Fig. 15. Package outline TO-220F (SOT186A)

12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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