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BUL45*
BUL45F*

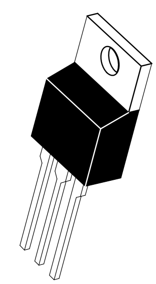
*Motorola Preferred Device

Designer's™ Data Sheet
NPN Silicon Power Transistor
High Voltage SWITCHMODE™ Series

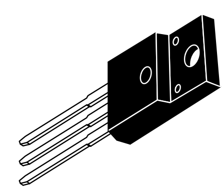
POWER TRANSISTOR
5.0 AMPERES
700 VOLTS
35 and 75 WATTS

Designed for use in electronic ballast (light ballast) and in Switchmode Power supplies up to 50 Watts. Main features include:

- Improved Efficiency Due to:
  — Low Base Drive Requirements (High and Flat DC Current Gain h_{FE})
  — Low Power Losses (On–State and Switching Operations)
  — Fast Switching: t_{fi} = 100 ns (typ) and t_{si} = 3.2 µs (typ)
  @ I_C = 2.0 A, I_{B1} = I_{B2} = 0.4 A
- Full Characterization at 125°C
- Tight Parametric Distributions Consistent Lot–to–Lot
- BUL45F, Case 221D, is UL Recognized at 3500 V_{RMS}: File #E69369



BUL45
CASE 221A–06
TO–220AB



BUL45F
CASE 221D–02
ISOLATED TO–220 TYPE
UL RECOGNIZED

MAXIMUM RATINGS

Rating	Symbol	BUL45	BUL45F	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	400		Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	700		Vdc
Emitter–Base Voltage	V_{EBO}	9.0		Vdc
Collector Current — Continuous — Peak(1)	I_C I_{CM}	5.0 10		Adc
Base Current	I_B	2.0		Adc
RMS Isolated Voltage(2) Test No. 1 Per Fig. 22a (for 1 sec, R.H. < 30%, Test No. 2 Per Fig. 22b T_C = 25°C) Test No. 3 Per Fig. 22c	V_{ISOL}	— — —	4500 3500 1500	Volts
Total Device Dissipation (T_C = 25°C) Derate above 25°C	P_D	75 0.6	35 0.28	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	– 65 to 150		°C

THERMAL CHARACTERISTICS

Rating	Symbol	MJE18006	MJF18006	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.65 62.5	3.55 62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)	$V_{CEO(sus)}$	400	—	—	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)	I_{CEO}	—	—	100	µAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0) (T_C = 125°C)	I_{CES}	— —	— —	10 100	µAdc
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)	I_{EBO}	—	—	100	µAdc

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.
(2) Proper strike and creepage distance must be provided.

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Base–Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.2 Adc)	$V_{BE(sat)}$	—	0.84	1.2	Vdc
(I_C = 2.0 Adc, I_B = 0.4 Adc)		—	0.89	1.25	
Collector–Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.2 Adc)	$V_{CE(sat)}$	—	0.175	0.25	Vdc
(T_C = 125°C)		—	0.150	—	
Collector–Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 0.4 Adc)	$V_{CE(sat)}$	—	0.25	0.4	Vdc
(T_C = 125°C)		—	0.275	—	
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	14	—	34	—
(T_C = 125°C)		—	32	—	
(I_C = 2.0 Adc, V_{CE} = 1.0 Vdc)		7.0	14	—	
(T_C = 125°C)		5.0	12	—	
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc)		10	22	—	
DYNAMIC CHARACTERISTICS					
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	—	12	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	50	75	pF
Input Capacitance (V_{EB} = 8.0 Vdc)	C_{ib}	—	920	1200	pF
Dynamic Saturation Voltage: Determined 1.0 µs and 3.0 µs respectively after rising I_{B1} reaches 90% of final I_{B1} (see Figure 18) — (I_C = 1.0 Adc, I_{B1} = 100 mAdc, V_{CC} = 300 V) 1.0 µs	V_{CE} (Dyn sat)	—	1.75	—	Vdc
(T_C = 125°C)		—	4.4	—	
3.0 µs		—	0.5	—	
(T_C = 125°C)		—	1.0	—	
(I_C = 2.0 Adc, I_{B1} = 400 mAdc, V_{CC} = 300 V) 1.0 µs		—	1.85	—	
(T_C = 125°C)		—	6.0	—	
3.0 µs		—	0.5	—	
(T_C = 125°C)		—	1.0	—	
SWITCHING CHARACTERISTICS: Resistive Load					
Turn–On Time (I_C = 2.0 Adc, I_{B1} = I_{B2} = 0.4 Adc, Pulse Width = 20 µs, Duty Cycle < 20%, V_{CC} = 300 V)	t_{on}	—	75	110	ns
(T_C = 125°C)		—	120	—	
Turn–Off Time	t_{off}	—	2.8	3.5	µs
(T_C = 125°C)		—	3.5	—	
SWITCHING CHARACTERISTICS: Inductive Load (V_{CC} = 15 Vdc, L_C = 200 µH, V_{clamp} = 300 Vdc)					
Fall Time (I_C = 2.0 Adc, I_{B1} = 0.4 Adc, I_{B2} = 0.4 Adc)	t_{fi}	70	—	170	ns
(T_C = 125°C)		—	200	—	
Storage Time	t_{si}	2.6	—	3.8	µs
(T_C = 125°C)		—	4.2	—	
Crossover Time	t_c	—	230	350	ns
(T_C = 125°C)		—	400	—	
Fall Time (I_C = 1.0 Adc, I_{B1} = 100 mAdc, I_{B2} = 0.5 Adc)	t_{fi}	—	110	150	ns
(T_C = 125°C)		—	100	—	
Storage Time	t_{si}	—	1.1	1.7	µs
(T_C = 125°C)		—	1.5	—	
Crossover Time	t_c	—	170	250	ns
(T_C = 125°C)		—	170	—	
Fall Time (I_C = 2.0 Adc, I_{B1} = 250 mAdc, I_{B2} = 2.0 Adc) (T_C = 125°C)	t_{fi}	—	80	120	ns
Storage Time (T_C = 125°C)	t_{si}	—	0.6	0.9	µs
Crossover Time (T_C = 125°C)	t_c	—	175	300	ns

TYPICAL STATIC CHARACTERISTICS

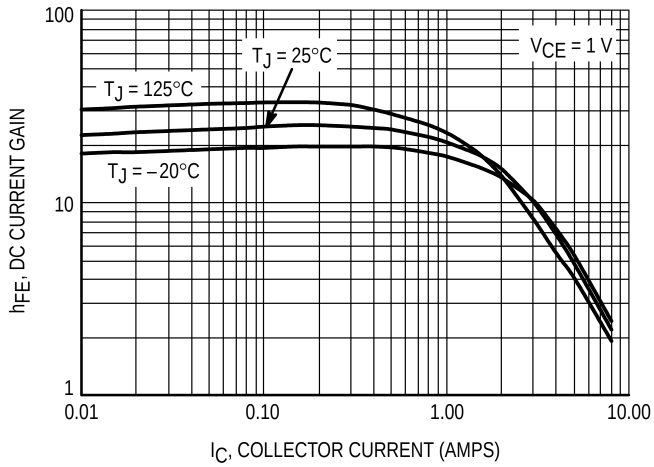


Figure 1. DC Current Gain @ 1 Volt

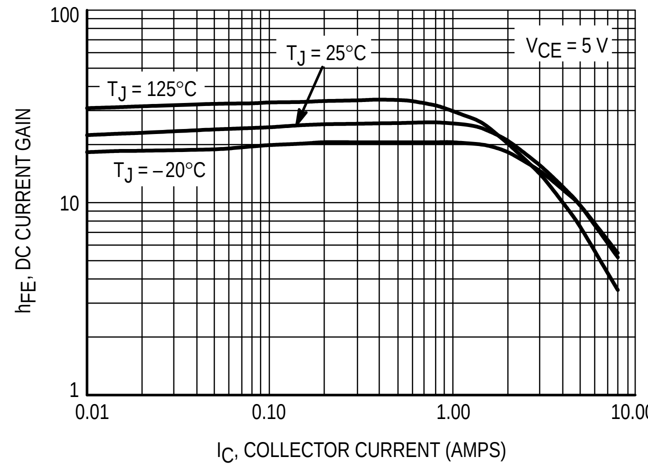


Figure 2. DC Current Gain at @ 5 Volts

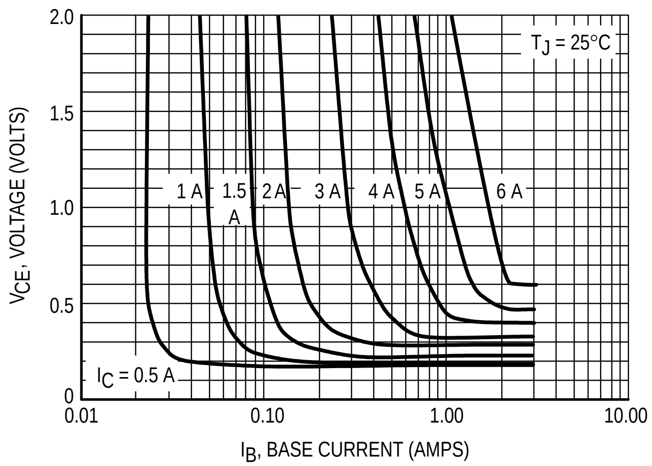


Figure 3. Collector–Emitter Saturation Region

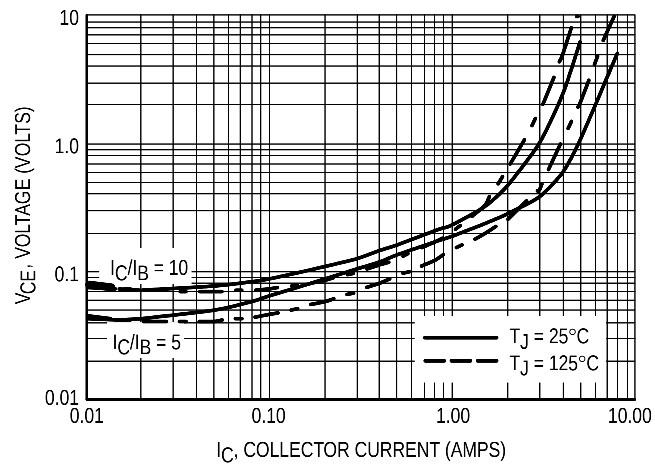


Figure 4. Collector–Emitter Saturation Voltage

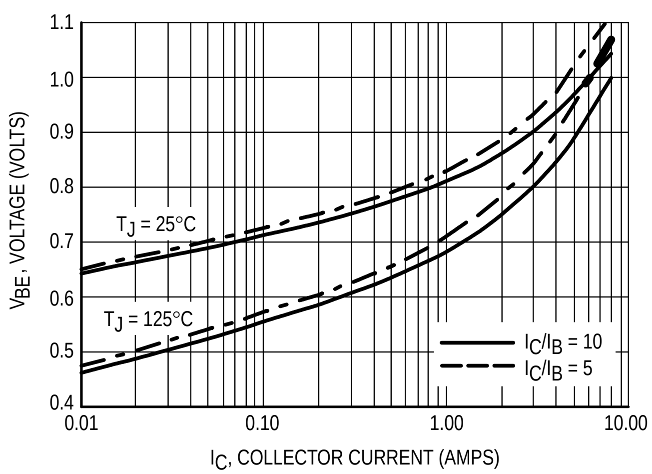


Figure 5. Base–Emitter Saturation Region

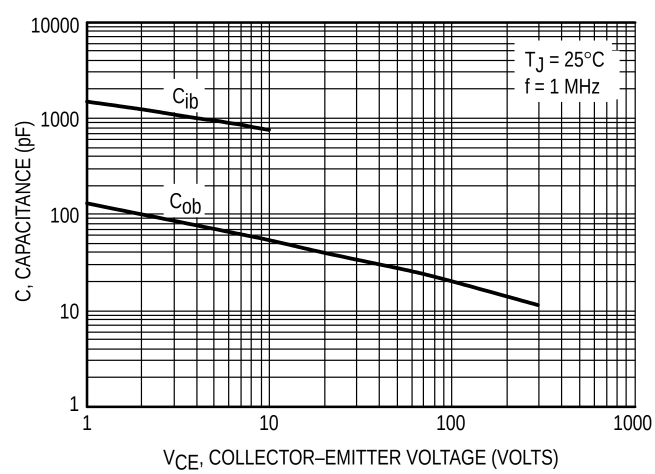


Figure 6. Capacitance

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

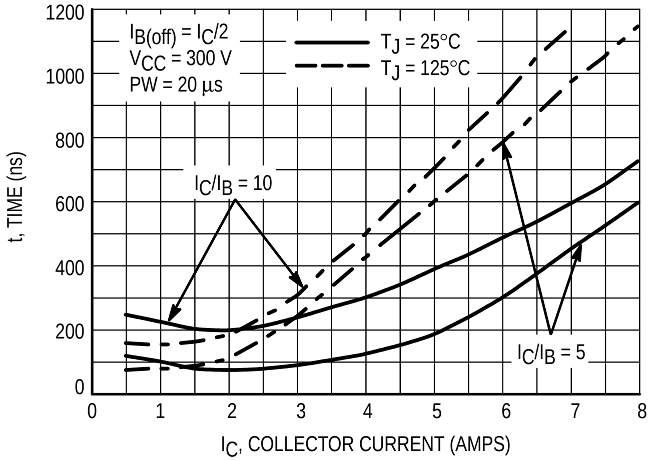


Figure 7. Resistive Switching, t_{on}

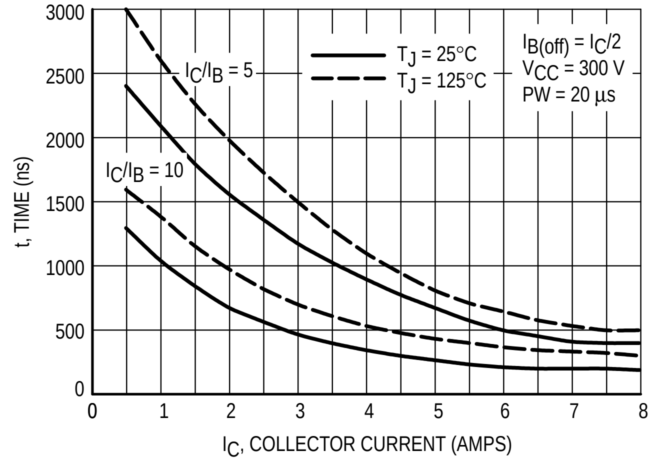


Figure 8. Resistive Switching, t_{off}

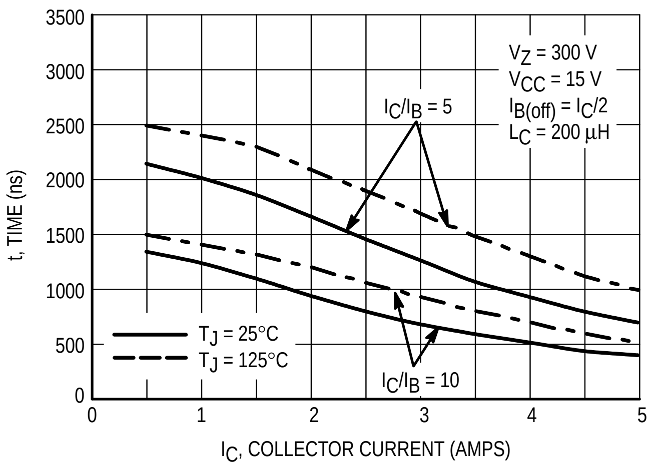


Figure 9. Inductive Storage Time, t_{si}

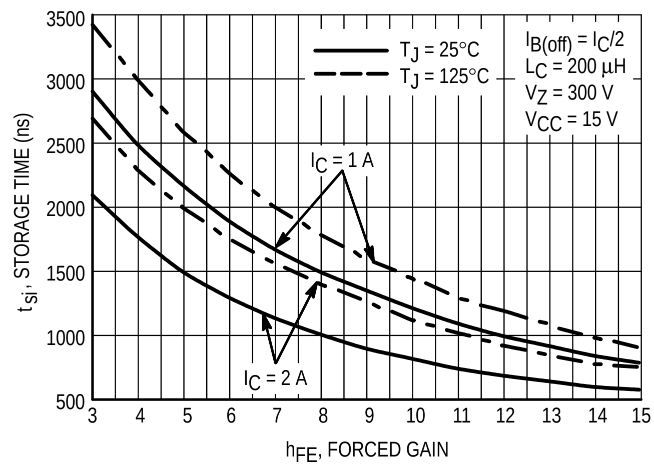


Figure 10. Inductive Storage Time, $t_{si}(h_{FE})$

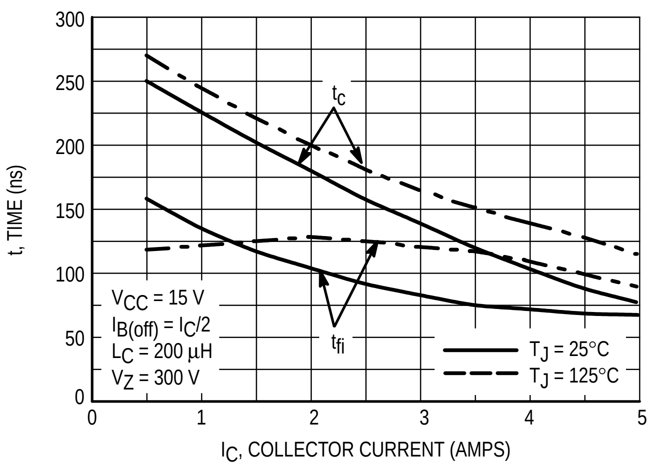


Figure 11. Inductive Switching, t_c & t_{fi}, $I_C/I_B = 5$

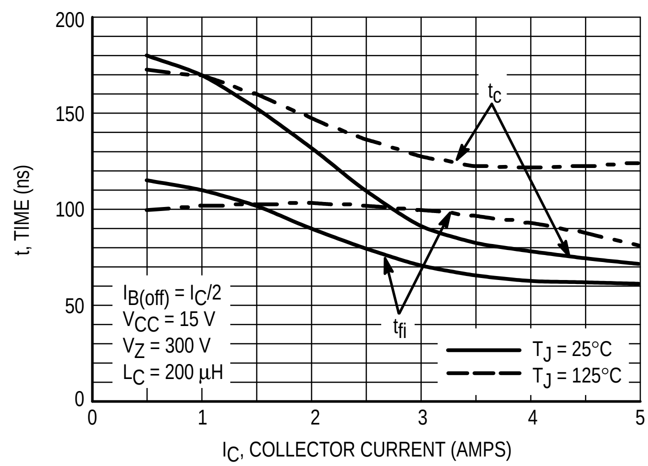


Figure 12. Inductive Switching, t_c & t_{fi}, $I_C/I_B = 10$

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

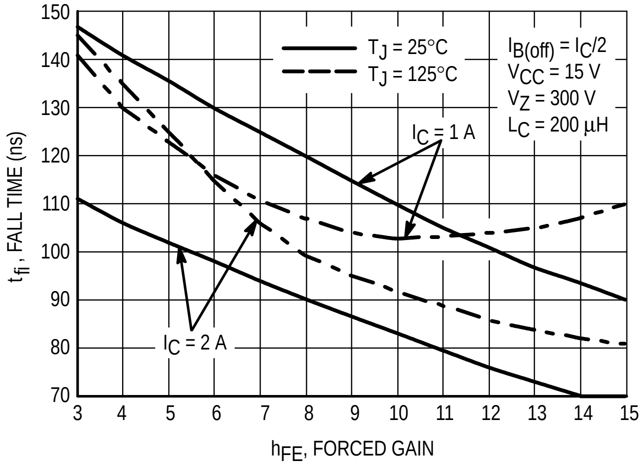


Figure 13. Inductive Fall Time, $t_{fi}(h_{FE})$

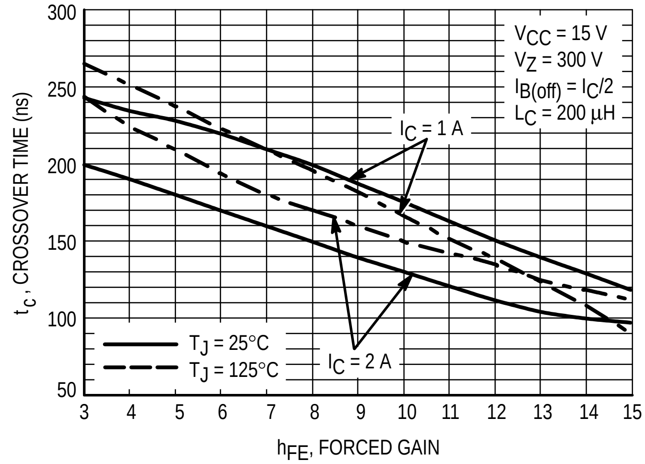


Figure 14. Crossover Time

GUARANTEED SAFE OPERATING AREA INFORMATION

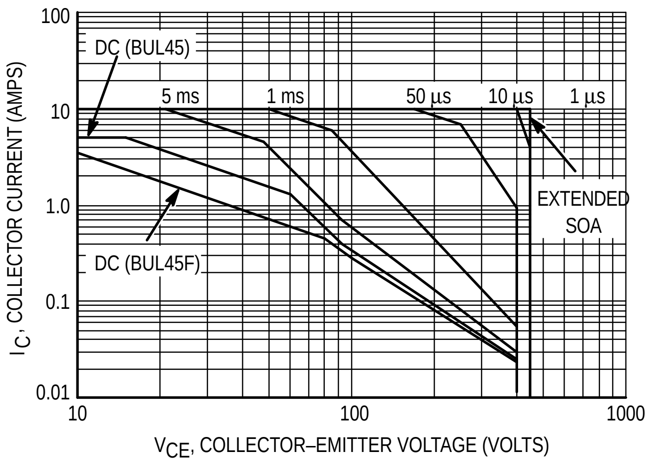


Figure 15. Forward Bias Safe Operating Area

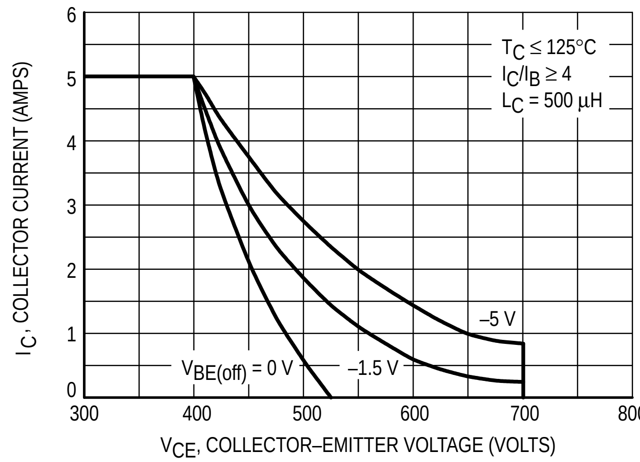


Figure 16. Reverse Bias Switching Safe Operating Area

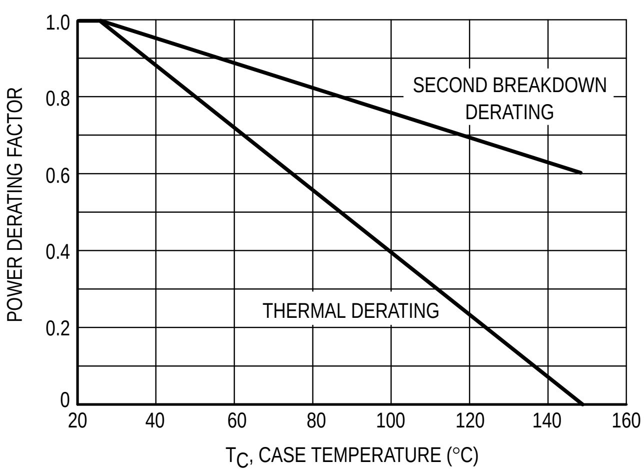


Figure 17. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown in Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17. $T_{J(pk)}$ may be calculated from the data in Figures 20 and 21. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base–to–emitter junction reverse–biased. The safe level is specified as a reverse–biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

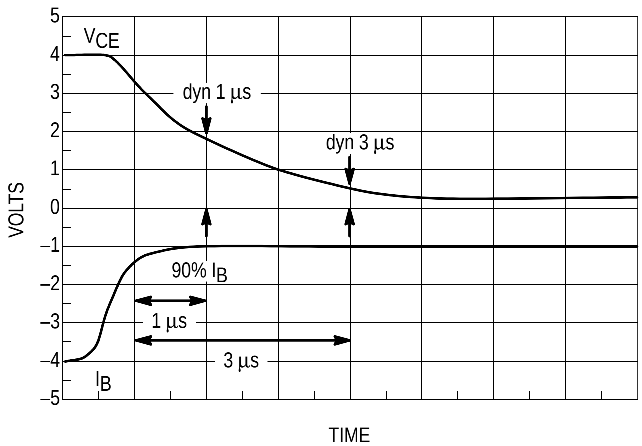


Figure 18. Dynamic Saturation Voltage Measurements

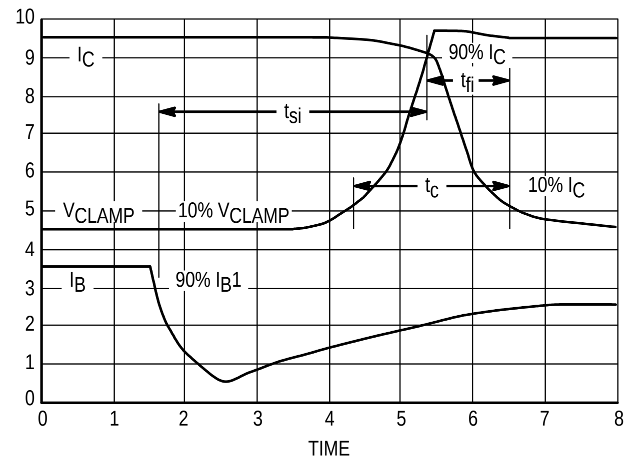
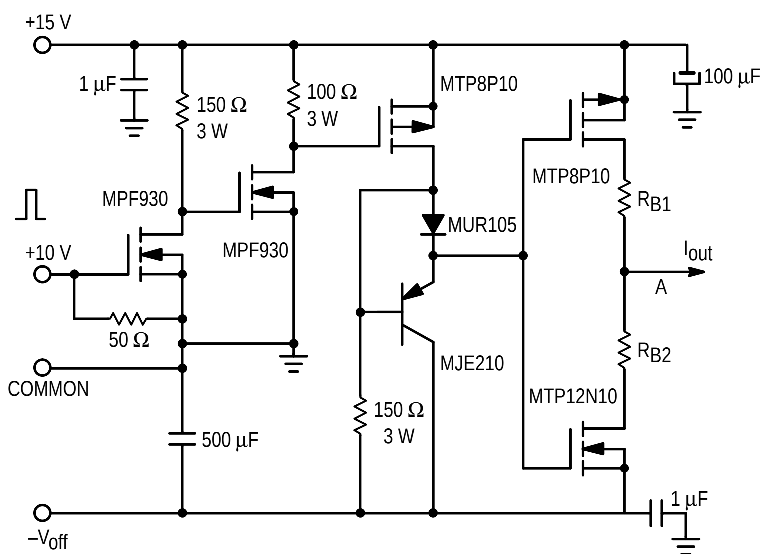
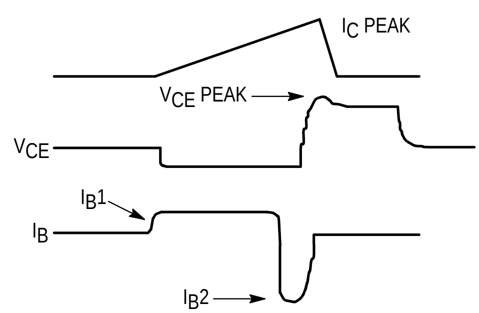


Figure 19. Inductive Switching Measurements





V(BR)CEO(sus)	INDUCTIVE SWITCHING	RBSOA
L = 10 mH	L = 200 µH	L = 500 µH
RB2 = ∞	RB2 = 0	RB2 = 0
V_{CC} = 20 VOLTS	V_{CC} = 15 VOLTS	V_{CC} = 15 VOLTS
I_C(pk) = 100 mA	RB1 SELECTED FOR DESIRED I_B1	RB1 SELECTED FOR DESIRED I_B1

Table 1. Inductive Load Switching Drive Circuit

TYPICAL THERMAL RESPONSE

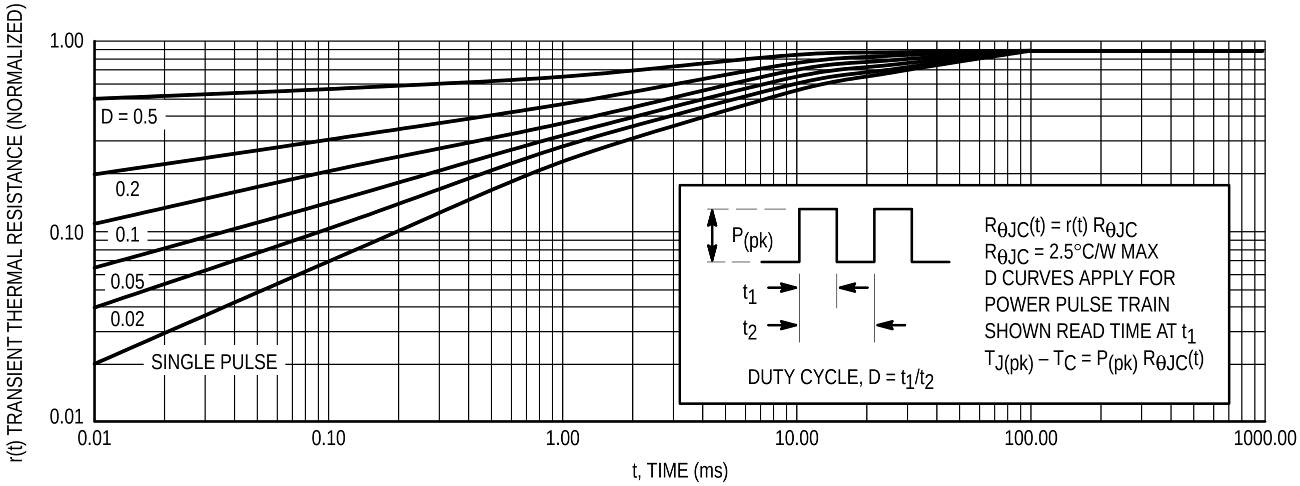


Figure 20. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUL45

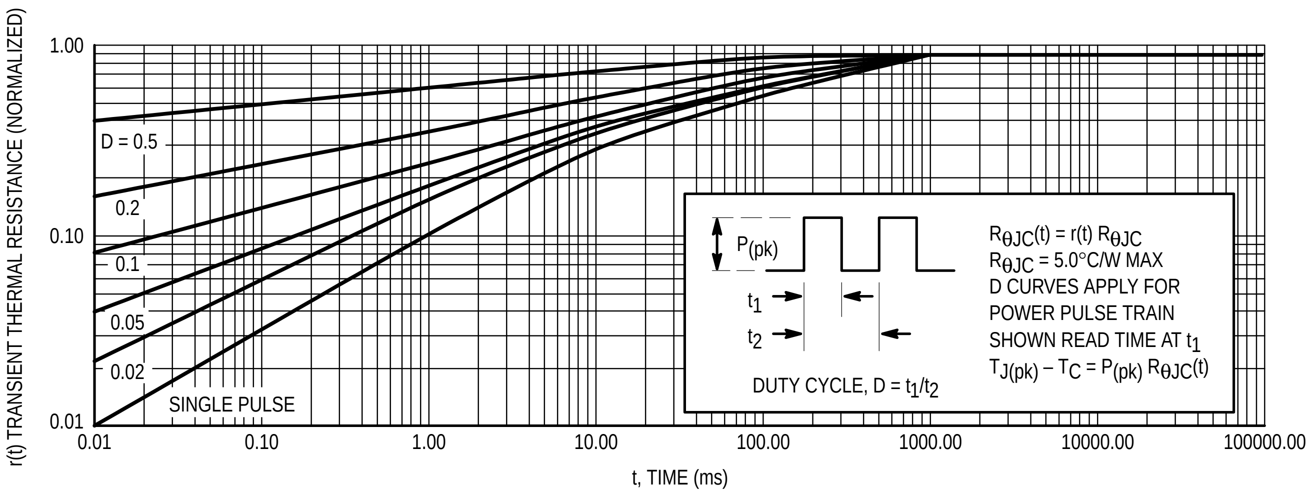
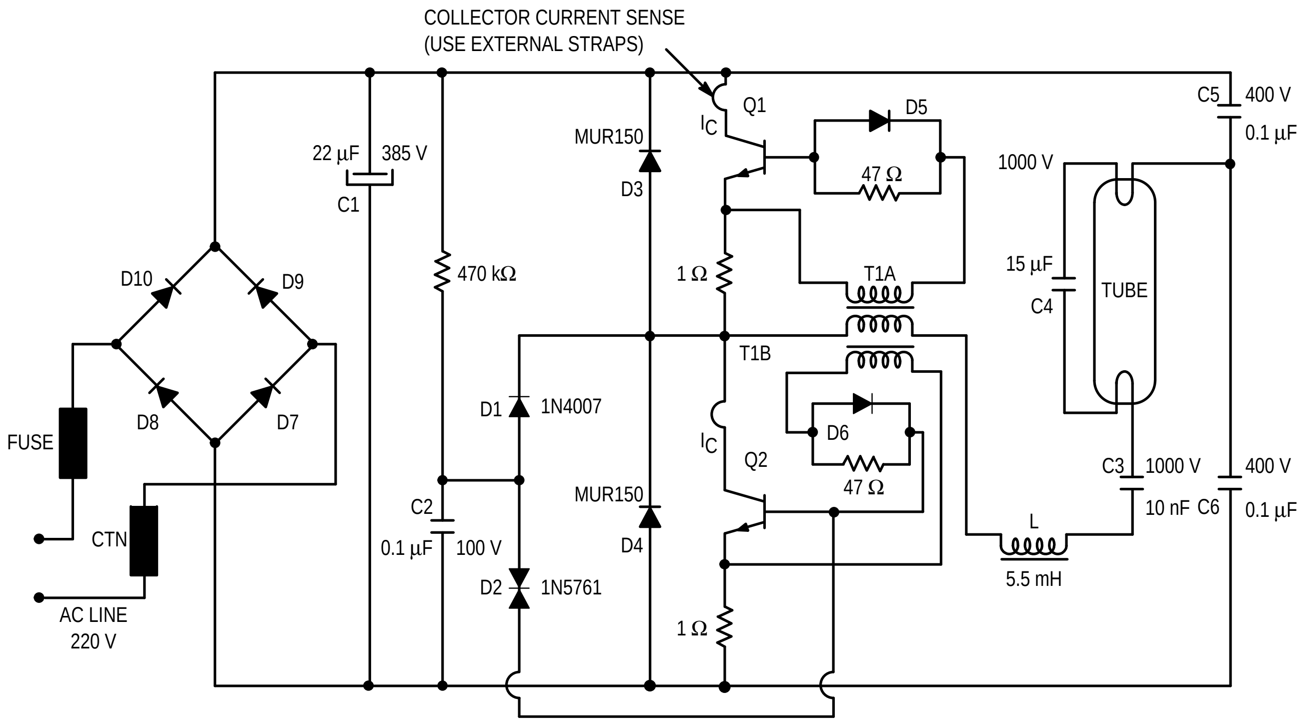


Figure 21. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUL45F

The BUL45/BUL45F Bipolar Power Transistors were specially designed for use in electronic lamp ballasts. A circuit designed by Motorola applications was built to demonstrate how well these devices operate. The circuit and detailed component list are provided below.



Components Lists

Q1 = Q2 = BUL45 Transistor
D1 = 1N4007 Rectifier
D2 = 1N5761 Rectifier
D3 = D4 = MUR150
D5 = D6 = MUR105
D7 = D8 = D9 = D10 = 1N400
CTN = 47 Ω @ 25°C
L = RM10 core, A1 = 400, B51 (LCC) 75 turns, wire ∅ = 0.6 mm
T1 = FT10 toroid, T4A (LCC)
Primary: 4 turns
Secondaries: T1A: 4 turns
T1B: 4 turns

All resistors are 1/4 Watt, ±5%
R1 = 470 kΩ
R2 = R3 = 47 Ω
R4 = R5 = 1 Ω (these resistors are optional, and might be replaced by a short circuit)
C1 = 22 µF/385 V
C2 = 0.1 µF
C3 = 10 nF/1000 V
C4 = 15 nF/1000 V
C5 = C6 = 0.1 µF/400 V

NOTES:
1. Since this design does not include the line input filter, it cannot be used “as–is” in a practical industrial circuit.
2. The windings are given for a 55 Watt load. For proper operation they must be re–calculated with any other loads.

Figure 22. Application Example

TEST CONDITIONS FOR ISOLATION TESTS*

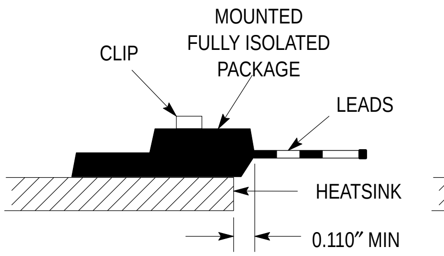


Figure 22a. Screw or Clip Mounting Position for Isolation Test Number 1

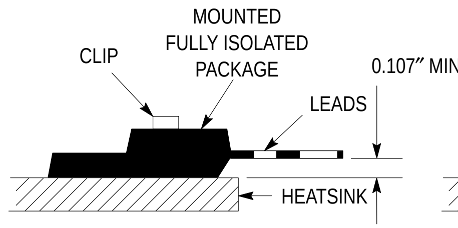


Figure 22b. Clip Mounting Position for Isolation Test Number 2

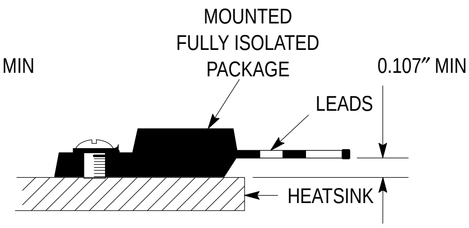


Figure 22c. Screw Mounting Position for Isolation Test Number 3

* Measurement made between leads and heatsink with all leads shorted together.

MOUNTING INFORMATION**

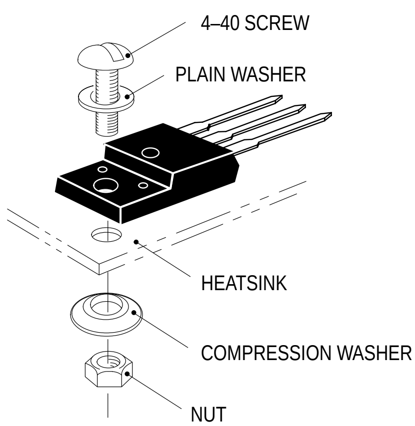


Figure 23a. Screw–Mounted

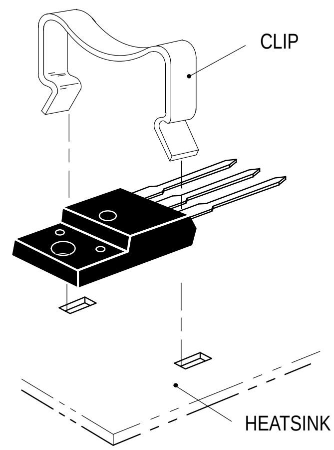


Figure 23b. Clip–Mounted

Figure 23. Typical Mounting Techniques for Isolated Package

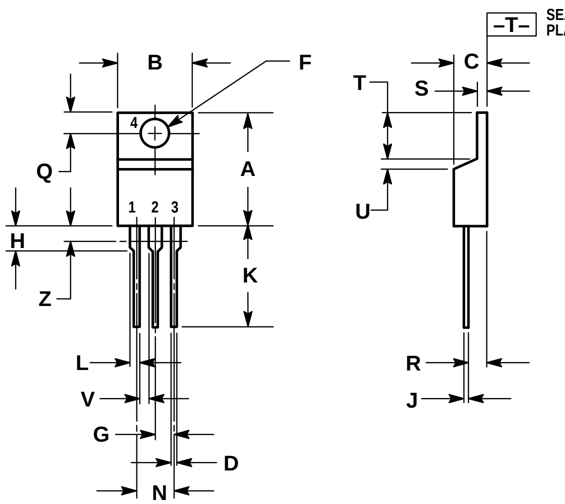
Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, Motorola does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

PACKAGE DIMENSIONS

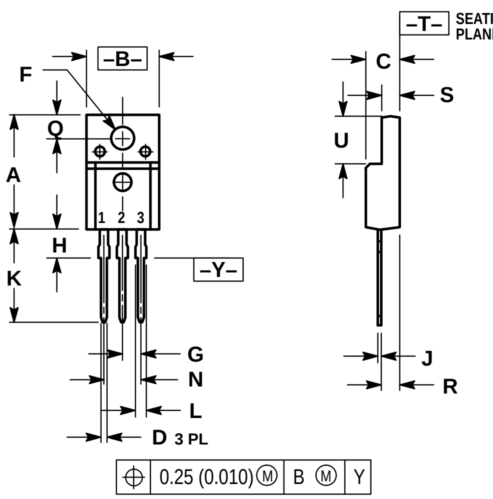


STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

BUL45
CASE 221A–06
TO–220AB
ISSUE Y



STYLE 2:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.621	0.629	15.78	15.97
B	0.394	0.402	10.01	10.21
C	0.181	0.189	4.60	4.80
D	0.026	0.034	0.67	0.86
F	0.121	0.129	3.08	3.27
G	0.100 BSC		2.54 BSC	
H	0.123	0.129	3.13	3.27
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.14	1.52
N	0.200 BSC		5.08 BSC	
Q	0.126	0.134	3.21	3.40
R	0.107	0.111	2.72	2.81
S	0.096	0.104	2.44	2.64
U	0.259	0.267	6.58	6.78

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INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, Toshikatsu Otsuki,
6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–3521–8315

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298