

Dual 5V Regulator with Serial Data Buffer Interface for Microcontroller Applications

April 1994

Features

- Dual 5V Regulator
 - V_{OUT1} at 5V 100mA - Standby
 - V_{OUT2} at 5V 100mA - Enabled
 - Regulation Range 6V to 18V
 - Bandgap Voltage References
- Low Quiescent Idle Current, 500 μ A Typ.
- Over-Voltage Shutdown Protection, 20.5V Typ.
- Reverse Battery Protection, -26V Max.
- Thermal Shutdown Protection
- Short Circuit Current Limiting
- Low Input P.S. Flag and Delayed Reset Control
- Low Voltage Shutdown Control, Output1
- Ignition Comparator Logic Level Control
- Data Comparator and 100X Current Mult. Used as Input/Output Buffers for Remote Serial Data Communication

Applications

- Automotive 5V Regulators and Data Buffers
- Industrial Controller Remote System
- Microcontroller and Memory Power Supply
- Radio, TV, CATV, Consumer Applications

Description

The CA3277 is a Dual 5V Voltage Regulator IC intended for microprocessor and logic controller applications. It is supplied with features that are commonly specified for sequentially controlled shutdown and startup requirements of microcontrollers. Over-voltage shutdown, short circuit current limiting and thermal shutdown features are provided for protection in the harsh environmental applications of industrial and automotive systems. The CA3277 functions are complementary to the needs of microcontroller and memory circuits, providing for sustained memory with a 5V standby output.

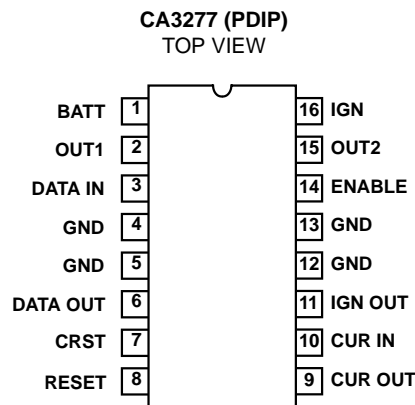
The Ignition Comparator senses the voltage level at the IGN IN input and provides a 5V logic switched output (supply sourced from OUT1). The Ignition Output, IGN OUT can be used to signal a system microcontroller which can respond with a logic switched output to the CA3277 ENABLE input control for OUT2. The OUT1 +5V Standby Supply of the regulator is normally used as a power supply for microcontroller/memory circuits to preserve stored data when in the standby mode. To allow for maximum heat transfer from the chip, the four center leads are directly connected to the die mounting pad.

Refer to AN9302 for further information on CA3277 circuit Applications.

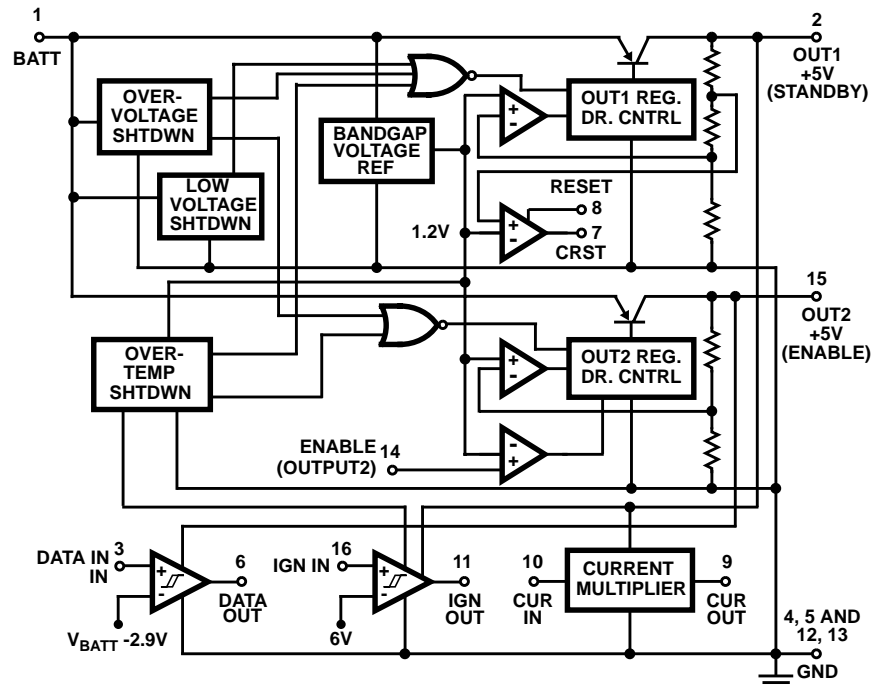
Ordering Information

| PART NUMBER | TEMPERATURE RANGE | PACKAGE |
|-------------|-------------------|---------------------|
| CA3277E | -40°C to +85°C | 16 Lead Plastic DIP |

Pinout



Functional Block Diagram



Specifications CA3277

Absolute Maximum Ratings

| | |
|---|-------------------------|
| Max. BATT, IGN IN Input Voltage (Note1) | ±26V |
| Max. Operating Voltage; BATT, IGN IN | $V_{BATT(SD)}$ (~20.5V) |
| Max. Positive Voltages: (For Negative Voltages, Note 2) | |
| ENABLE Input | V_{BATT} |
| DATA IN Input | V_{BATT} |
| CUR OUT, Output | V_{BATT} |
| RESET, Output | V_{BATT} |
| Max. Operating Load Current, OUT1 | 100mA |
| Max. Operating Load Current, OUT2 | 100mA |
| Max. Current Mult. Load Currents: | |
| Min. Load Resistance, CUR OUT | 225Ω to BATT (75mA max) |
| Min. Load Resistance, CUR IN | 1KΩ to GND (-5mA max) |
| Max. Load Current OUT1, OUT2 (Short Duration) | Self-Limiting |
| Max. Plus/Minus Load Currents: (Note 3) | |
| IGN OUT Output | Self-Limiting |
| DATA OUT Output | Self-Limiting |
| RESET Output | Self-Limiting |

Thermal Information

| | | |
|---|------------------------------|---------------|
| Thermal Resistance | θ_{JA} | θ_{JL} |
| Plastic DIP Package | 60°C/W | 12°C/W |
| (Temp. meas. on center lead next to case) | | |
| Power Dissipation, P_D (Note 4): | | |
| Up to +60°C (Free Air) | 1.5W | |
| Above +60°C: | Derate Linearly at 16.6mW/°C | |
| Up to +85°C w/heat sink (PC Board): | 1.6 W | |
| Operating Temperature Range | -40°C to +85°C | |
| Storage Temperature Range | -55°C to +150°C | |
| Max. Junction Temperature | +150°C | |
| Lead Temperature (During Solder) | +265°C | |
| 1/16 ± 1/32" from case, 10s max | | |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{BATT} = 13.5\text{V}$, ENABLE ON ($V_{EN} = 3.5\text{V}$), IGN IN connected to BATT, OUT1 and OUT2 bypassed with 20μF to GND, DATA IN connected through 250Ω to BATT, LOADS: OUT1 = 50mA, OUT2 = 80mA; Unless Otherwise Specified (Refer to Figure 4 Test Circuit)

| PARAMETERS | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-----------------|--|------|-----|------|------------|
| REGULATOR OUTPUT1 | | | | | | |
| Output Voltage | V_{OUT1} | $V_{BATT} = 9\text{V}$ to 16V | 4.75 | 5 | 5.25 | V |
| Dropout Voltage (Note 5) | V_{DO1} | $V_{BATT} = 4.75\text{V}$ | 4.15 | 4.6 | - | V |
| Line Reg | | $V_{BATT} = 6.2\text{V}$ to 16V | - | 9 | 40 | mV |
| Load Reg | | $I_{LOAD} = 0.5\text{mA}$ to 50mA | - | 30 | 60 | mV |
| Current Limiting | | | - | 170 | 250 | mA |
| Low Voltage Shutdown | | Ramp V_{BATT} Down Until OUT1 drops (PNP Driver Cutoff) | - | 3.5 | - | V |
| REGULATOR OUTPUT2 | | | | | | |
| Output Voltage | V_{OUT2} | $V_{BATT} = 9\text{V}$ to 16V | 4.75 | 5 | 5.25 | V |
| Dropout Voltage (Note 5) | V_{DO2} | $V_{BATT} = 5.6\text{V}$ | 4.6 | 5 | - | V |
| Line Reg | | $V_{BATT} = 6.2\text{V}$ to 16V | - | 7.5 | 40 | mV |
| Load Reg | | $I_{LOAD} = 0.5\text{mA}$ to 80mA | - | 35 | 60 | mV |
| Current Limiting | | | - | 190 | 250 | mA |
| ENABLE Input Current | I_{EN} | $V_{EN} = 5\text{V}$ | - | 50 | 150 | μA |
| ENABLE Input Sw. Thd. | $V_{EN(THD)}$ | Ramp ENABLE Input Up Until OUT2 is Switched ON | - | 1.2 | - | V |
| CURRENT MULTIPLIER | | | | | | |
| Current Mult. Gain, (I_{COUT}/I_{CIN}) | | $I_{CIN} = -200\mu\text{A}$ | 80 | 100 | - | Gain Ratio |
| Current Mult. Output Sat. | $V_{COUT(SAT)}$ | $I_{CIN} = -200\mu\text{A}$, CUR OUT Load = 1KΩ to V_{BATT} | - | 0.3 | 1 | V |
| Current Mult., Max. Drive Cur. | $I_{COUT(MAX)}$ | $I_{CIN} = -700\mu\text{A}$ | 35 | 50 | - | mA |
| RESET | | | | | | |
| Reset, (RST) Threshold | | Ramp V_{BATT} Down, Measure V_{BATT} when RESET (V_{RST}) goes low | 3.8 | 4.2 | 4.5 | V |
| Reset Delay Time (Note 6) | t_{RST} | CRST Cap. = 0.47μF, $V_{BATT} = 6.8\text{V}$ RESET Load = 5KΩ to OUT1 | 50 | 150 | 250 | ms |
| RESET Out High | $V_{OH(RST)}$ | 47KΩ to OUT1 | 4 | - | - | V |
| RESET Low | $V_{OL(RST)}$ | $V_{BATT} = 3.75\text{V}$, RST 47KΩ to OUT1 | - | - | 0.2 | V |
| RESET Output Sink Current | I_{OL} | CRST to GND, $V_{BATT} = 6.8\text{V}$ | - | 8 | - | mA |

Specifications CA3277

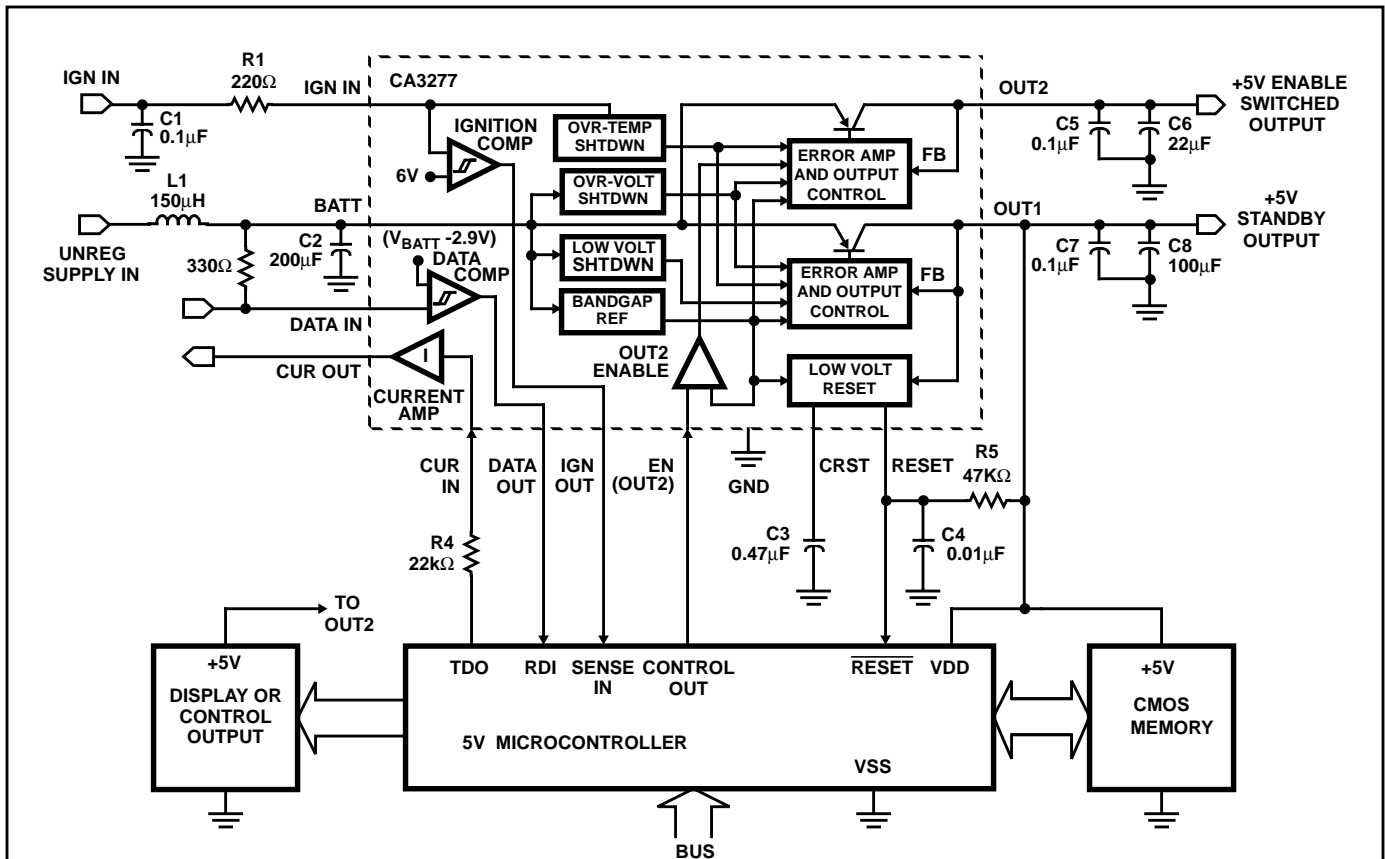
Electrical Specifications $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{\text{BATT}} = 13.5\text{V}$, ENABLE ON ($V_{\text{EN}} = 3.5\text{V}$), IGN IN connected to BATT, OUT1 and OUT2 bypassed with $20\mu\text{F}$ to GND, DATA IN connected through 250Ω to BATT, LOADS: OUT1 = 50mA, OUT2 = 80mA; Unless Otherwise Specified (Refer to Figure 4 Test Circuit) **(Continued)**

| PARAMETERS | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------------|-------------------------|--|--------------------------|-------------------------|-------------------------|--------------------|
| DATA COMPARATOR | | | | | | |
| Data Comp Thd | | | $V_{\text{BATT}} - 3.6$ | $V_{\text{BATT}} - 2.9$ | $V_{\text{BATT}} - 2.2$ | V |
| Data Comp Hysteresis | | | - | 200 | - | mV |
| DATA OUT Low | V_{OL} | $V_{\text{BATT}} = 16\text{V}$, $V_{\text{DATA IN}} = (V_{\text{BATT}} - 5\text{V})$ | - | - | 0.15 | V |
| DATA OUT High | V_{OH} | $V_{\text{BATT}} = 16\text{V}$, $V_{\text{DATA IN}} = 16\text{V}$ | $V_{\text{OUT1}} - 0.15$ | - | 5.25 | V |
| DATA OUT Low Sink Current | I_{OL} | $V_{\text{DATA IN}}$ Low | - | 1 | - | mA |
| DATA OUT High Source Current | I_{OH} | $V_{\text{DATA IN}}$ High | - | -50 | - | μA |
| IGNITION COMPARATOR | | | | | | |
| Ign Comp Thd | | | 5.5 | 6 | 6.5 | V |
| Ign Comp Hysteresis | | | - | 200 | - | mV |
| IGN OUT Low | V_{OL} | | - | - | 0.15 | V |
| IGN OUT High | V_{OH} | | 4.6 | | 5.25 | V |
| IGN OUT Low Sink Current | I_{OL} | $V_{\text{IGN IN}}$ Low | - | 1 | - | mA |
| IGN OUT High Source Current | I_{OH} | $V_{\text{IGN IN}}$ High | - | -70 | - | μA |
| OTHER PARAMETERS | | | | | | |
| Idle Current | I_{Q} | $V_{\text{BATT}} = 12.6\text{V}$, No Loads, $V_{\text{EN}} = V_{\text{IGN IN}} = 0\text{V}$ | - | 500 | 800 | μA |
| Over-Voltage Shutdown | $V_{\text{BATT(OVSD)}}$ | Ramp V_{BATT} Up Until OUT1 and OUT2 Shutdown | 19 | 20.5 | 23 | V |
| Thermal Shutdown | T_{J} | | - | 150 | - | $^{\circ}\text{C}$ |
| Ripple Rejection | | $1V_{\text{PP}}$ at 3kHz on BATT INPUT, Measure AC Ripple on OUT1, OUT2 | 45 | 55 | - | dB |

NOTES:

- For negative voltages on the BATT and IGN IN inputs, current drain is primarily reverse junction leakage, except when DATA IN, CUR OUT, ENABLE and RESET are directly connected to BATT. (Note 2)
- For negative voltage DATA IN, CUR OUT, ENABLE and RESET interface to NPN or equivalent on-chip structures; providing a forward junction for current conduction into the IC. Negative current must be limited by the impedance of the external connection. This is also the case where these terminals are interconnected to BATT, Normal application does not require the BATT connection, except for DATA IN where a series diode for reverse current blocking may be used. (see Description text information)
- Refer to the Electrical Characteristic TABLE for all Self-Limiting values.
- Dissipation, approximately equals: $P_{\text{D}} \approx [(V_{\text{IN}} I_{\text{IN}}) + (V_{\text{CUR OUT}} I_{\text{CUR OUT}}) - 5(I_{\text{OUT1}} + I_{\text{OUT2}})]$, where $I_{\text{IN}} V_{\text{IN}}$ is IGN IN and BATT input dissipation and $V_{\text{OUT1}} \sim V_{\text{OUT2}} \sim 5\text{V}$. This assumes negligible dissipation for the Ignition Comp., Reset and Data Comp. Outputs.
- Dropout Voltage is $V_{\text{DO1}} = (V_{\text{BATT}} - V_{\text{OUT1}})$ for REG. OUT1 and $V_{\text{DO2}} = (V_{\text{BATT}} - V_{\text{OUT2}})$ for REG. OUT2
- Reset Delay Time, t_{RST} is the time period that the RESET (Pin 8) is low following the discharge of the CRST capacitor to ground. For test evaluation, the CRST pin may be discharged repetitively with a transistor switch. The RESET pin switches from low to high when the CRST pin is charged to approximately 3V. Normal ATE testing measures the source charging current, which is typically $10\mu\text{A}$. For any other value of Capacitor the charge time, t for reset is determined as follows: $t \sim 308C$, where C is in μF and t is in milliseconds. (i.e. $C = 0.47\mu\text{F}$, $t = 141\text{ms}$)

CA3277



NOTE: DATA IN and CUR OUT are remote/host Serial Data Communication Buffers. Typical Remote Source Impedance for DATA IN is 1k Ω . Typical Remote Load for CUR OUT is 250 Ω .

FIGURE 1. TYPICAL APPLICATION CIRCUIT OF THE CA3277 DUAL 5V REGULATOR WITH MICROCONTROLLER AND SERIAL DATA BUFFER INTERFACE TO A REMOTE HOST

Applications

Other functions of the CA3277 include a Data Comparator and Current Multiplier for use as interface buffers to transfer serial data at higher level logic to and from a remote host microcontroller. The OUT1 5V Standby Supply provides power to the local microcontroller which interfaces to the CA3277 interface buffers at a 5V logic level. As shown in Figure 1, the DATA IN input of the Data Comparator receives serial data referenced to the BATT voltage level. The output of the Data Comparator is 5V CMOS compatible logic and is connected to the RDI (remote data input) terminal of the microcontroller. The TDO (data out) output of the microcontroller is connected to the Current Multiplier input of the CA3277.

Current Multiplier - The Current Multiplier, with internal circuitry shown in Figure 2, receives data from the microcontroller in the form of an open drain or gate switched output driving a 22k Ω resistor load in series to the Current Input at pin 10 (CUR IN). The input stage of the Current Multiplier is a current mirror amplifier which is internally connected to the 5V regulated OUT1 voltage source. The output stage of the Current Multiplier is a current mirror amplifier referenced to GND and has an open collector Current Output at pin 9 (CUR OUT), with a minimum drive capability of 35mA. The Current Multiplier output load is

normally connected via resistive loading to the BATT voltage supply level. As such, the microcontroller transmits data out (TDO output) to the input of the CA3277 Current Multiplier which amplifies and translates the signal back to the voltage reference level of the BATT power supply input. When driving a similar remote CA3277, the voltage drop from the BATT input line switches the Data Comparator which provides serial data to the RDI input of the remote microcontroller. The nominal current gain of the Current Multiplier is 100X.

The application use of the Current Multiplier is not limited to digital serial data transfer. The Current Multiplier is an independent function and is open to use for other purposes, including linear signal amplification, sensor output amplification and current controlled threshold switching. The current output terminal, CUR OUT may be externally load-connected to OUT1, OUT2, BATT or any other power supply level up to the maximum ratings given for the BATT input terminal. It is important to note that some applied uses of the Current Multiplier may contribute significant on-chip power dissipation. A nominal current mirror input drive of 200 μ A will provide sufficient drive to switch a 250 Ω resistor load at the input of the data comparator. As such, the quiescent OFF condition of the Data comparator should be in the High state.

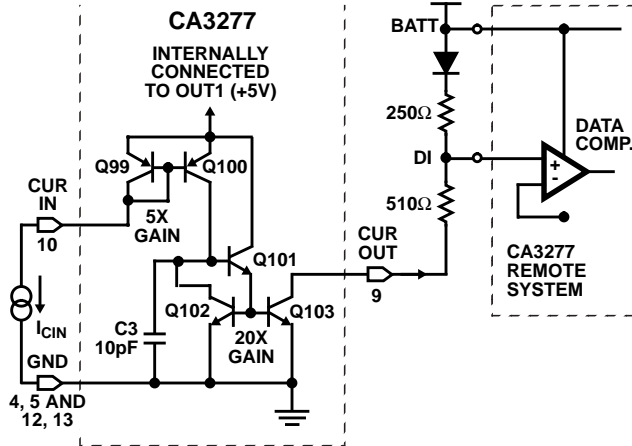


FIGURE 2. CURRENT MULTIPLIER DRIVING A REMOTE CA3277 DATA COMPARATOR

Data Comparator - The Data Comparator provides a means of translating serial data from a high to low voltage. The DATA IN terminal of the Data Comparator is biased to receive signal input that is source referenced to the BATT supply voltage level. In normal use the signal input would be supplied from a remote Current Multiplier having a resistor load tied to the BATT voltage supply. The DATA OUT output from the Data Comparator is CMOS compatible 5V non-inverting logic data referenced to GND. The switching threshold at the DATA IN input is bias stabilized by the bandgap voltage and is typically at ($V_{BATT} - 2.9V$). The Data Comparator is in a high state when DATA IN input is at the BATT voltage level and is in a low state when DATA IN is at ($V_{BATT} - 5V$). The output stage of the Data Comparator is internally supply biased from the Switched 5V Regulator output to provide a high state of 5V and a low state of 0V (GND). The DATA OUT terminal can typically sink 1.2mA in a low state or source 50 μ A in a high state.

In system applications the Data Comparator is used to translate remote data at high voltage down to 5V logic levels. The Current Multiplier is used to reverse the process by translating 5V logic data back to the BATT voltage level when sending data back to the remote system. The Data Comparator and Current Multiplier are level matched for remote communication between microcontroller systems using the common BATT power supply voltage of the CA3277. The current driven serial data from the Current Multiplier is sent to a remote system by translating the signal up to the BATT voltage level, or an external power supply level that is compatible with the remote device. The Data Comparator of the remote system receives the data, interfaces to its microcontroller and responds with signal drive from its Current Multiplier to translate the signal back to the host. For best noise immunity the transmission in each direction should be over a twisted pair or shielded line. As such, two microcontrollers, each with the interface protection of a CA3277, can provide intelligent master/slave system communications under adverse environmental conditions.

Ignition Comparator - While the Ignition Comparator is provided as an essential part of the start-up control in automotive systems, this circuit function may be used as an independent switching comparator. **It is important to note that the thermal shutdown feature on the chip is disabled when the IGN IN input is low.** Disabling of the on-chip thermal protection is done to satisfy the requirement of low idle current when the system is in a standby condition. The non-inverting IGN IN input has a switching threshold of typically 6V with 200mV of hysteresis and is switched with logic levels reference to GND as the low state and BATT as the high state. The IGN OUT output is 5V CMOS compatible logic, equivalent to the Data Comparator output stage, but is internally supply biased from the Standby 5V Regulator. As such, the high state is level referenced to OUT1. The IGN OUT output terminal can typically sink 1.2mA in a low state or source 70 μ A in a high state.

Enable - A CMOS or TTL high at the ENABLE input switches the regulated 5V/Switched Output ON at OUT2. The ENABLE input has an internal pull-down of typically 50 μ A to ensure that OUT2 is OFF when the ENABLE input is not connected. The input threshold level for switching is the bandgap voltage reference of 1.2V. When the ENABLE input is low, all drive current to the output pass transistor is cutoff and OUT2 voltage drops to ground level. The ENABLE input is normally switched from the interfacing microcontroller but may be activated from a remote source.

Reset - The purpose of the Low Voltage Reset function is to flag a low voltage condition at OUT1. When the RESET output, pin 8 switches low, the voltage level at OUT1 has dropped below the regulation level. The CRST and RESET are high when OUT1 is at 5V. When OUT1 drops to less than 4.2V (typical), the CRST Capacitor at pin 7 is internally discharged, causing the RESET pin to change from a high to a low state, outputting a negative going pulse. The RESET output is an NPN open collector driver requiring an external load resistor, normally connected to OUT1. The RESET output flag may be sent to a microcontroller to initiate a power-down sequence. For any condition that causes OUT1 to drop below the reset threshold, such as undesired transients, the RESET output is switched low for a delay period, t_{RST} determined by the value of the external capacitor, C_{RST} at CRST terminal. For a value of 0.47 μ F the delay period is typically 141ms. This correlates to approximately 10 μ A of charging current sourced from the CRST terminal to charge C_{RST} .

Regulation - The regulated output stages of the CA3277 have similar circuits, each having an error amplifier to compare the output voltage to the bandgap reference voltage. The circuit of the 5V/Switched regulator is shown in Figure 3. By feedback, the output voltage is differentially compared to the bandgap reference voltage. The error signal is then amplified to drive a PNP pass transistor and maintain a stable 5V output with both line and load regulation over the full operating temperature range. Except for the ENABLE control of OUT2, the OUT1 drive circuit is similar to the OUT2 circuit.

Protection - Both OUT1 and OUT2 PNP output pass transistors are protected with Over-Voltage Shutdown and Over-Temperature Shutdown. Current Limiting for each output is independent and is accomplished by limited drive current from the pre-drivers (Q135 for OUT2) to the PNP output pass transistor (Q136). Over-Voltage is sensed as a threshold voltage level at the BATT input. Both output stages are shutdown when the V_{BATT} voltage level is typically greater than 20.5V. When the Ignition voltage is high, the Over-Temperature level is sensed as V_{BE} changes and compared to the bandgap reference voltage. When the chip temperature exceeds 150°C, both output stages are shutdown. When Over-Voltage or Over-Temperature thresholds are exceeded, the sensed states are OR'd to switch OFF drive to the output stages. The ENABLE control for OUT2 is added to the OR control of the OUT2 drive circuit. The Low Voltage Shutdown control is added to the OR control of the OUT1 drive circuit. Low Voltage Shutdown occurs at approximately 3.5V as the BATT supply input is ramped down, forcing cutoff of the PNP output pass transistor. The external capacitor on OUT1 holds charge, with a long RC time constant delay to sustain shutdown control in the microcontroller. The internal shunt resistance at the OUT1 terminal is typically 148KΩ.

Under conditions of reverse battery or negative supply voltages on the BATT input, current in the IC is primarily reverse junction leakage. The design of the CA3277 is configured to prevent high current if the power supply is reversed. Exceptions to this are preventable. One example is current through the DATA IN input line terminating resistor,

normally connected directly to the BATT supply line. This provides a path for current conduction into the IC through an internal diode junction. The current is limited by the external resistor and may be as high as 100mA at -26V. Where negative supply voltages are potentially a problem, the resistive load from DATA IN to BATT can be in series with a reverse voltage blocking diode, such as a 1N914. This input diode-resistor circuit is shown in Figure 2 as the remote interface and load to the Current Multiplier output.

Dissipation - The CA3277 device dissipation is the combined watts of input voltage times current less the external watts of power supplied by the chip. For normal use, the major contribution to on-chip dissipation is primarily the BATT input dissipation. The Current Multiplier output has a potential to add significant dissipation. The open collector driver of the Current Multiplier Output, pin 9 may or may not be in saturation when sinking current. Because it is a current mirror output with a constant current drive, the voltage may be increased on pin 9, with a significant increase in the resulting dissipation. The chip dissipation is approximately equal to:

$$P_D \approx [(V_{IN}I_{IN}) + (V_{COUT}I_{COUT}) - 5(I_{OUT1}+I_{OUT2})]$$

where $I_{IN}V_{IN}$ is IGN IN and BATT input dissipation, assuming $V_{BATT} = V_{IGN IN}$, and $V_{OUT1} \sim V_{OUT2} \sim 5V$. This assumes negligible dissipation for the Ignition Comparator, Data Comparator and Reset outputs.

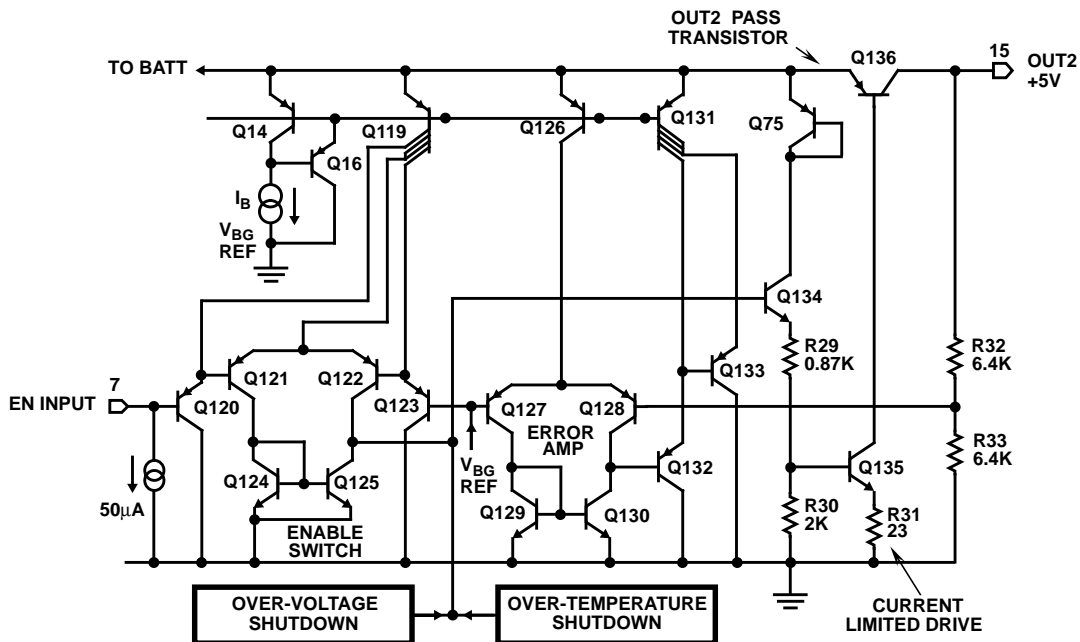


FIGURE 3. OUTPUT2 DRIVER AND ERROR AMPLIFIER WITH THE ENABLE CONTROL

CA3277

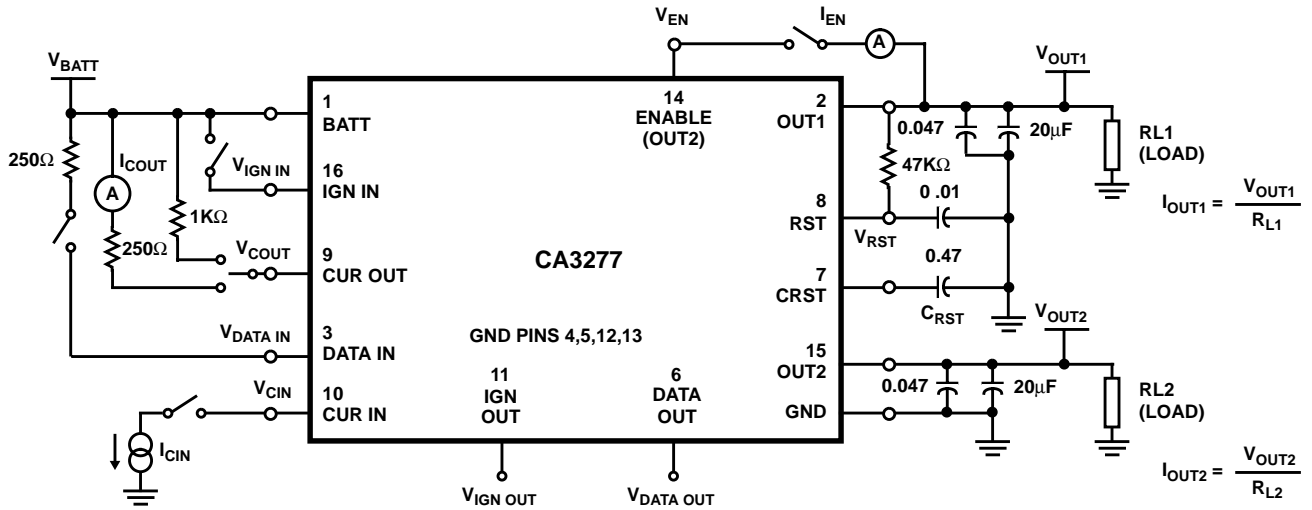


FIGURE 4. CHARACTERISTIC EVALUATION AND TEST CIRCUIT

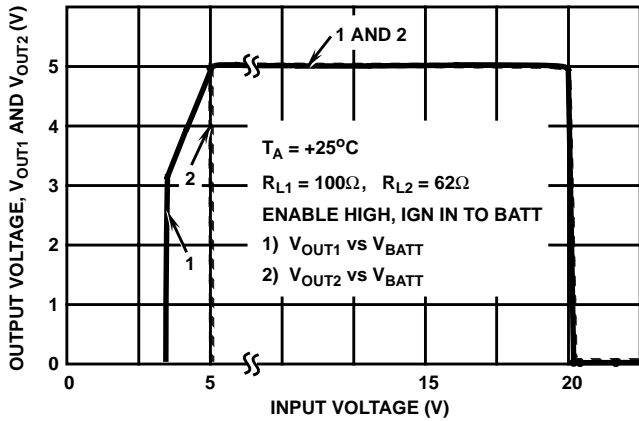


FIGURE 4A. TYPICAL CHARACTERISTIC CURVES FOR OUT1 AND OUT2 OUTPUT VOLTAGE vs BATT VOLTAGE INPUT

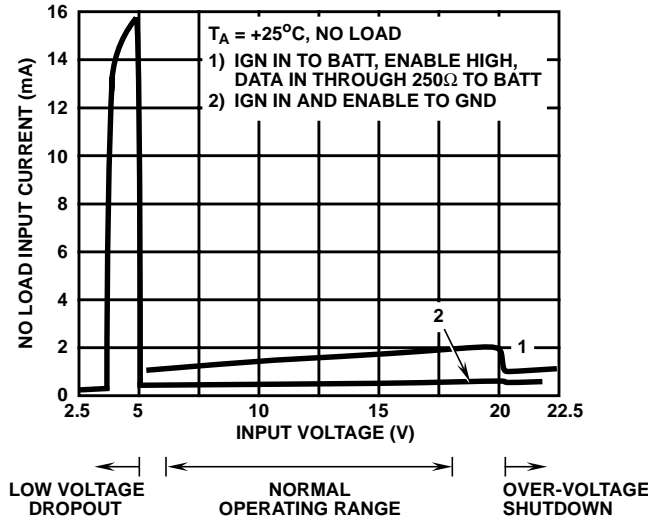


FIGURE 4B. TYPICAL CHARACTERISTICS CURVES FOR NO-LOAD BATT INPUT CURRENT vs BATT INPUT VOLTAGE FOR OFF STATE IDLE CURRENTS

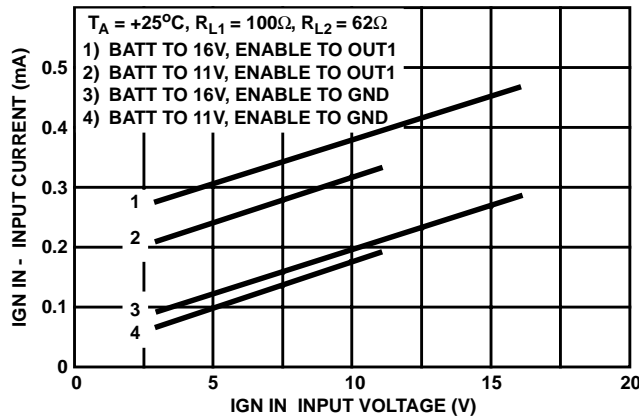


FIGURE 4C. TYPICAL IGN IN CURRENT vs IGN IN INPUT VOLTAGE

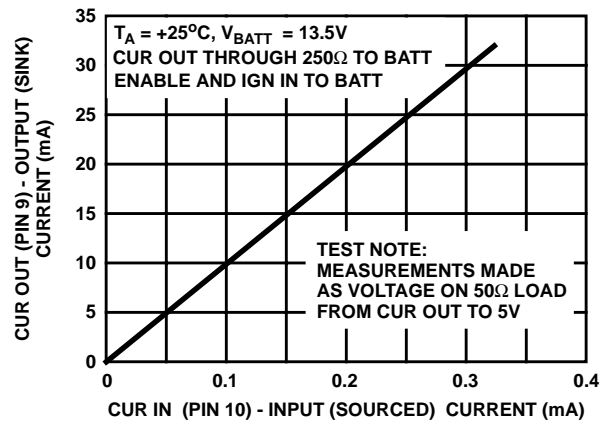


FIGURE 4D. TYPICAL CURRENT MULTIPLIER CURRENT GAIN CHARACTERISTIC

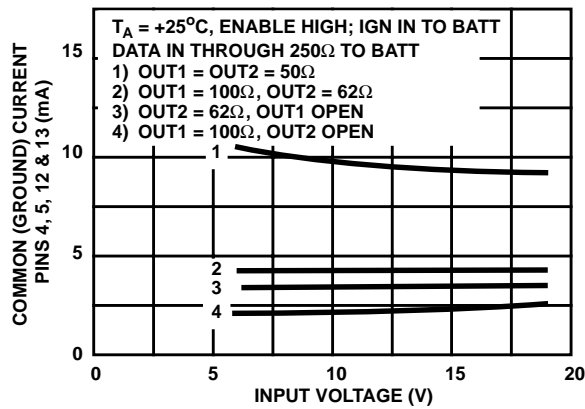


FIGURE 4E. TYPICAL CHARACTERISTIC CURVES FOR COMMON (GROUND) CURRENT vs BATT VOLTAGE INPUT WITH OUTPUT LOAD

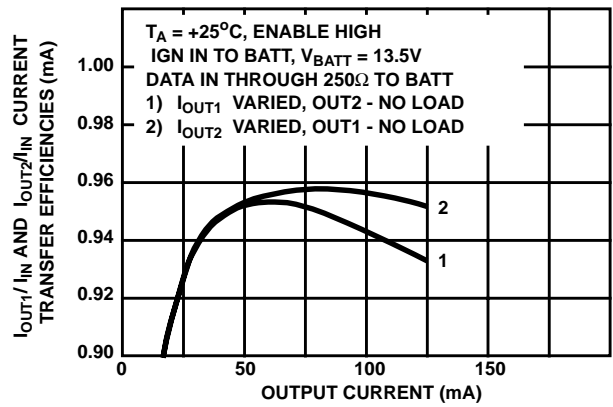


FIGURE 4F. TYPICAL CHARACTERISTIC CURVES FOR CURRENT TRANSFER EFFICIENCY OF $I_{\text{OUT1}}/I_{\text{IN}}$ AND $I_{\text{OUT2}}/I_{\text{IN}}$ WHERE I_{IN} INCLUDES ($I_{\text{IGN IN}} + I_{\text{DATA IN}}$) BIAS CURRENTS

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