

## CD4013BC Dual D-Type Flip-Flop

### General Description

The CD4013B dual D-type flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement mode transistors. Each flip-flop has independent data, set, reset, and clock inputs and "Q" and "Q̄" outputs. These devices can be used for shift register applications, and by connecting "Q̄" output to the data input, for counter and toggle applications. The logic level present at the "D" input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line respectively.

### Features

- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45 V<sub>DD</sub> (typ.)
- Low power TTL: fan out of 2 driving 74L compatibility: or 1 driving 74LS

### Applications

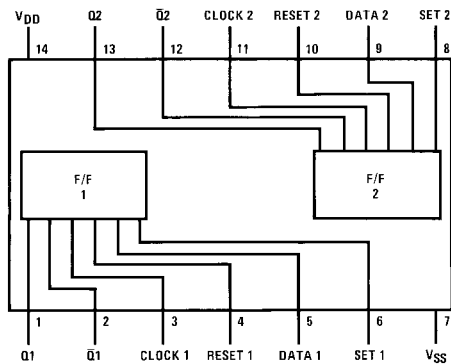
- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial electronics
- Remote metering
- Computers

### Ordering Code:

Order Number	Package Number	Package Description
CD4013BCM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4013BCSJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
CD4013BCN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Connection Diagram



Top View

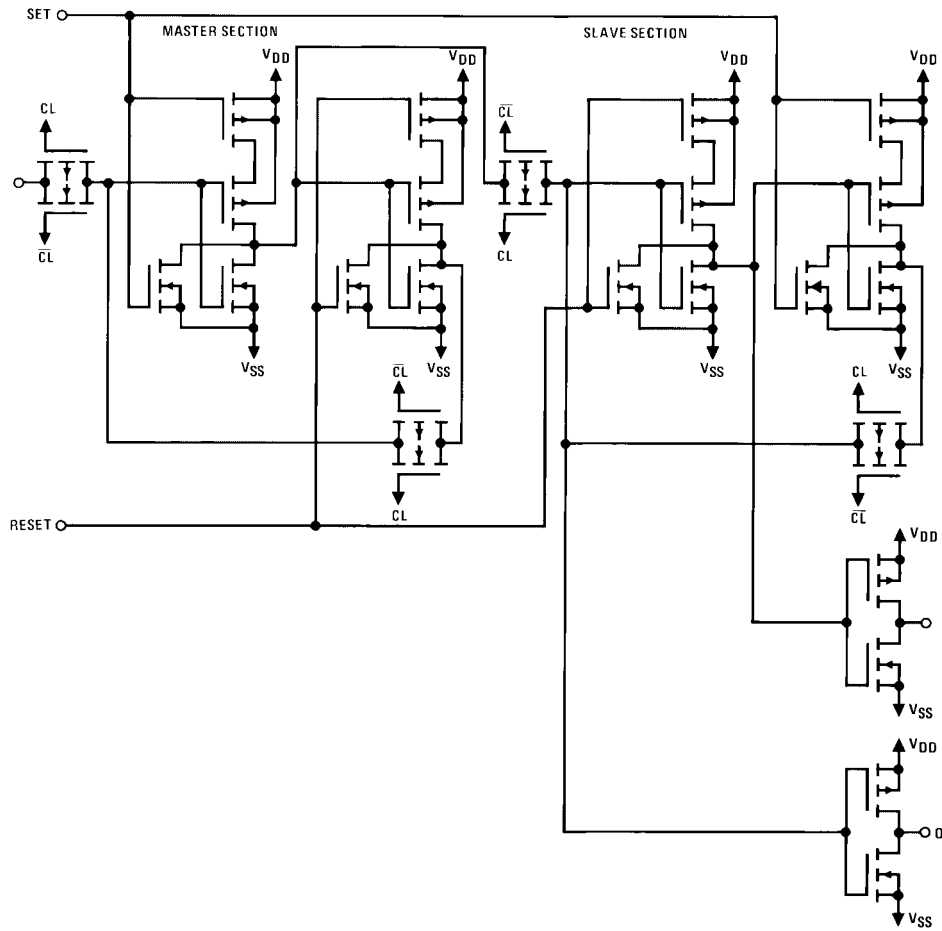
### Truth Table

CL (Note 1)	D	R	S	Q	Q̄
—	0	0	0	0	1
—	1	0	0	1	0
~	x	0	0	Q	Q̄
x	x	1	0	0	1
x	x	0	1	1	0
x	x	1	1	1	1

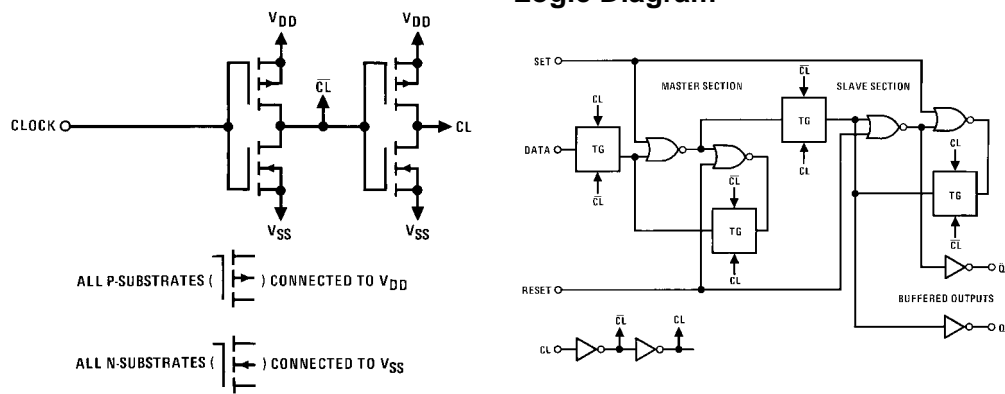
No Change  
x = Don't Care Case

Note 1: Level Change

Schematic Diagrams



Logic Diagram



<b>Absolute Maximum Ratings</b> (Note 2)		<b>Recommended Operating Conditions</b> (Note 3)	
(Note 3)			
DC Supply Voltage ( $V_{DD}$ )	-0.5 $V_{DC}$ to +18 $V_{DC}$	DC Supply Voltage ( $V_{DD}$ )	+3 $V_{DC}$ to +15 $V_{DC}$
Input Voltage ( $V_{IN}$ )	-0.5 $V_{DC}$ to $V_{DD}$ +0.5 $V_{DC}$	Input Voltage ( $V_{IN}$ )	0 $V_{DC}$ to $V_{DD}$ $V_{DC}$
Storage Temperature Range ( $T_S$ )	-65°C to +150°C	Operating Temperature Range ( $T_A$ )	-55°C to +125°C
Power Dissipation ( $P_D$ )		<b>Note 2:</b> "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.	
Dual-In-Line	700 mW	<b>Note 3:</b> $V_{SS} = 0V$ unless otherwise specified.	
Small Outline	500 mW		
Lead Temperature ( $T_L$ )			
(Soldering, 10 seconds)	260°C		

**DC Electrical Characteristics** (Note 3)

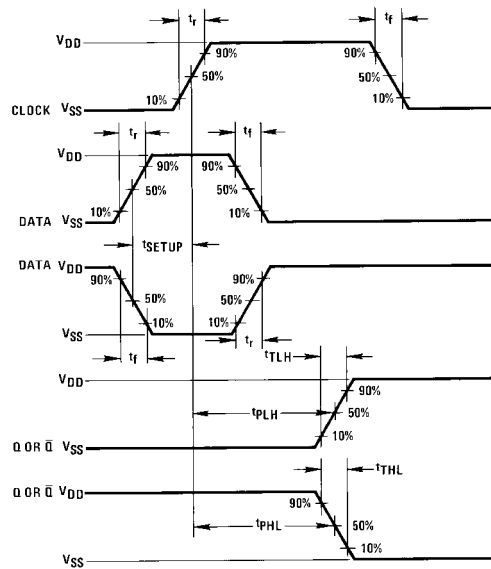
Symbol	Parameter	Conditions	-55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
$I_{DD}$	Quiescent Device Current	$V_{DD} = 5V, V_{IN} = V_{DD}$ or $V_{SS}$ $V_{DD} = 10V, V_{IN} = V_{DD}$ or $V_{SS}$ $V_{DD} = 15V, V_{IN} = V_{DD}$ or $V_{SS}$		1.0 2.0 4.0			1.0 2.0 4.0		30 60 120	$\mu A$
$V_{OL}$	LOW Level Output Voltage	$ I_{OL}  < 1.0 \mu A$ $V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		0.05 0.05 0.05			0.05 0.05 0.05		0.05 0.05 0.05	V
$V_{OH}$	HIGH Level Output Voltage	$ I_{OH}  < 1.0 \mu A$ $V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$	4.95 9.95 14.95		4.95 9.95 14.95			4.95 9.95 14.95		V
$V_{IL}$	LOW Level Input Voltage	$ I_{OL}  < 1.0 \mu A$ $V_{DD} = 5V, V_O = 0.5V$ or 4.5V $V_{DD} = 10V, V_O = 1.0V$ or 9.0V $V_{DD} = 15V, V_O = 1.5V$ or 13.5V		1.5 3.0 4.0			1.5 3.0 4.0		1.5 3.0 4.0	V
$V_{IH}$	HIGH Level Input Voltage	$ I_{OH}  < 1.0 \mu A$ $V_{DD} = 5V, V_O = 0.5V$ or 4.5V $V_{DD} = 10V, V_O = 1.0V$ or 9.0V $V_{DD} = 15V, V_O = 1.5V$ or 13.5V	3.5 7.0 11.0		3.5 7.0 11.0			3.5 7.0 11.0		V
$I_{OL}$	LOW Level Output Current (Note 4)	$V_{DD} = 5V, V_O = 0.4V$ $V_{DD} = 10V, V_O = 0.5V$ $V_{DD} = 15V, V_O = 1.5V$	0.64 1.6 4.2		0.51 1.3 3.4	0.88 2.25 8.8		0.36 0.9 2.4		mA
$I_{OH}$	HIGH Level Output Current (Note 4)	$V_{DD} = 5V, V_O = 4.6V$ $V_{DD} = 10V, V_O = 9.5V$ $V_{DD} = 15V, V_O = 13.5V$	-0.64 -1.6 -4.2		-0.51 -1.3 -3.4	-0.88 -2.25 -8.8		-0.36 -0.9 -2.4		mA
$I_{IN}$	Input Current	$V_{DD} = 15V, V_{IN} = 0V$ $V_{DD} = 15V, V_{IN} = 15V$		-0.1 0.1		$-10^{-5}$ $10^{-5}$	-0.1 0.1		-1.0 1.0	$\mu A$

**Note 4:**  $I_{OH}$  and  $I_{OL}$  are measured one output at a time.

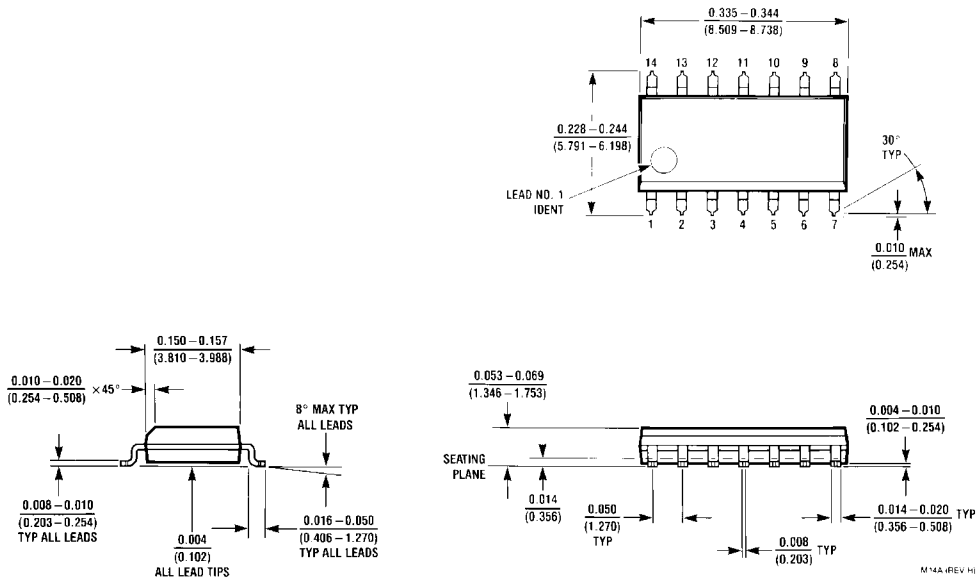
AC Electrical Characteristics (Note 5)						
$T_A = 25^\circ\text{C}$ , $C_L = 50\text{ pF}$ , $R_L = 200\text{ k}$ , unless otherwise noted						
Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>CLOCK OPERATION</b>						
$t_{PHL}, t_{PLH}$	Propagation Delay Time	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		200 80 65	350 160 120	ns
$t_{THL}, t_{TLH}$	Transition Time	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		100 50 40	200 100 80	ns
$t_{WL}, t_{WH}$	Minimum Clock Pulse Width	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		100 40 32	200 80 65	ns
$t_{RCL}, t_{FCL}$	Maximum Clock Rise and Fall Time	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$			15 10 5	$\mu\text{s}$
$t_{SU}$	Minimum Set-Up Time	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		20 15 12	40 30 25	ns
$f_{CL}$	Maximum Clock Frequency	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$	2.5 6.2 7.6	5 12.5 15.5		MHz
<b>SET AND RESET OPERATION</b>						
$t_{PHL(R)}, t_{PLH(S)}$	Propagation Delay Time	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		150 65 45	300 130 90	ns
$t_{WH(R)}, t_{WH(S)}$	Minimum Set and Reset Pulse Width	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		90 40 25	180 80 50	ns
$C_{IN}$	Average Input Capacitance	Any Input		5	7.5	pF

Note 5: AC Parameters are guaranteed by DC correlated testing.

### Switching Time Waveforms



**Physical Dimensions** inches (millimeters) unless otherwise noted



**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow  
Package Number M14A**

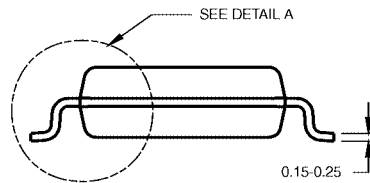
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

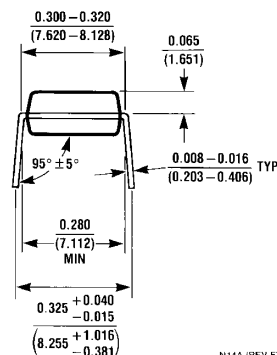
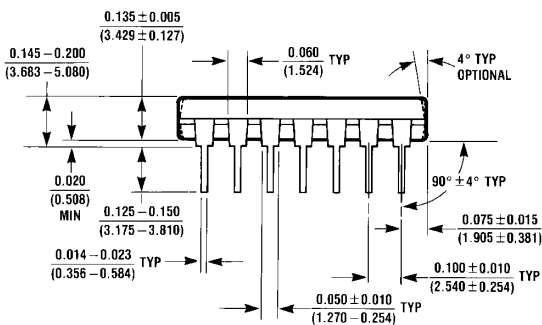
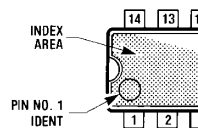
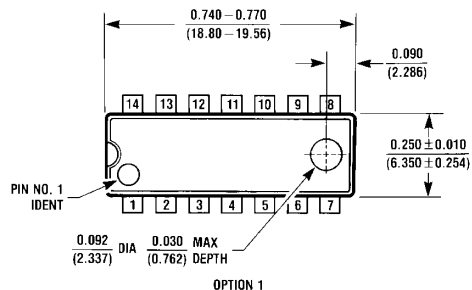
- NOTES:  
 A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.  
 B. DIMENSIONS ARE IN MILLIMETERS.  
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1



**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
 Package Number M14D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



N14A (REV F)

**14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A**

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