CMOS High Voltage Logic – CD4070B

CMOS Quad 2-Input Exclusive-OR gate in bare die form

Rev 1.0
19/09/18

Description

The CD4070B provides the system designer with direct implementation of the Exclusive-OR function. The device has equal source and sink current capabilities and conforms to standard B series output drive. Device outputs are buffered which improves transfer characteristics by providing very high gain. The device is capable of driving x2 low power TTL loads or x1 LSTTL load. The CD4070B is primarily used for higher voltage acceptance and where low power dissipation and/or high noise immunity are required.

Features:

- High Input Voltage up to 20V
- Symmetrical Output Characteristics
- Max input current 1µA at 18V over full Military Temperature Range
- Low Power TTL compatible
- Specified at 5V, 10V & 15V
- Direct drop-in replacement for obsolete components in long term programs.

Ordering Information

The following part suffixes apply:

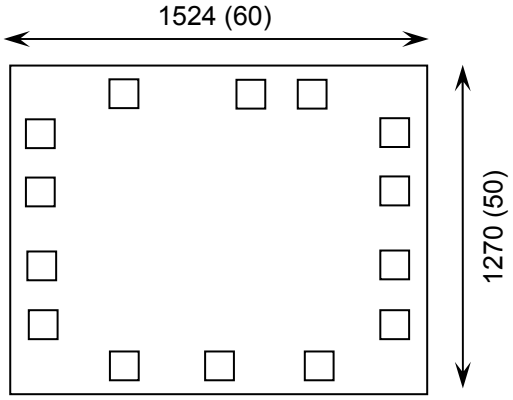
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space) + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 635µm(25 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1524 x 1270 50 x 37	µm mils
Minimum Bond Pad Size	102 x 102 4 x 4	µm mils
Die Thickness	635 (±20) 25 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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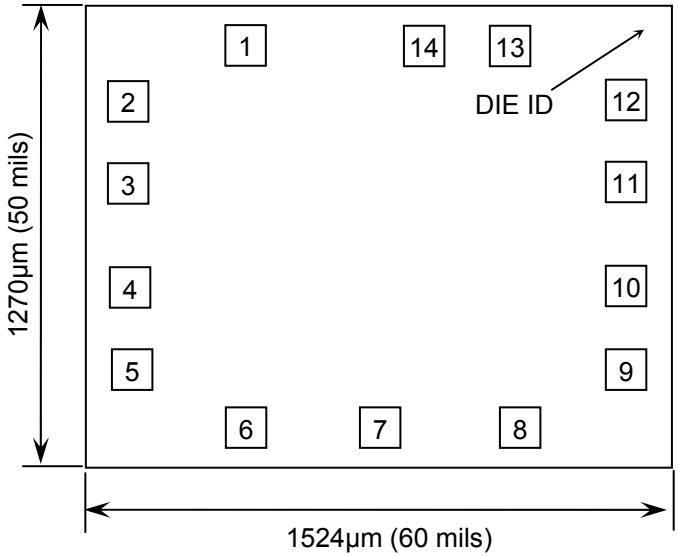
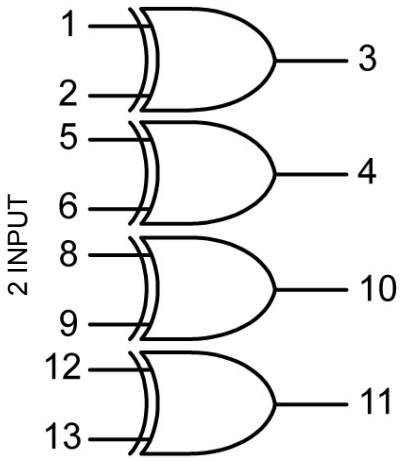
Pad Layout and Functions



PAD	FUNCTION
1	1A
2	1B
3	1Y
4	2Y
5	2A
6	2B
7	V_{SS}
8	3A
9	3B
10	3Y
11	4Y
12	4A
13	4B
14	V_{DD}
CONNECT CHIP BACK TO V_{DD} OR FLOAT	

Logic Diagram



Pad 14 = V_{DD}
Pad 7 = V_{SS}

Truth Table

INPUTS		OUTPUT
A	B	Y
L	L	L
H	L	H
L	H	H
H	H	L
H = High level (steady state) L = Low level (steady state)		

$Y = A \oplus B$

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Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to V_{SS})	V_{DD}	-0.5 to +20	V
DC Input or Output Voltage (Referenced to V_{SS})	V_{IN}, V_{OUT}	-0.5 to V_{DD}+0.5	V
Storage Temperature Range	T_{STG}	-65 to 150	°C
Input Current or Output Current (per Pad)	I_{IN}, I_{OUT}	±10	mA
Power Dissipation in Still Air	P_D	500	mW

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[3] (Voltages referenced to V_{SS})

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{DD}	3.0	18	V
DC Input Voltage, Output Voltage	V_{IN}, V_{OUT}	0	V_{DD}	V
Operating Temperature Range	T_J	-55	+125	°C

3. This device contains protection circuitry against damage due to high static voltages or electric fields. However, any voltage higher than maximum rated voltages to this high-impedance circuit should be avoided. For proper operation, V_{IN} & V_{OUT} should be constrained to the range $V_{SS} \le (V_{IN}$ or $V_{OUT}) \le V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages referenced to V_{SS})

PARAMETER	SYMBOL	V_{DD}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum High-Level Input Voltage	V_{IH}	5V	V_{OUT} = 0.5V	3.5	3.5	3.5	V
		10V	V_{OUT} = 1.0V	7	7	7	
		15V	V_{OUT} = 1.5V	11	11	11	
Maximum Low-Level Input Voltage	V_{IL}	5V	V_{OUT} = 0.5V or V_{DD} -0.5V	1.5	1.5	1.5	V
		10V	V_{OUT} = 0.5V or V_{DD} -0.5V	3	3	3	
		15V	V_{OUT} = 0.5V or V_{DD} -0.5V	4	4	4	
Minimum High-Level Output Voltage	V_{OH}	5V	V_{IN} = 0 or V_{DD}	4.95	4.95	4.95	V
		10V		9.95	9.95	9.95	
		15V		14.95	14.95	14.95	
Maximum Low-Level Output Voltage	V_{OL}	5V	V_{IN} = V_{DD} or 0	0.05	0.05	0.05	V
		10V		0.05	0.05	0.05	
		15V		0.05	0.05	0.05	
Maximum Input Leakage Current	I_{IN}	18V	V_{IN} = V_{DD} or V_{SS}	±0.1	±.0.1	±1.0	µA
Maximum Quiescent Supply Current	I_{DD}	5V	V_{IN} = V_{DD} or V_{SS} I_{OUT} = 0µA	0.25	7.5	7.5	µA
		10V		0.5	15	15	
		15V		1.0	30	30	
		20V		5.0	150	150	

DC Electrical Characteristics Continued (Voltages referenced to V_{SS})

PARAMETER	SYMBOL	V_{DD}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum Output Low (Sink) Current	I_{OL}	5V	V_{IN} = V_{DD} or V_{SS} V_{OL} = 0.4V	0.64	0.51	0.36	mA
		10V	V_{IN} = V_{DD} or V_{SS} V_{OL} = 0.5V	1.6	1.3	0.9	
		15V	V_{IN} = V_{DD} or V_{SS} V_{OL} = 1.5V	4.2	3.4	2.4	
Minimum Output High (Source) Current	I_{OH}	5V	V_{IN} = V_{DD} or V_{SS} V_{OH} = 2.5V	-3.0	-2.4	-1.7	mA
		5V	V_{IN} = V_{DD} or V_{SS} V_{OH} = 4.6V	-0.64	-0.51	-0.36	
		10V	V_{IN} = V_{DD} or V_{SS} V_{OH} = 9.5V	-1.6	-1.3	-0.9	
		15V	V_{IN} = V_{DD} or V_{SS} V_{OH} = 13.5V	-4.2	-3.4	-2.4	

4. . $-55^{\circ}C \le T_J \le +125^{\circ}C$

AC Electrical Characteristics[5]

PARAMETER	SYMBOL	V_{DD}	CONDITIONS	TYPICAL	LIMITS		UNITS
				25°C	85°C	FULL RANGE[4]	
Propagation Delay, Input A or B to Output Y (Figure 1)	t_{PLH}, t_{PHL}	5V	C_L = 50pF, R_L = 200kΩ t_r = t_f = 20ns	125	250	500	ns
		10V		60	120	240	
		15V		45	90	180	
Output Transition Time, Any Output (Figure 1)	t_{TLH}, t_{THL}	5V	C_L = 50pF, R_L = 200kΩ t_r = t_f = 20ns	100	200	400	ns
		10V		50	100	200	
		15V		40	80	160	
Input Capacitance	C_{IN}	-	C_L = 50pF, R_L = 200kΩ t_r = t_f = 20ns	5	7.5	7.5	pF

5. Not production tested in die form, characterized by chip design and tested in package.

Switching Waveform

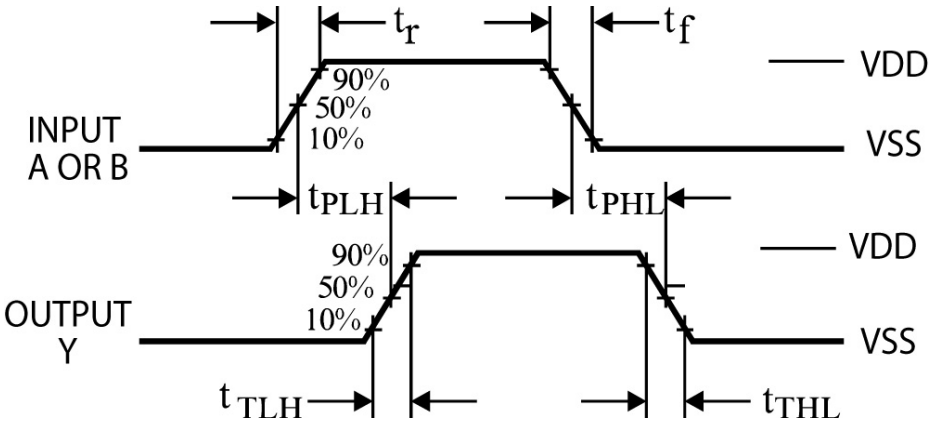

Figure 1 – Propagation Delay, Transition Timing