HARRIS SEMICONDUCTOR

CD54AC163/3A
CD54ACT163/3A

June 1997

COMPLETE DATA SHEET COMING SOON!

Synchronous Presettable Binary Counters

Description

The CD54AC163/3A and CD54ACT163/3A are synchronous presettable binary counters that utilize the Harris Advanced CMOS Logic technology. The CD54AC163/3A and CD54ACT163/3A are reset synchronously with the clock. Counting and parallel presetting are both accomplished synchronously with the negative-to-positive transition of the clock.

A LOW level on the Synchronous Parallel Enable input, $\overline{SPE}$, disables the counting operation and allows data at the P0 to P3 inputs to be loaded into the counter (provided that the setup and hold requirements for $\overline{SPE}$ are met).

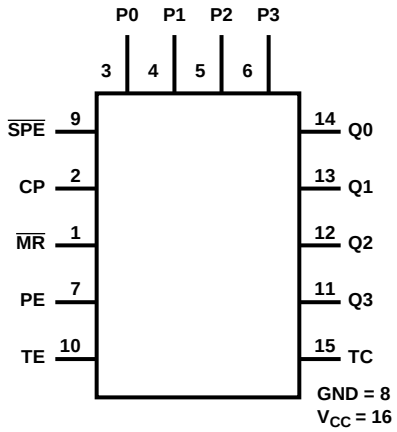
The counters are reset with a LOW level on the Master Reset input, $\overline{MR}$. The requirements for setup and hold time with respect to the clock must be met.

Two count enables, PE and TE, in each counter are provided for n-bit cascading. Reset action occurs regardless of the level of the $\overline{SPE}$, PE and TE inputs.

The look-ahead carry feature simplifies serial cascading of the counters. Both count enable inputs (PE and TE) must be HIGH to count. The TE input is gated with the Q outputs of all four stages so that at the maximum count, the terminal count (TC) output goes HIGH for one clock period. This TC pulse is used to enable the next cascaded stage.

The CD54AC163/3A and CD54ACT163/3A are supplied in 16 lead dual-in-line ceramic packages (F suffix).

Functional Diagram



ACT INPUT LOAD TABLE

INPUT	UNIT LOAD (NOTE 1)
Pn	0.13
CP	1
$\overline{MR}$, TE	0.83
$\overline{SPE}$	0.67
PE	0.5

NOTE:

1. Unit load is ΔI_{CC} limit specified in DC Electrical Specifications Table, e.g., 2.4mA Max at +25°C.

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . . -0.5V to +6V
DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . . ±20mA
DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . . ±50mA
DC Output Source or Sink Current, Per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . . ±50mA
DC V_{CC} or GND Current, I_{CC} or I_{GND}
For Up to 4 Outputs Per Device, Add ±25mA For Each Additional Output . . . . . ±100mA

Power Dissipation Per Package, P_D
T_A = -55°C to +100°C (Package F) 500mW
T_A = +100°C to +125°C (Package F) . . . . . Derate Linearly at 8mW/°C to 300mW
Operating Temperature Range, T_A
Package Type F . . . . . -55°C to +125°C
Storage Temperature, T_{STG} . . . . . -65°C to +150°C
Lead Temperature (During Soldering)
At Distance 1/16in. ± 1/32in. (1.59mm ± 0.79mm)
From Case For 10s Max . . . . . +265°C
Unit Inserted Into a PC Board (Min Thickness 1/16in., 1.59mm)
With Solder Contacting Lead Tips Only. . . . . +300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Supply Voltage Range, V_{CC}
Unless Otherwise Specified, All Voltages Referenced to GND
T_A = Full Package Temperature Range
CD54AC Types . . . . . 1.5V to 5.5V
CD54ACT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O. . . . . 0V to V_{CC}

Operating Temperature, T_A . . . . . -55°C to +125°C
Input Rise and Fall Slew Rate, dt/dv
at 1.5V to 3V (AC Types) . . . . . 0ns/V to 50ns/V
at 3.6V to 5.5V (AC Types) . . . . . 0ns/V to 20ns/V
at 4.5V to 5.5V (AC Types) . . . . . 0ns/V to 10ns/V

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3893**