CDB42406

Evaluation Board For CS42406

Features

- Single-ended analog inputs and outputs
- CS8406 S/PDIF digital audio transmitter
- CS8416 S/PDIF digital audio receiver
- Header for optional external configuration of CS42406
- Header for external DSP serial audio I/O
- 3.3 V to 5.0 V Logic Interface
- 14 Pre-defined Board Setup Options
- Demonstrates recommended layout and grounding arrangements
- Windows compatible software interface to configure CS42406 and intra-board connections

ORDERING INFORMATION

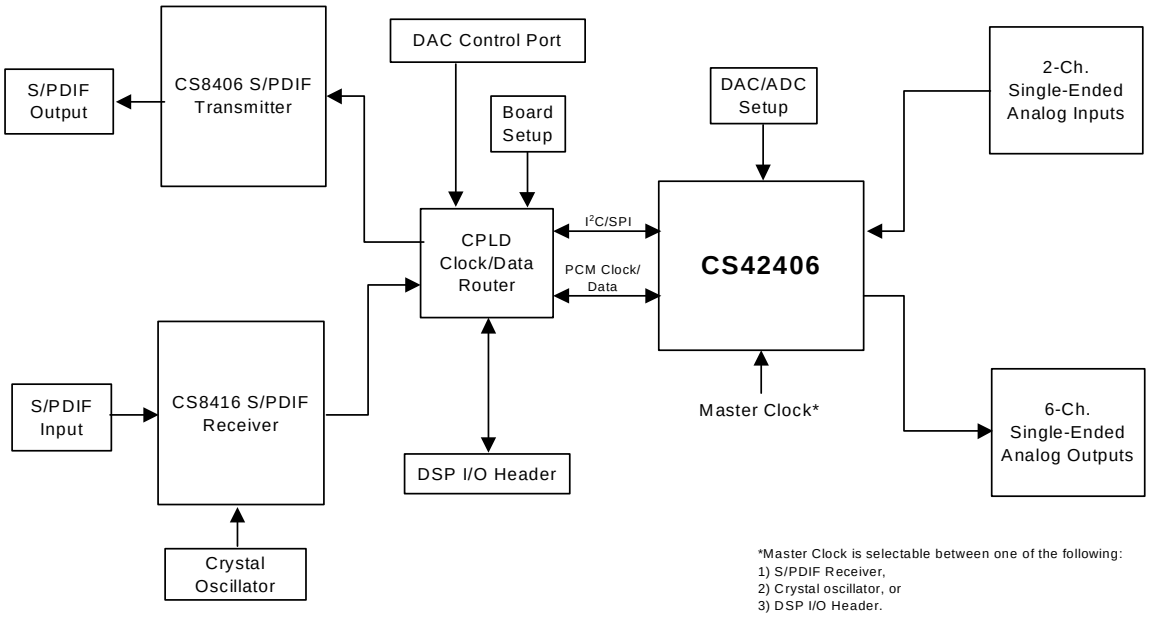
CDB42406 Evaluation Board

Description

The CDB42406 demonstration board is an excellent means for evaluating the CS42406 CODEC. Evaluation requires an analog/digital signal source and analyzer, and power supplies. Optionally, a Windows PC compatible computer may be used to evaluate the CS42406 DAC in control port mode.

System timing can be provided by the CS42406, by the CS8416 phase-locked to its S/PDIF input, by an I/O stake header or by an on-board oscillator. RCA phono jacks are provided for the CS42406 analog outputs and inputs. Digital data I/O is available via RCA phono or optical connectors to the CS8416 and CS8406. 14 predefined board setup options are selectable using a 4-position DIP switch.

The Windows software provides a GUI to make configuration of the DAC easy. The software communicates through the PC's parallel port to configure the control port registers so that all features of the CS42406 can be evaluated. The evaluation board may also be configured to accept external timing and data signals for operation in a user application during system development.



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Contacting Cirrus Logic Support

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1. SYSTEM OVERVIEW

The CDB42406 demonstration board is an excellent means for evaluating the CS42406 stereo CODEC. Analog and digital audio signal interfaces are provided, as well as a DB-25 computer parallel port interface for use with the supplied Windows configuration software.

The CDB42406 schematic set has been partitioned into 10 pages and is shown in Figures 16 through 25.

1.1 CS42406 Audio CODEC

A complete description of the CS42406 is included in the CS42406 product data sheet.

1.2 CS8406 Digital Audio Transmitter

The operation of the CS8406 transmitter (see Figure 18) and a discussion of the digital audio interface are included in the CS8406 data sheet.

The CS8406 converts the PCM data generated by the CS42406 to the standard S/PDIF data stream. The CS8406 operates in slave mode and only accepts a 256Fs master clock on the OMCK input pin. The serial audio input data for the CS8406 is received from the serial audio output of the CS42406. Digital Interface format selection of either Left Justified or I^2S can be made via the I2S/LJ position on switch S3 (see Table 2 for switch control options).

1.3 CS8416 Digital Audio Receiver

The operation of the CS8416 receiver (see Figure 17) and a discussion of the digital audio interface are included in the CS8416 data sheet.

The CS8416 converts the input S/PDIF data stream into PCM data for the CS42406. The CS8416 operates in master mode only. Digital Interface format selection of either Left Justified or I^2S can be made via the I2S or LJ position on S1(see Table 2 for switch control options).

The CS8416 contains an internal input multiplexer which must be set to receive the appropriate stream from the Optical or Coaxial input connector. This is done via the Coaxial or Optical position on switch S1.

1.4 Canned Oscillator

Oscillator Y1 provides a System Clock. This clock can be routed through the CS8416 out the RMCK pin when the S/PDIF input is disconnected (refer to the CS8416 data sheet for details on OMCK operation). To use the canned oscillator as the source of the MCLK signal, select from one of the pre-defined options, detailed in section 1.7, using the SW[3:0] positions on switch S4.

The oscillator is mounted in pin sockets, allowing easy removal or replacement. The board is shipped with a 12.2880 MHz crystal oscillator stuffed at Y1.

1.5 Analog Input

RCA connectors supply the CS42406 analog inputs through unity gain, AC-coupled single-ended circuits. A 1 Vrms single-ended signal will drive the CS42406 inputs to full scale.

1.6 Analog Outputs

The CS42406 analog outputs are routed through a single-pole RC filter. The corner frequency can be extended to 190 kHz by simply removing one of the 1500 pF filter capacitors.

1.7 CPLD Board Setup

The CPLD (U9) controls all digital signal routing between the CS42406, CS8416, CS8406, AUDIO MCLK (Y1), and DSP I/O HDR. The user may choose from 14 clock/data routing options by setting certain combinations of switch S4. See sections 1.7.1 through 1.7.4 for a description of each mode. Any combination can be realized in either stand-alone or control port mode.

1.7.1 S/PDIF IN & S/PDIF OUT (Setup 0 - Setup 2)

There are 3 different setup options for routing MCLK, LRCK and SCLK for S/PDIF input and output conversion. These options allow the user to choose between 3 different masters for the ADC subclocks. Should the CS8416 lose lock to the S/PDIF input, the RMCK will automatically switch from the PLL to the OMCK input (see the CS8416 datasheet for details). The CS8406 is always clocked from the same source as the ADC.

1.7.1a Setup 0

Using the recovered clock from the S/PDIF input data stream, the CS8416 masters all clocks for the ADC and all clocks and data for the DAC. For implementation of this setup option, set DIP switch S4 (SW[3:0]) to ‘0000’b.

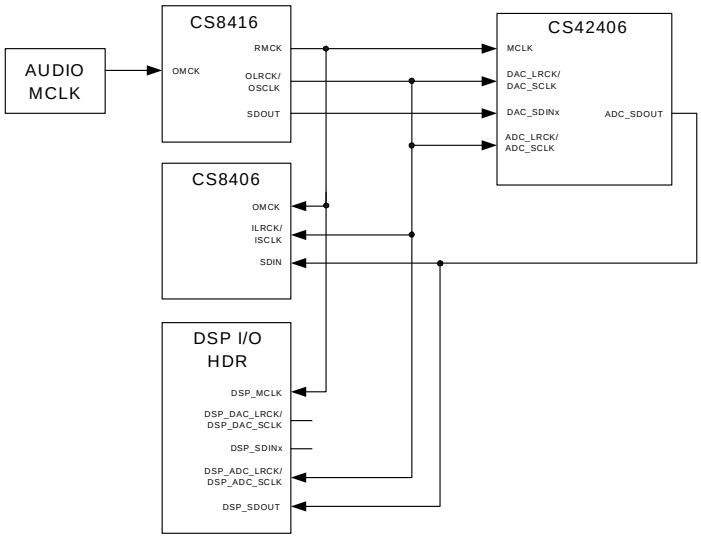

Figure 1. S/PDIF IN/OUT - Setup 0

1.7.1b Setup 1

Using the recovered clock from the S/PDIF input data stream, the CS8416 masters MCLK, subclocks and data for the DAC. A DSP connected to the DSP I/O HDR masters the subclocks for the ADC and CS8406. For implementation of this setup option, set DIP switch S4 (SW[3:0]) to ‘0001’b.

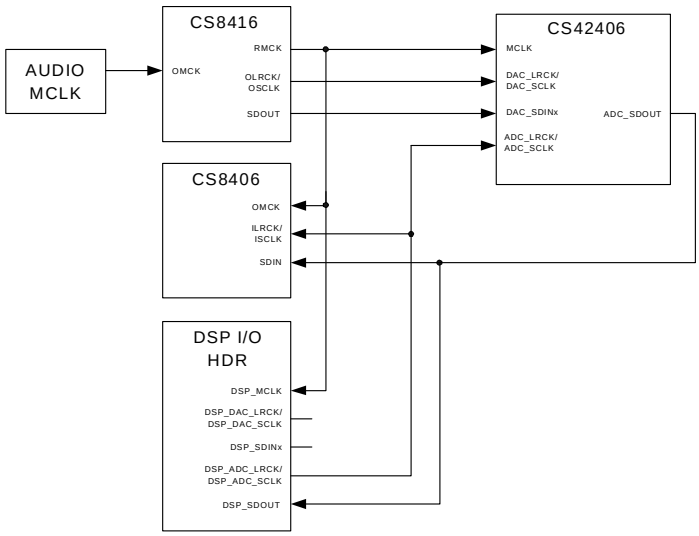

Figure 2. S/PDIF IN/OUT - Setup 1

1.7.1c Setup 2

Using the recovered clock from the S/PDIF input data stream, the CS8416 masters MCLK, subclocks and data for the DAC. The ADC masters its own subclocks. For implementation of this setup option, set DIP switch S4 (SW[3:0]) to ‘0010’b.

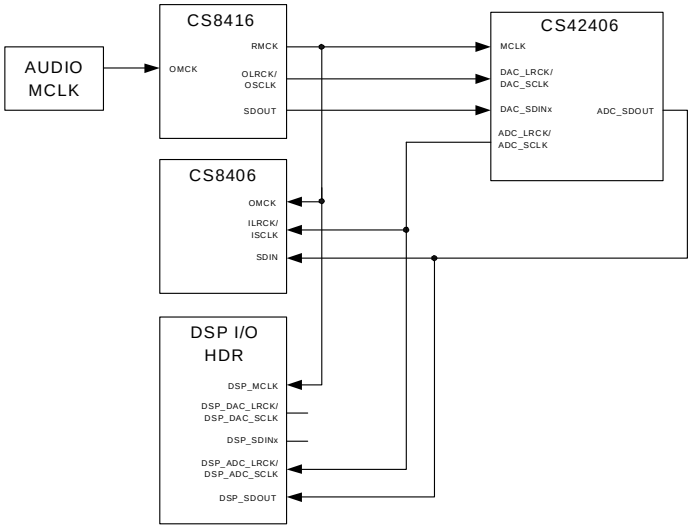

Figure 3. S/PDIF IN/OUT - Setup 2

1.7.2 Digital Loopback (Setup 3 - Setup 6)

There are 4 different setup options for routing MCLK, LRCK and SCLK for digital loopback. These setup configurations allow analog input/output analysis without the need for a digital signal analyzer/source. These options also allow the user to choose between 2 different MCLK and 2 different subclock sources for the ADC/DAC.

1.7.2a Setup 3

Using the on-board crystal oscillator, AUDIO MCLK, the CS42406 ADC masters the subclocks and data for the DAC. For implementation of this setup option, set DIP switch S4 (SW[3:0]) to ‘0011’b.

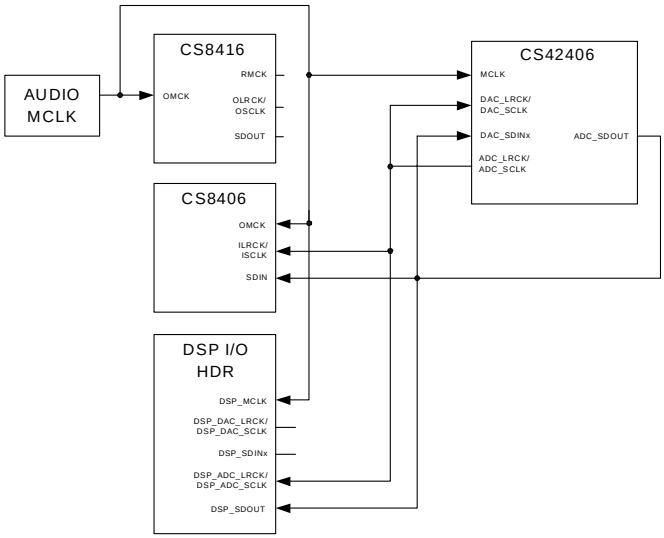

Figure 4. Digital Loopback - Setup 3

1.7.2b Setup 4

Using the on-board crystal oscillator, AUDIO MCLK, a DSP connected to DSP I/O HDR masters the subclocks for the ADC/DAC. For implementation of this setup option, set DIP switch S4 (SW[3:0]) to ‘0100’b.

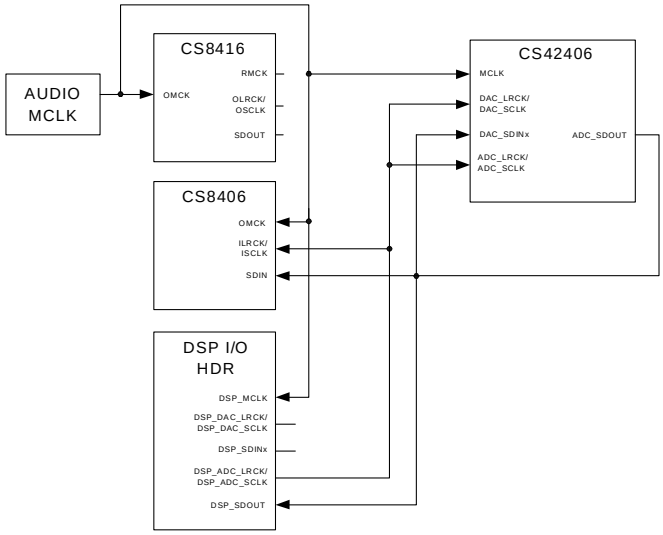

Figure 5. Digital Loopback - Setup 4

1.7.2c Setup 5

Using the master clock from an external DSP connected to the DSP I/O HDR, DSP_MCLK, the CS42406 ADC masters the subclocks and data for the DAC. For implementation of this setup option, set DIP switch S4 (SW[3:0]) to ‘0101’b.

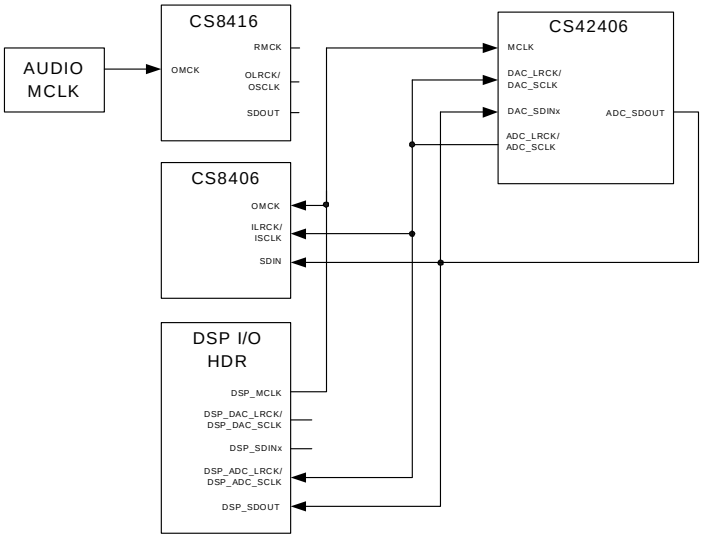

Figure 6. Digital Loopback - Setup 5

1.7.2d Setup 6

An external DSP connected to DSP I/O HDR, masters all clocks for the ADC/DAC. For implementation of this setup option, set DIP switch S4 (SW[3:0]) to ‘0110’b.

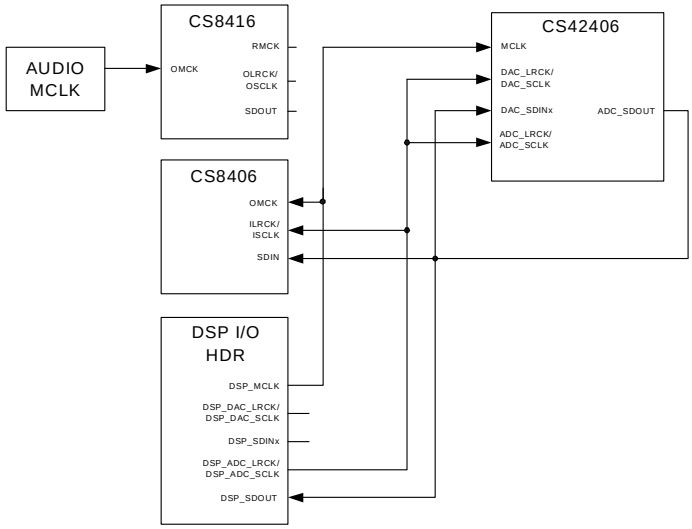

Figure 7. Digital Loopback - Setup 6

1.7.3 DSP Routing

There are 6 different setup options for routing MCLK, LRCK and SCLK for DSP control. These options allow either shared or independent control over the subclocks for the DAC and ADC. The user may also choose between 2 different MCLK sources.

1.7.3a Setup 7

An external DSP connected to DSP I/O HDR masters all clocks for the ADC/DAC and provides data to the DAC. Subclocks for the ADC/DAC are input via DSP_ADC_LRCK and DSP_ADC_SCLK. For implementation of this setup option, set DIP switch S4 (SW[3:0]) to ‘0111’b.

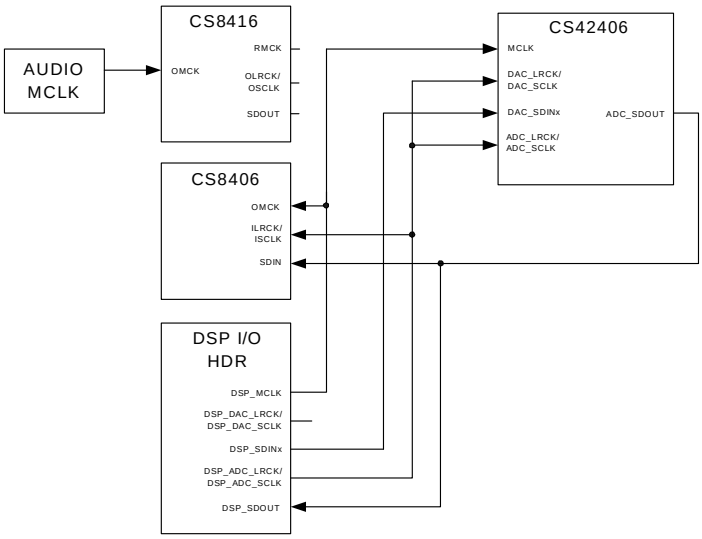

Figure 8. DSP Routing - Setup 7

1.7.3b Setup 8

Using the on-board crystal oscillator, AUDIO MCLK, a DSP connected to DSP I/O HDR masters the subclocks for the ADC/DAC and provides data to the DAC. Subclocks for the ADC/DAC are input via DSP_ADC_LRCK and DSP_ADC_SCLK. For implementation of this setup option, set DIP switch S4 (SW[3:0]) to ‘1000’b.

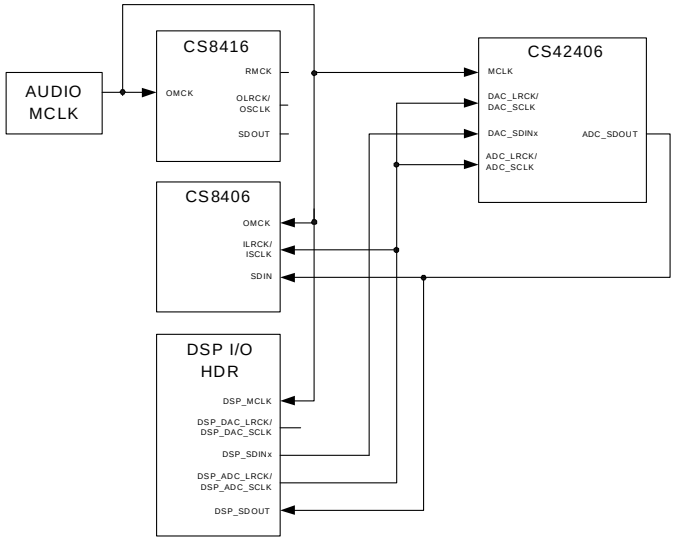

Figure 9. DSP Routing - Setup 8

1.7.3c Setup 9

Using the on-board crystal oscillator, AUDIO MCLK, a DSP connected to DSP I/O HDR masters the subclocks for the ADC/DAC and provides data to the DAC. Subclocks for the ADC are input via DSP_ADC_LRCK and DSP_ADC_SCLK while subclocks for the DAC are input via DSP_DAC_LRCK and DSP_DAC_SCLK. This allows independent control of the sample rate for the ADC and DAC. For implementation of this setup option, set DIP switch S4 (SW[3:0]) to ‘1001’b.

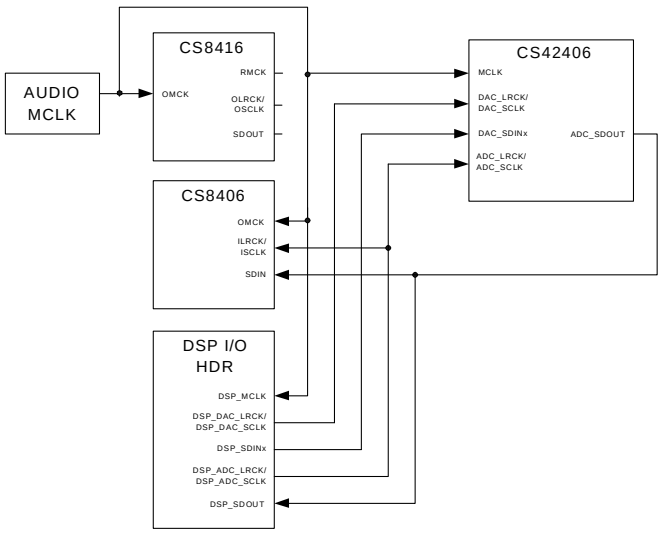

Figure 10. DSP Routing - Setup 9

1.7.3d Setup 10

A DSP connected to DSP I/O HDR masters all clocks for the ADC/DAC and provides data to the DAC. Subclocks for the ADC are input via DSP_ADC_LRCK and DSP_ADC_SCLK while subclocks for the DAC are input via DSP_DAC_LRCK and DSP_DAC_SCLK. This allows independent control of the sample rate for the ADC and DAC. For implementation of this setup option, set DIP switch S4 (SW[3:0]) to ‘1010’b.

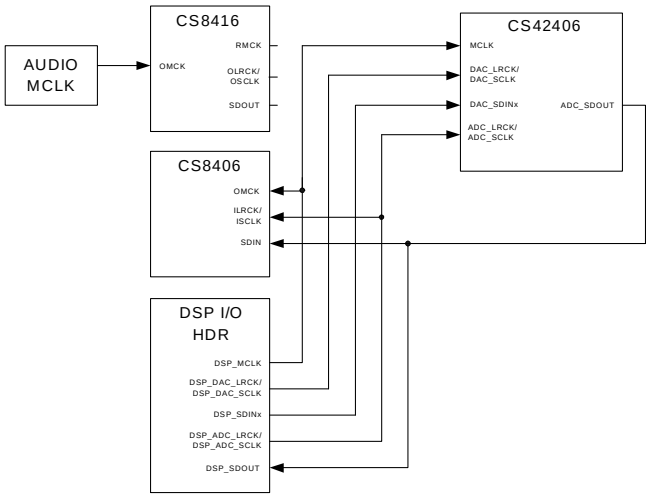

Figure 11. DSP Routing - Setup 10

1.7.3e Setup 11

Using the on-board crystal oscillator, AUDIO MCLK, a DSP connected to DSP I/O HDR masters the subclocks for the DAC and provides data to the DAC. Using the on-board crystal oscillator, AUDIO MCLK, the CS42406 ADC masters its subclocks and are output onto DSP_ADC_LRCK and DSP_ADC_SCLK. The subclocks for the DAC are input via DSP_DAC_LRCK and DSP_DAC_SCLK. This allows independent control of the sample rate for the ADC and DAC. For implementation of this setup option, set DIP switch S4 (SW[3:0]) to ‘1011’b.

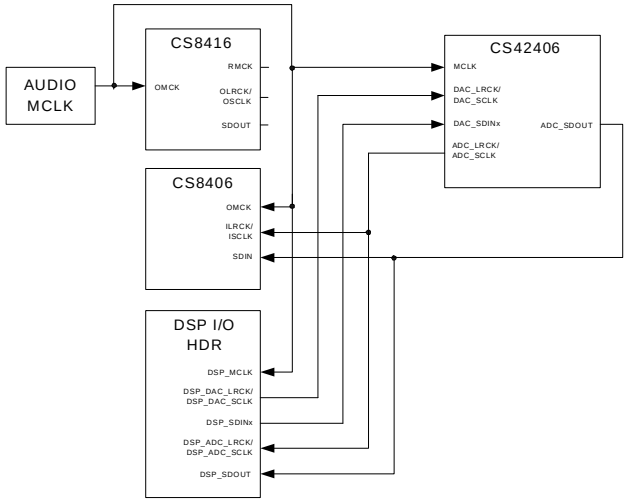

Figure 12. DSP Routing - Setup 11

1.7.3f Setup 12

A DSP connected to DSP I/O HDR masters all clocks for the DAC and provides data to the DAC. Using a DSP connected to DSP I/O HDR, the CS42406 ADC masters its subclocks and are output onto DSP_ADC_LRCK and DSP_ADC_SCLK. The subclocks for the DAC are input via DSP_DAC_LRCK and DSP_DAC_SCLK. This allows independent control of the sample rate for the ADC and DAC. For implementation of this setup option, set DIP switch S4 (SW[3:0]) to '1100'b.

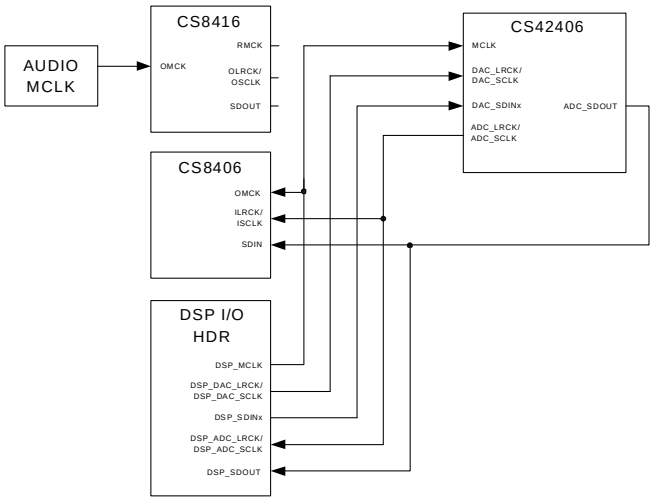

Figure 13. DSP Routing - Setup 12

1.7.4 No Routing

The remaining setup options will tri-state all clock/data output on the CPLD with the exception of the ADC_SDOUT from the CS42406 to the inputs of the CS8406 and DSP_I/O_HDR.

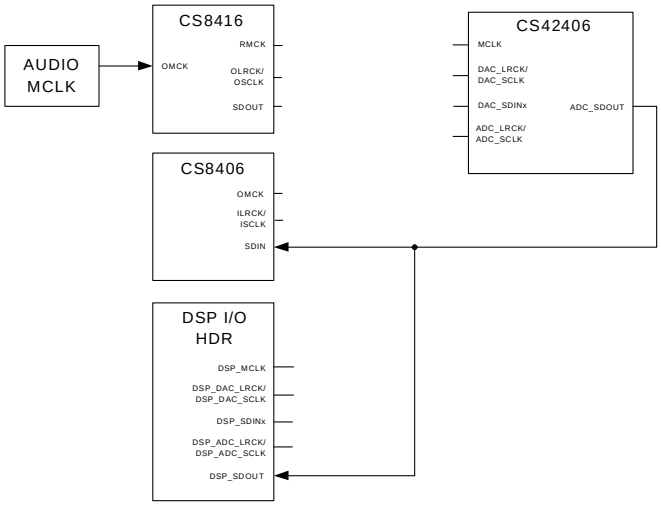

Figure 14. No Routing

1.8 Stand-Alone Control

Switches S1-S4 allow signal routing and configuration of the CDB42406. Switch S1 controls the interface format of the CS8416 and allows selection between the OPTICAL and COAXIAL S/PDIF inputs. The DAC portion of the CS42406 may operate in either stand-alone (configured using switch S2) or control port mode (configured via the PC Parallel Port through a graphical user interface). The ADC portion of the CS42406 operates in stand-alone mode at all times and must be configured using switch S3. Switch S4 controls the routing of all clocks and data. See section 1.7 for a list of the various stand-alone options available. After setting any of these switches, the user must assert a reset by pressing the RESET button (S5).

Operation in stand-alone mode requires the parallel port cable to remain disconnected from the DB-25 connector (J24). Connecting a cable to the connector will enable the PC control port, automatically disabling various controls on switch S2.

1.9 PC Parallel Port Control

A graphical user interface is included with the CDB42406 to allow easy manipulation of the DAC registers of the CS42406. Connecting a cable to the DB-25 connector (J24) will enable the PC control port, automatically disabling various controls on switch S2.

1.10 External Control Headers

The evaluation board has been designed to allow interfacing with external systems via the headers J15 and J26.

The 32-pin header, J15, provides access to the serial audio signals required to interface with a DSP (see Figure 24). These signals are routed based on the setting of switch S4. See “CPLD Board Setup” in section 1.7 for various setup options for DSP routing.

The 6-pin header, J26, allows the user bidirectional access to the SPI/I^2C control signals. The signals on J26 default to outputs. When a cable is connected to the DB-25 connector (J24), the header (J26) may be used as an input. In this case, the control signals on J26 are routed to the corresponding control pins on the CS42406 and external control signals may be applied.

1.11 Power

Power must be supplied to the evaluation board through at least the +5.0 V binding post, (J1). Jumpers J3 and J6 connect the VD and VA supply, respectively, to a fixed +5.0 V or +3.3 V supply or to two separate binding posts (J4 and J7) for variable voltage settings. Jumper J5 allows the user to connect the VLS and VLC supplies of the CS42406 to a fixed +5.0 V or +3.3 V supply. All voltage inputs must be referenced to the single black banana-type ground connector (see Figure 25).

WARNING:Please refer to the CS42406 data sheet for allowable voltage levels.

1.12 Grounding and Power Supply Decoupling

The CS42406 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 15 provides an overview of the connections to the CS42406, Figure 26 shows the component placement, Figure 27 shows the top layout, and Figure 28 shows the bottom layout. The decoupling capacitors are located as close to the CS42406 as possible. Extensive use of ground plane fill in the evaluation board yields large reductions in radiated noise.

CONNECTOR	Reference Designator	INPUT/OUTPUT	SIGNAL PRESENT
+5V	J1	Input	+5.0 V Power Supply
GND	J2	Input	Ground Reference
VD	J4	Input	+3.3 V to +5.0 V Variable Power Supply for VD
VA	J7	Input	+3.3 V to +5.0 V Variable Power Supply for VA
RX-COAX	J10	Input	CS8416 digital audio input via coaxial cable
RX-OPT	OPT1	Input	CS8416 digital audio input via optical cable
TX-COAX	J18	Output	CS8406 digital audio output via coaxial cable
TX-OPT	OPT2	Output	CS8406 digital audio output via optical cable
PC Port	J24	Input/Output	Parallel connection to PC for SPI / I^2C control port signals
DSP HEADER	J15	Input/Output	I/O for Clocks & Data
EXT CTRL I/O	J26	Input/Output	I/O for external SPI / I^2C control port signals.
AINL AINR	J25 J27	Input	RCA phono jacks for analog input signal to CS42406
AOUTA1 AOUTB1 AOUTA2 AOUTB2 AOUTA3 AOUTB3	J8 J11 J13 J16 J19 J22	Output	RCA phono jacks for analog outputs

Table 1. System Connections

JUMPER / SWITCH	PURPOSE	IDENTIFIER	POSITION	FUNCTION SELECTED
S/PDIF In Setup (S1)	Optical or Coaxial S/PDIF Input Select	-	*OPTICAL COAXIAL	Optical Input Coaxial Input
S/PDIF In Setup (S1)	I^2S or Left Justified Input Select	-	*LJ I2S	Left Justified S/PDIF Input I^2S S/PDIF Input
J3	Selects source of voltage for the VD supply	-	VD_IN +3.3V *+5V	Voltage source is J4 binding post Voltage source is +3.3 V regulator Voltage source is +5 V regulator
J5	Selects source of voltage for the VLS and VLC supplies	-	+3.3V *+5V	Voltage source is +3.3 V regulator Voltage source is +5 V binding post (J1)
J6	Selects source of voltage for the VA supply	-	VA_IN +3.3V *+5V	Voltage source is J7 binding post Voltage source is +3.3 V regulator Voltage source is +5 V binding post (J1)
DAC SETUP (S2)	DAC Speed Mode Select	DAC_Mx	*00 01 10 11	Single-Speed Mode, w/out De-emphasis Single-Speed Mode, with De-emphasis Double-Speed Mode Quad-Speed Mode
DAC SETUP (S2)	Interface Format Select	DIFx	*00 01 10 11	Left Justified, up to 24-bit data I^2S, up to 24-bit data Right Justified 16-bit data Right Justified 24-bit data
DAC SETUP (S2)	Resets DAC	$\overline{\text{RST\_DAC}}$	0 *1	DAC reset is enabled DAC reset is disabled
ADC SETUP (S3)	ADC Speed Mode Select	ADC_Mx	00 01 10 *11	Clock Master, Single-Speed Mode Clock Master, Double-Speed Mode Clock Master, Quad-Speed Mode Clock Slave, All Speed Modes
ADC SETUP (S3)	MCLK/LRCK Ratio Select	384x/$\overline{256x}$	*0 1	MCLK/LRCK ratio is 256 MCLK/LRCK ratio is 384
ADC SETUP (S3)	ADC and CS8406 Interface Format Selection	I2S/$\overline{\text{LJ}}$	0 *1	Left Justified, up to 24-bit data I^2S, up to 24-bit data
ADC SETUP (S3)	Powerdown ADC	$\overline{\text{PDN\_ADC}}$	0 *1	ADC is powered down ADC is powered up
J9, J12, J14, J17, J20, J23	Mute Circuit Connection	-	*Shunted Open	Connects Mute Circuit to AOUTxx Disconnects Mute Circuit from AOUTxx

*Default factory settings

Table 2. Jumper/Switch Settings

2. BLOCK DIAGRAM

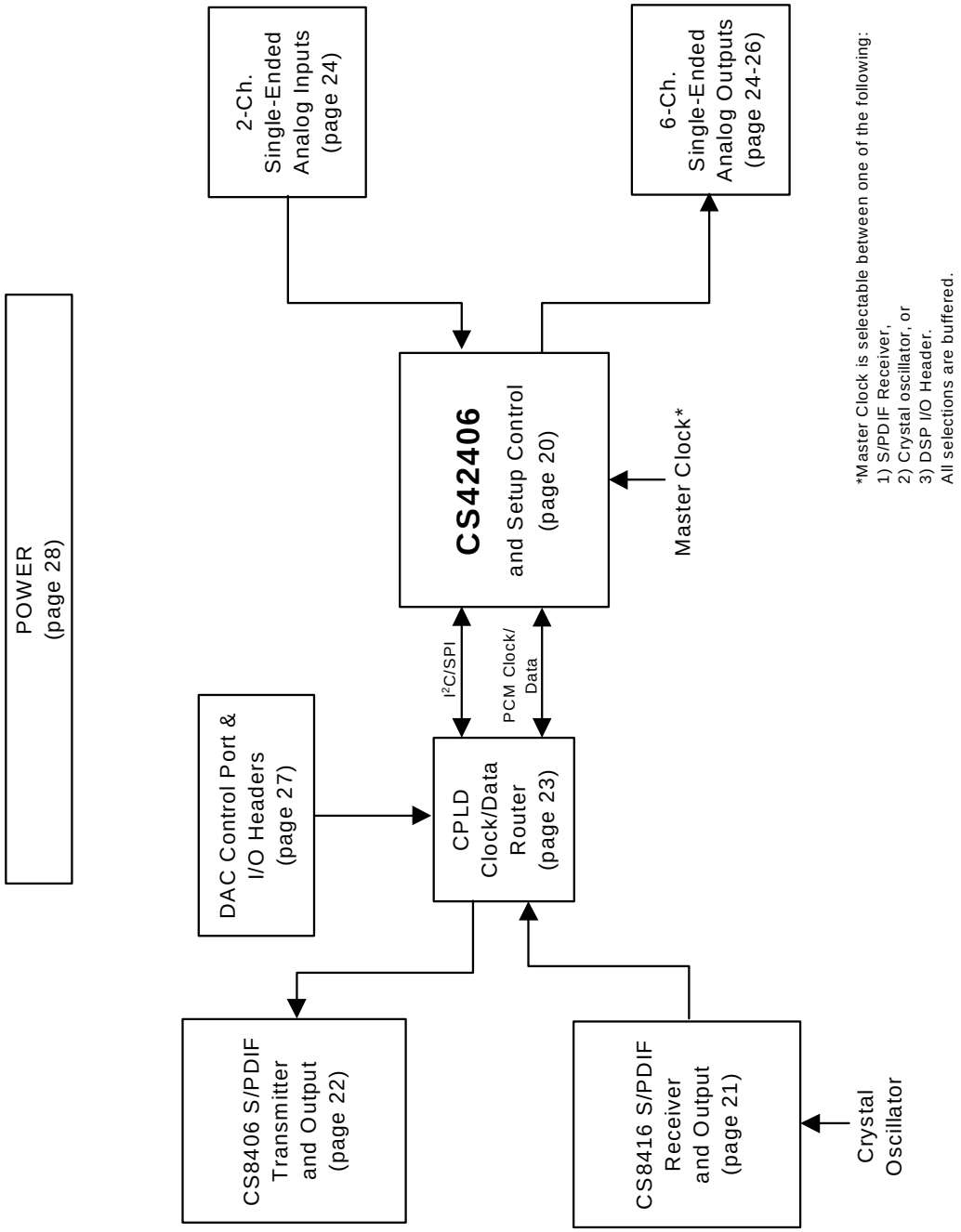

Figure 15. Block Diagram

3. SCHEMATICS

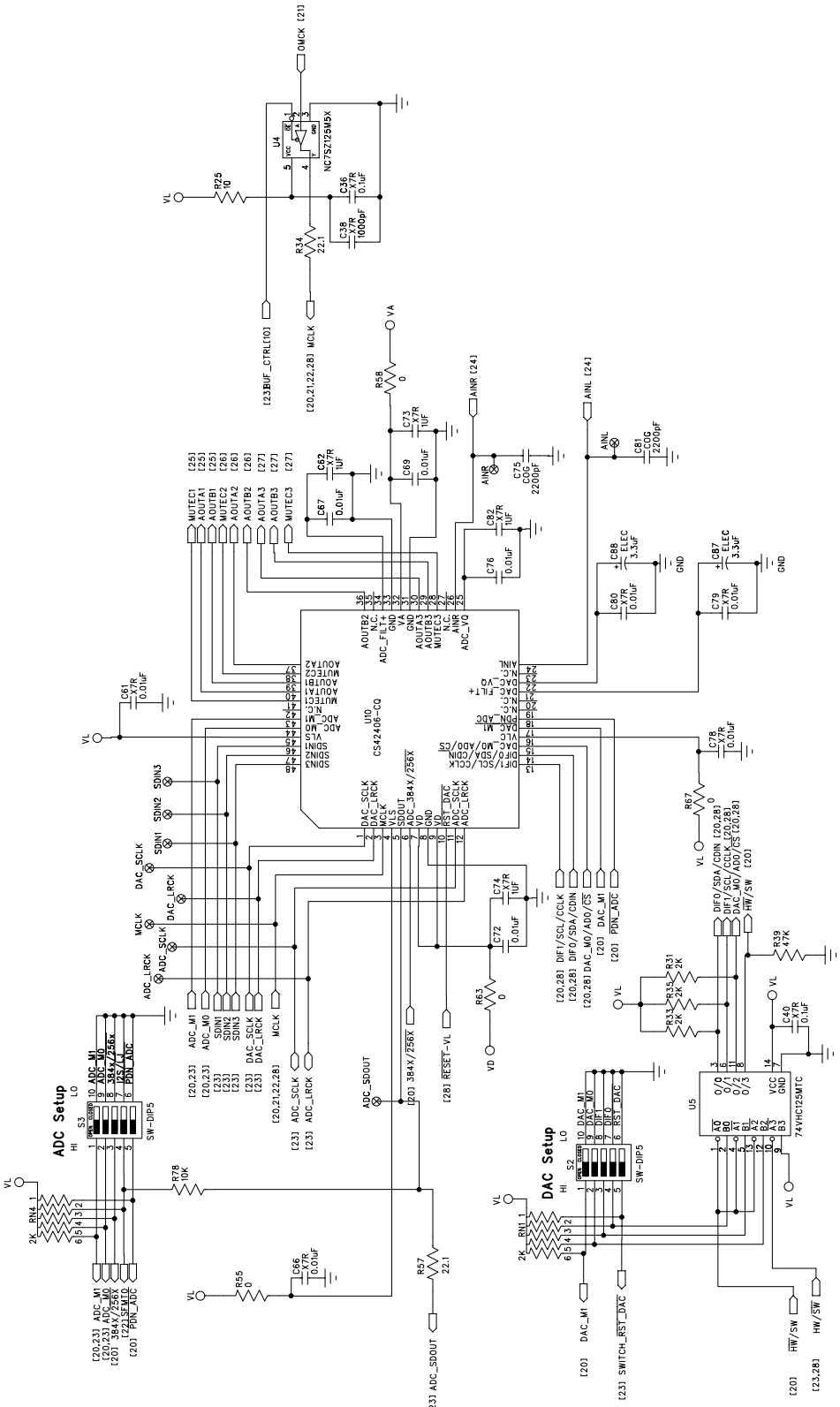

Figure 16. CS42406

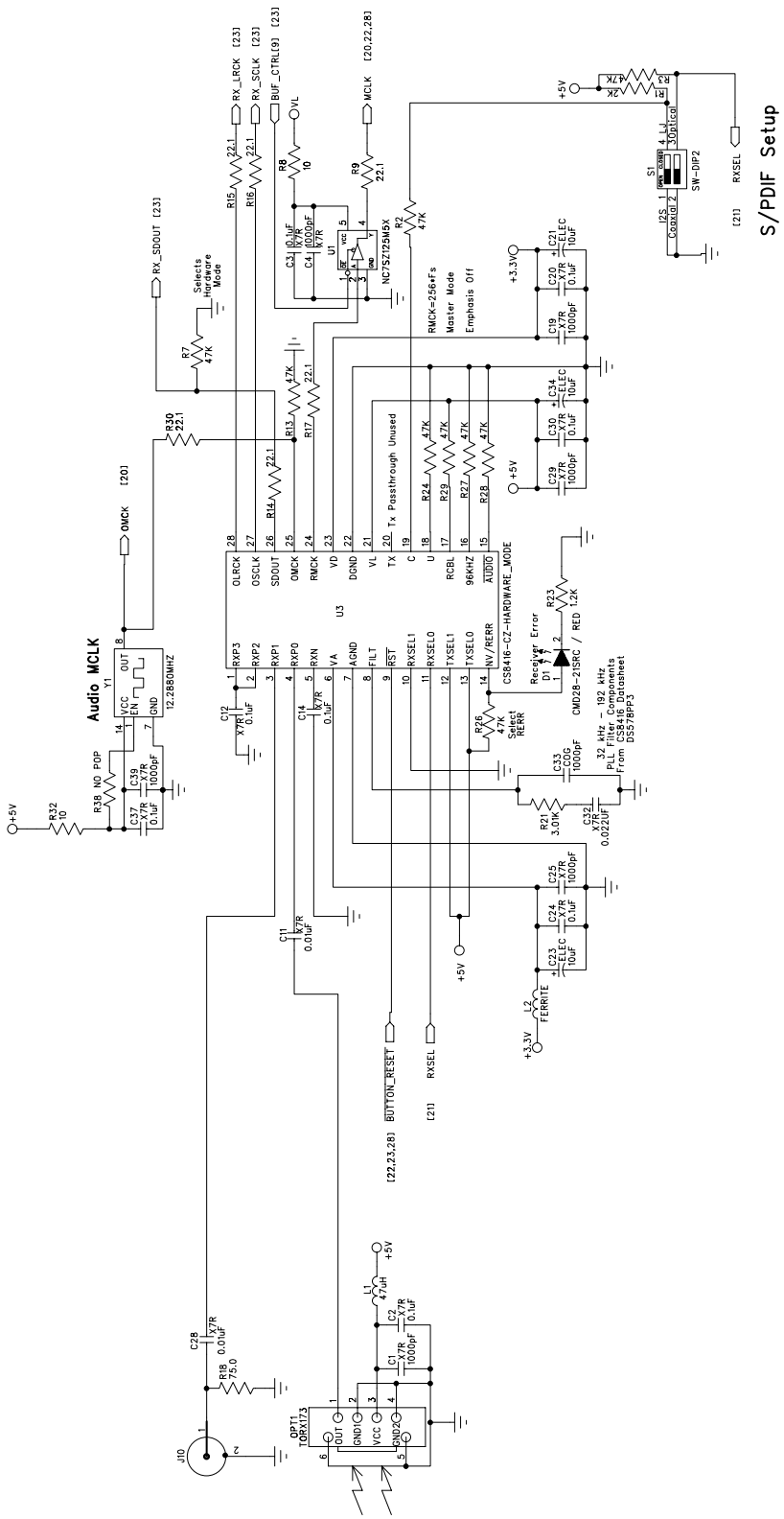

Figure 17. S/PDIF Input

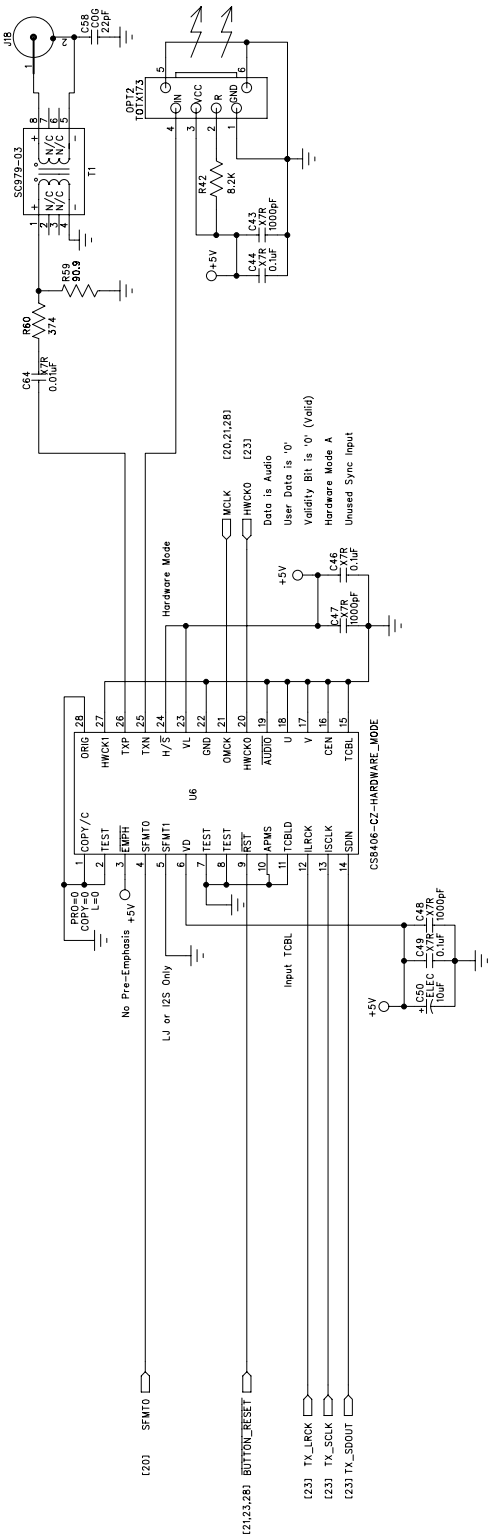

Figure 18. S/PDIF Output

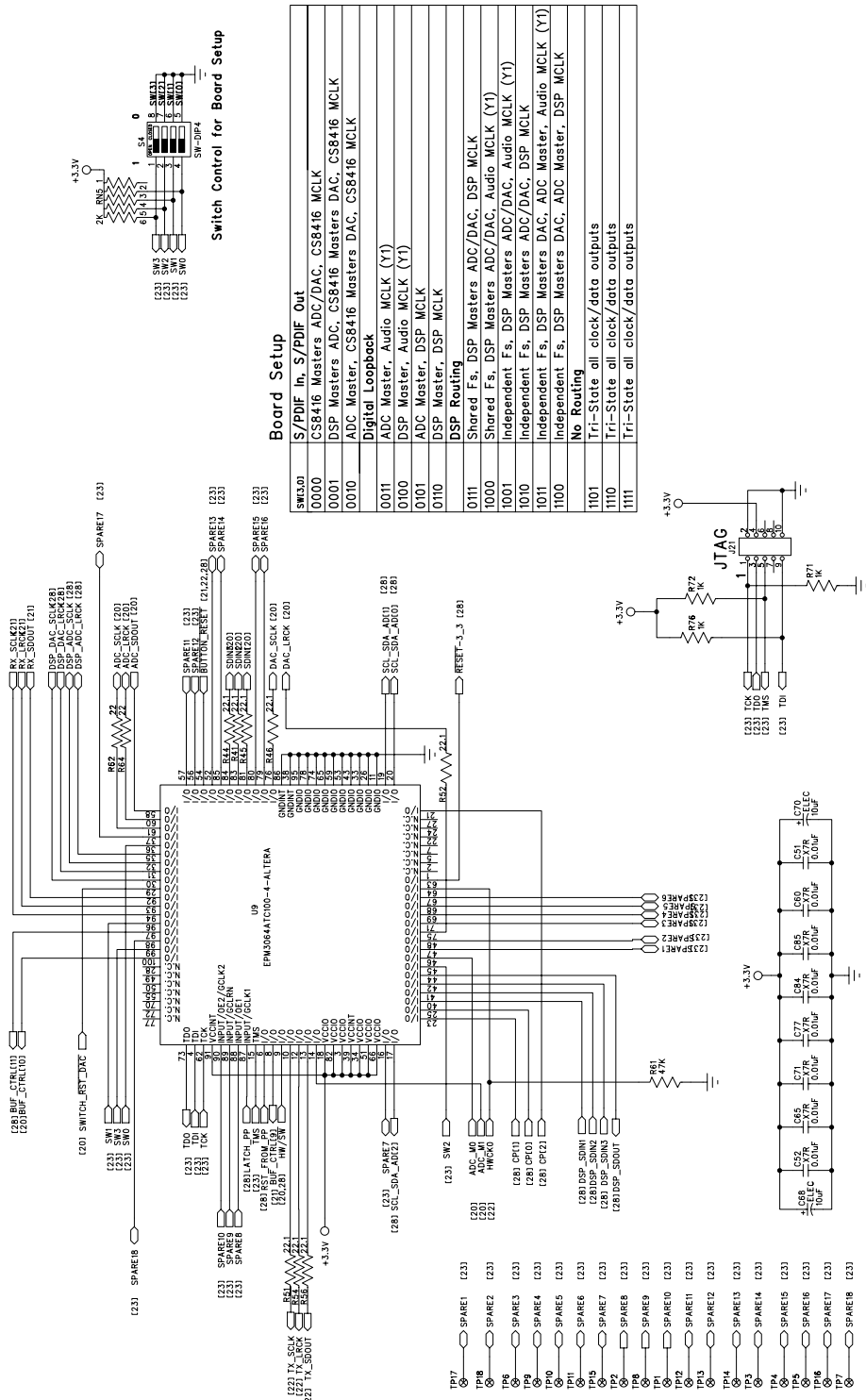

Figure 19. CPLD

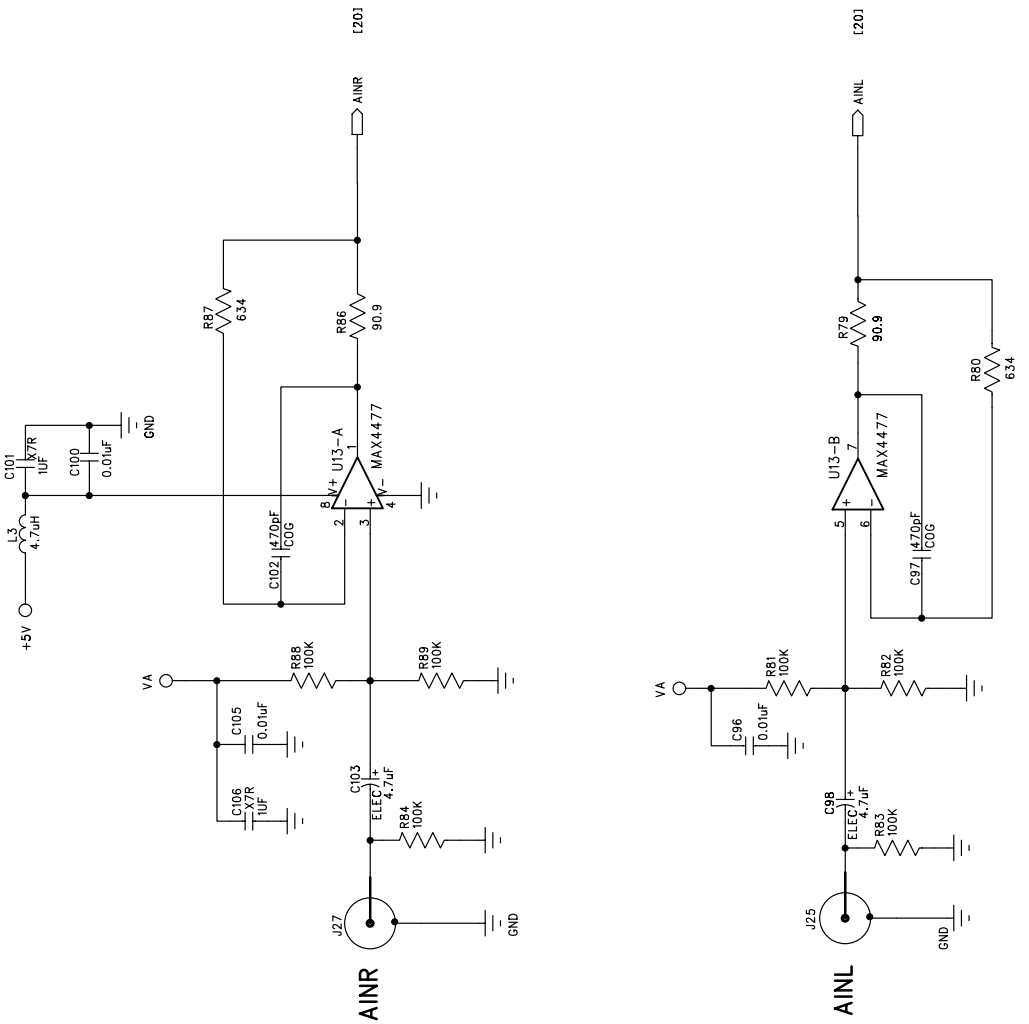

Figure 20. Analog Input

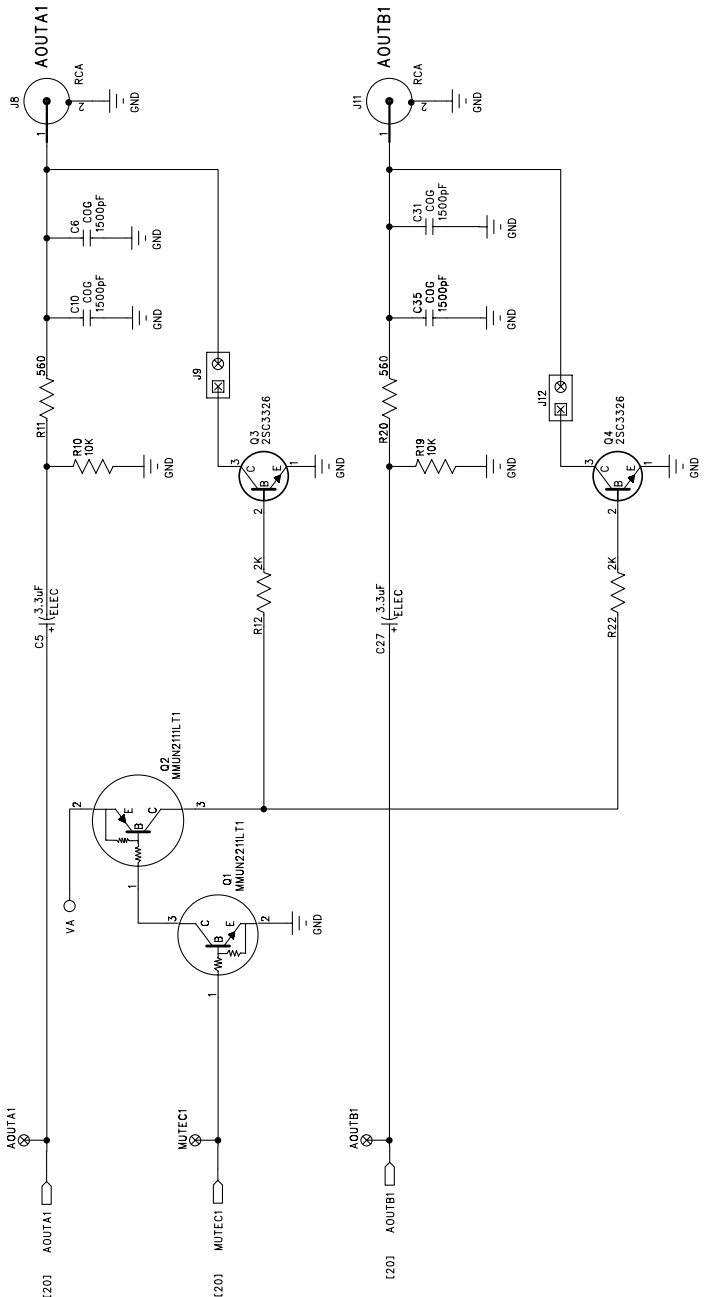

Figure 21. Ch. 1 Analog Output

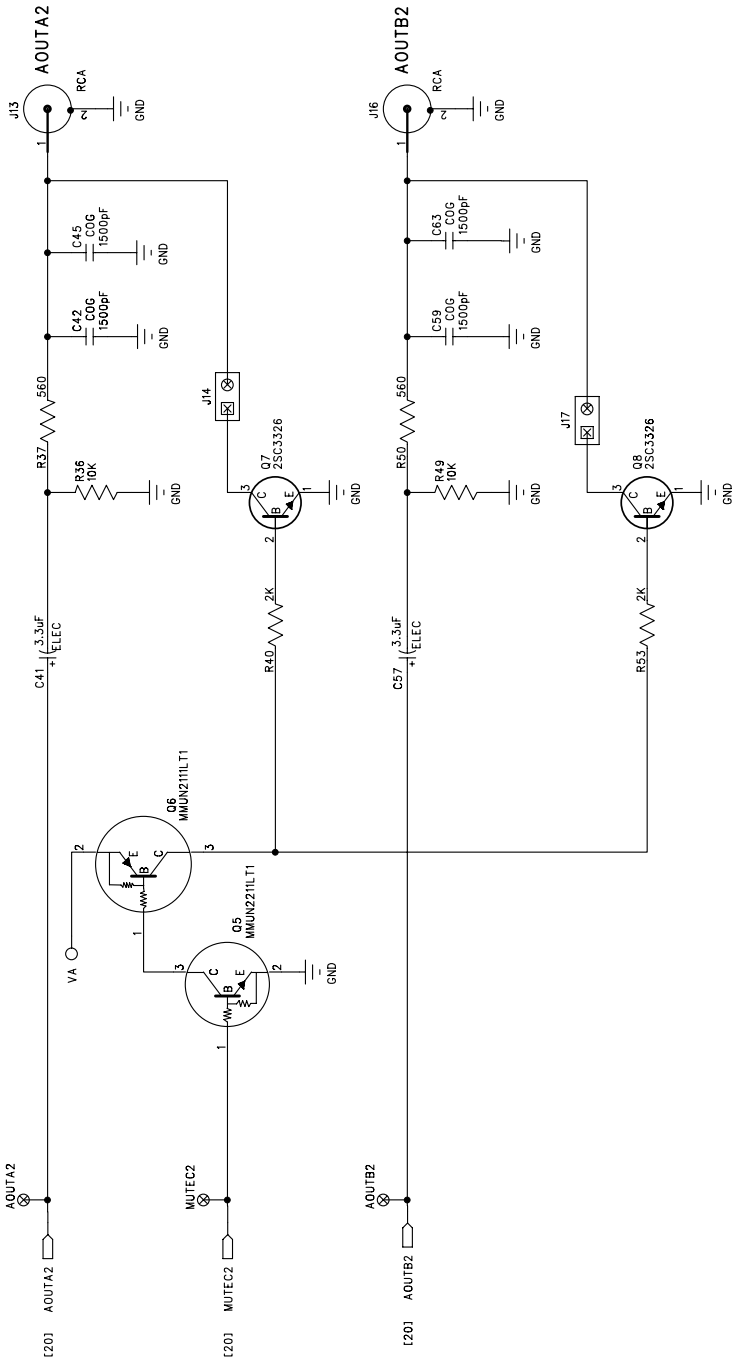

Figure 22. Ch. 2 Analog Output

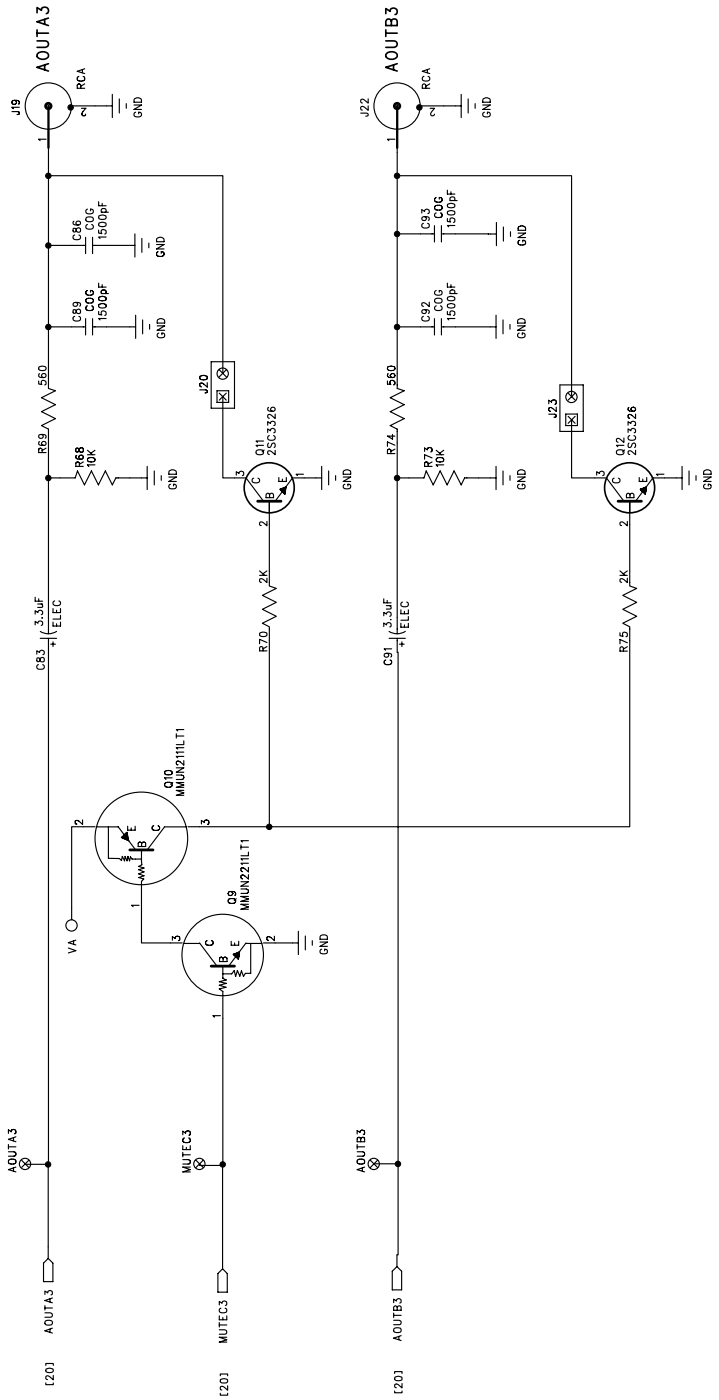

Figure 23. Ch. 3 Analog Output

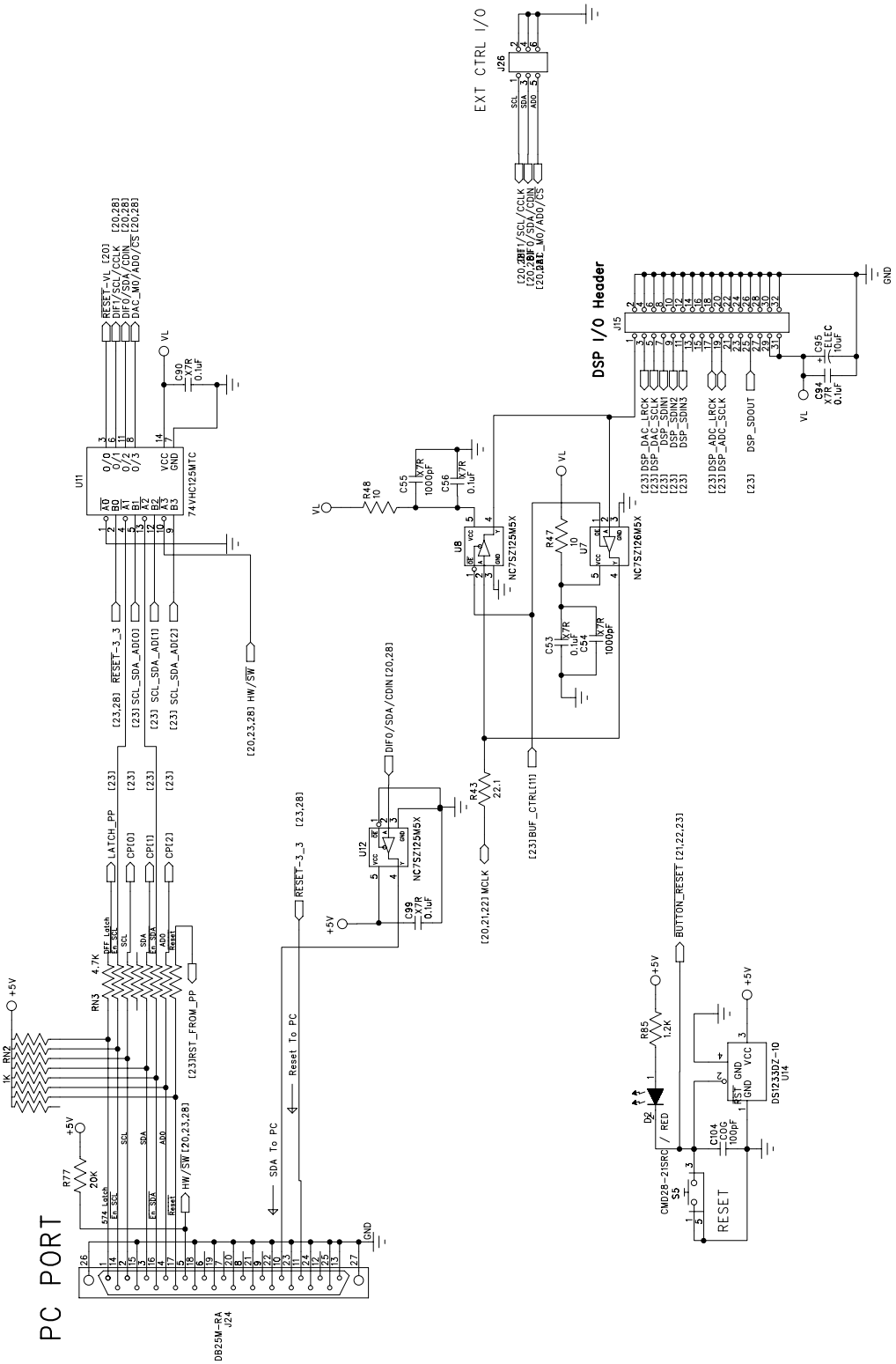

Figure 24. DAC Control Port and I/O Headers

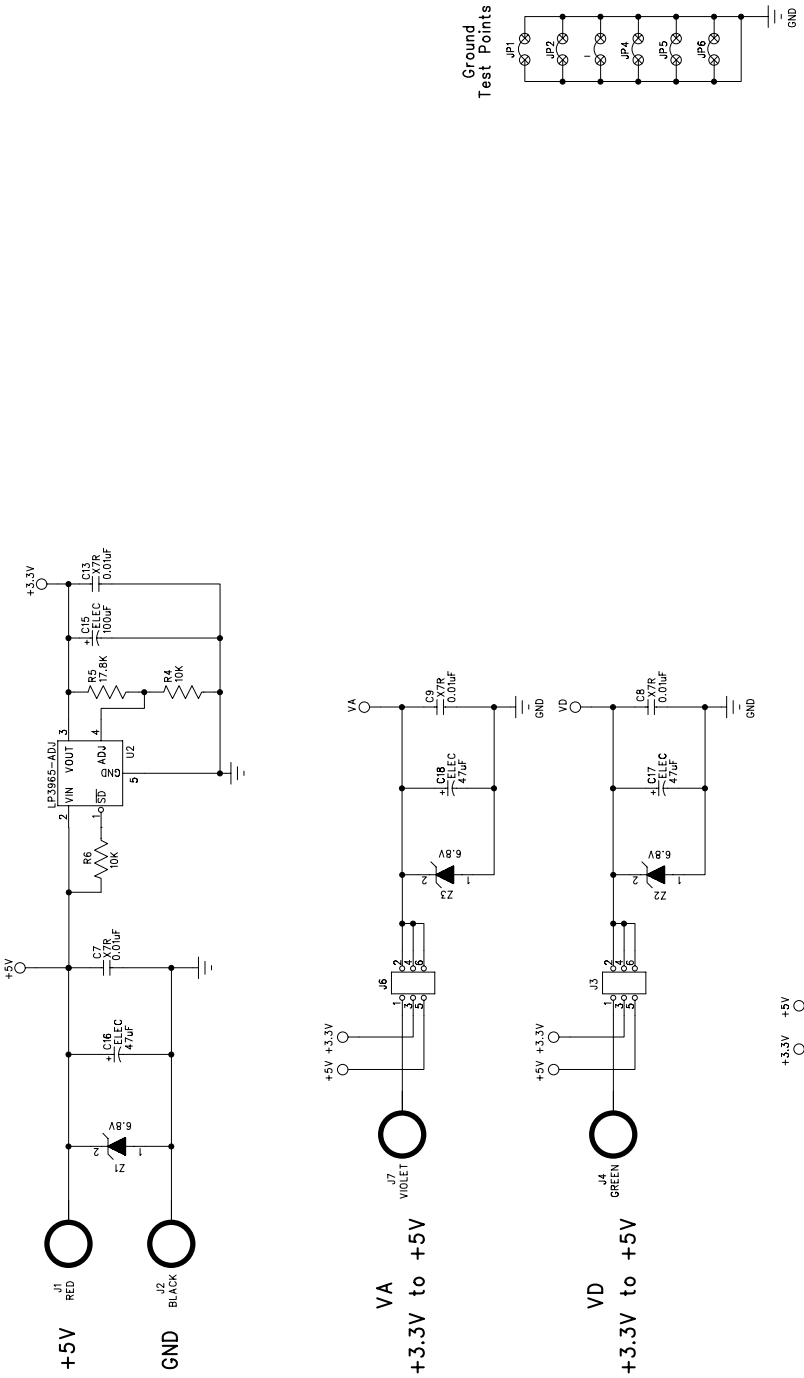

Figure 25. Power

4. LAYOUT

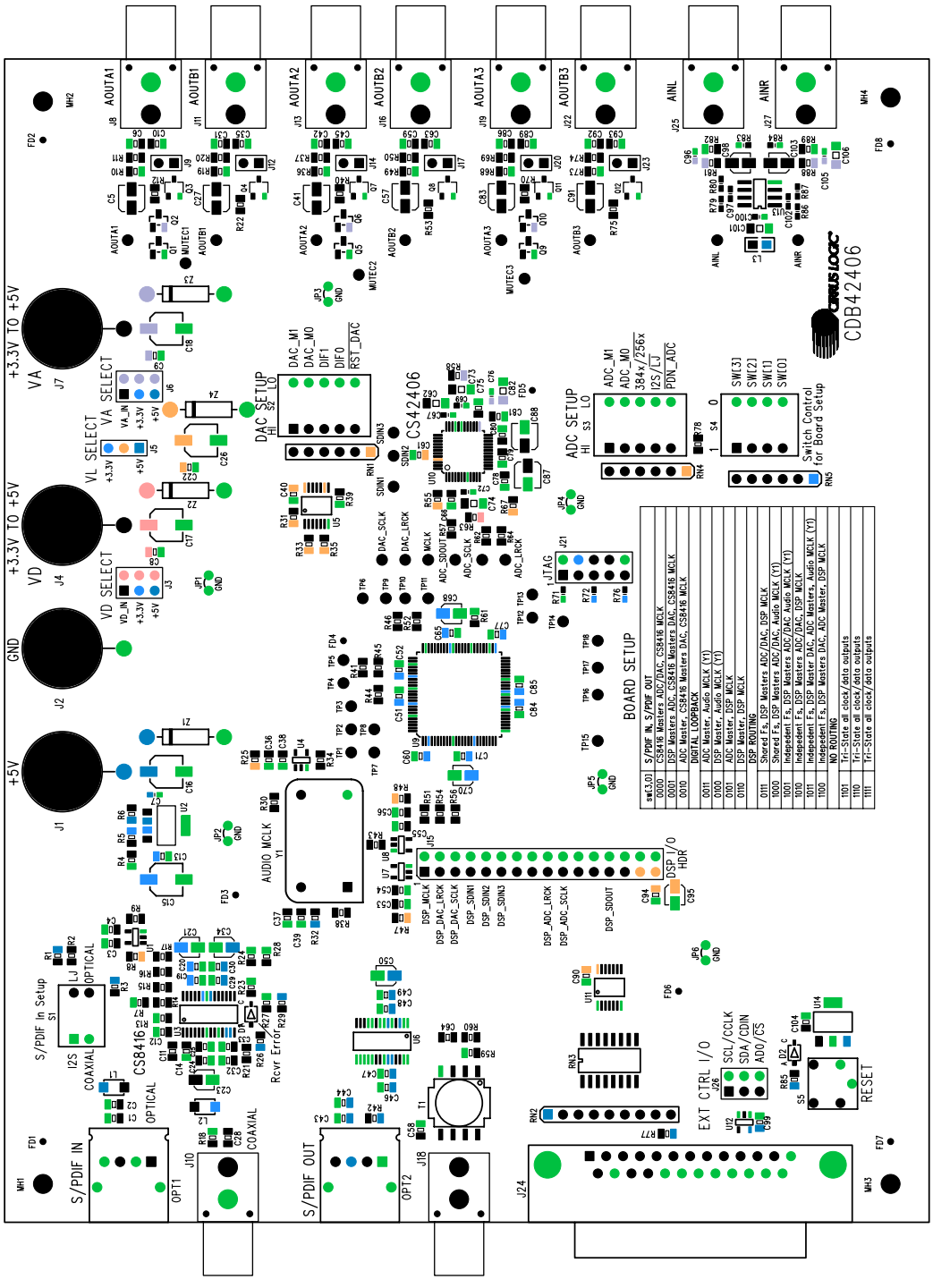

Figure 26. Silk Screen

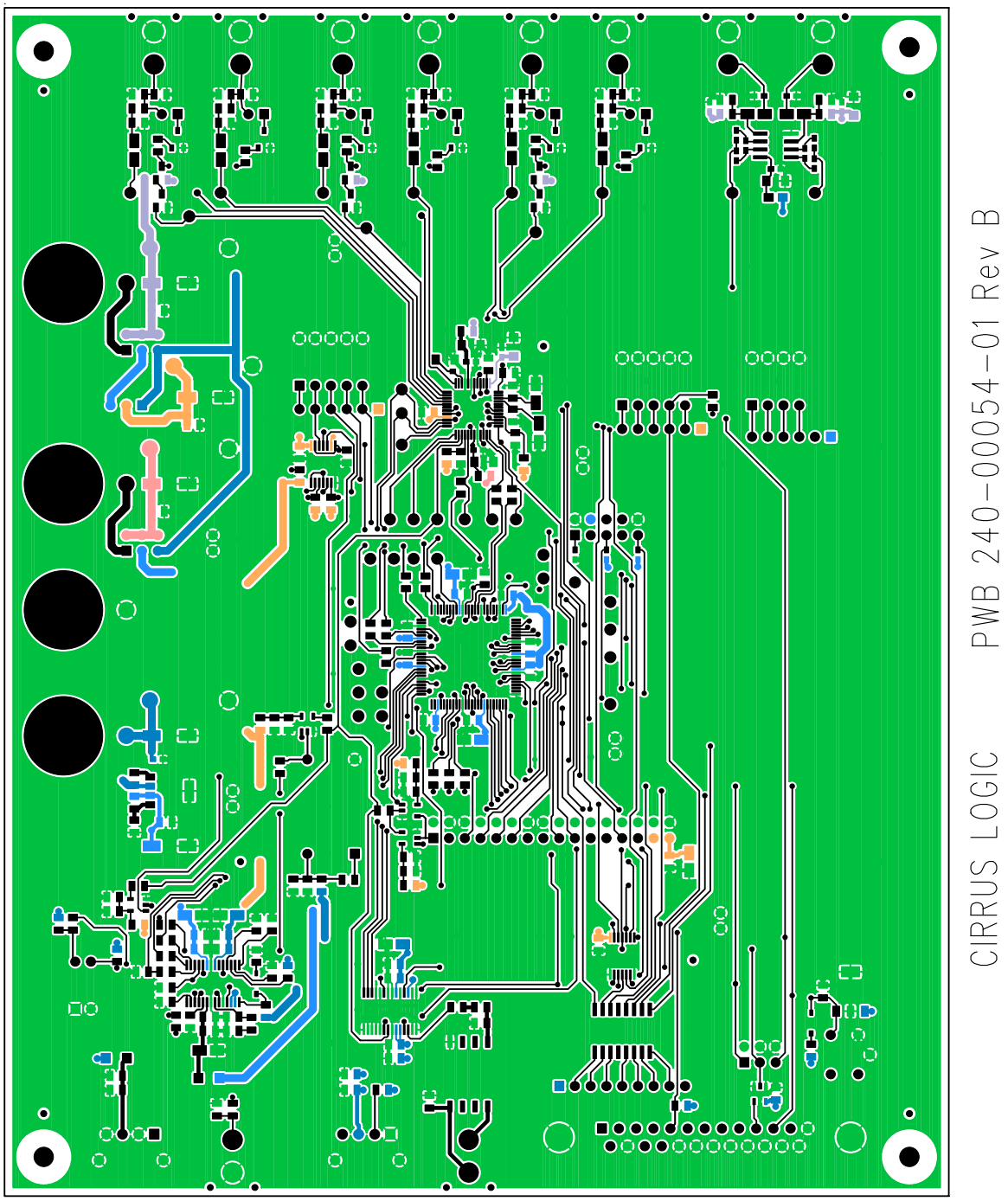

Figure 27. Topside Layer

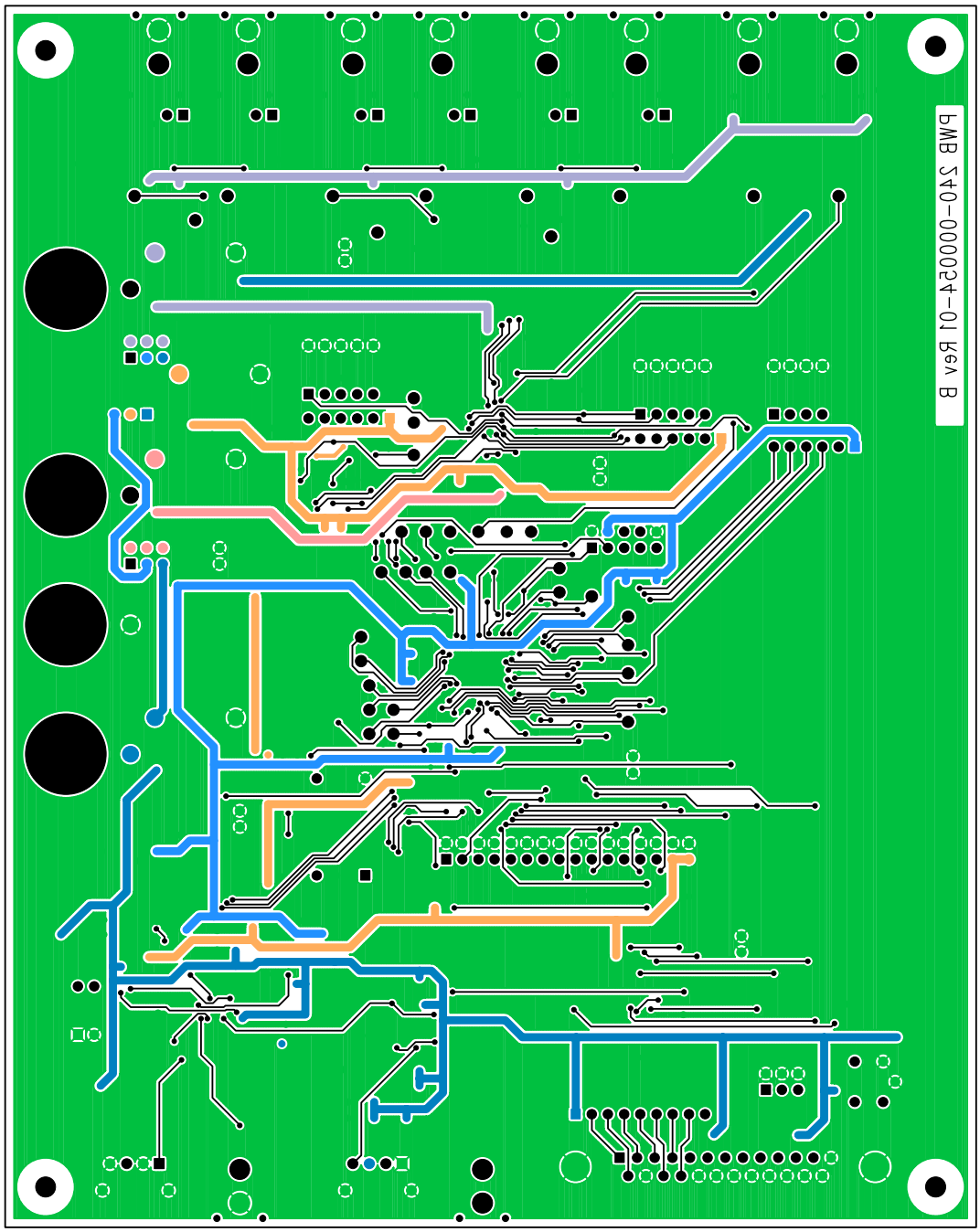

Figure 28. Bottomside Layer