CDB5321

Evaluation Board for CS5321 and CS5322

Features

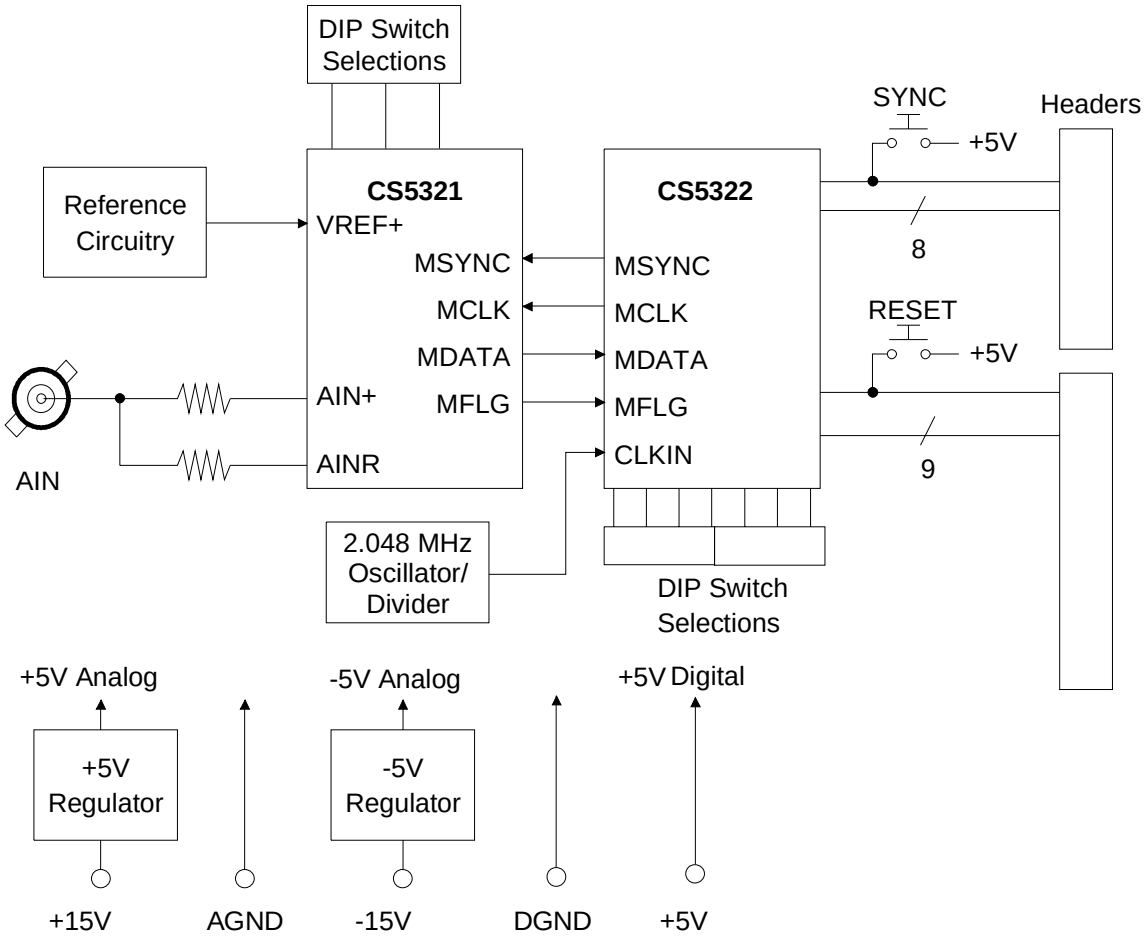
- DIP switch control of all CS5322 logic pins
- Header control of all CS5322 logic pins
- Supports manual operation of RESET and SYNC

Description

The CDB5321 is an evaluation board that allows laboratory characterization of the CS5321/CS5322 A/D converter chip-set. The chip-set supports seven different selectable word rates: 4 kHz, 2 kHz, 1 kHz, 500 Hz 250 Hz, 125 Hz and 62.5 Hz. Input to the board is 9 volts peak-to-peak. Output is via header connections to the CS5322 serial interface.

ORDERING INFORMATION

CDB5321 Evaluation Board



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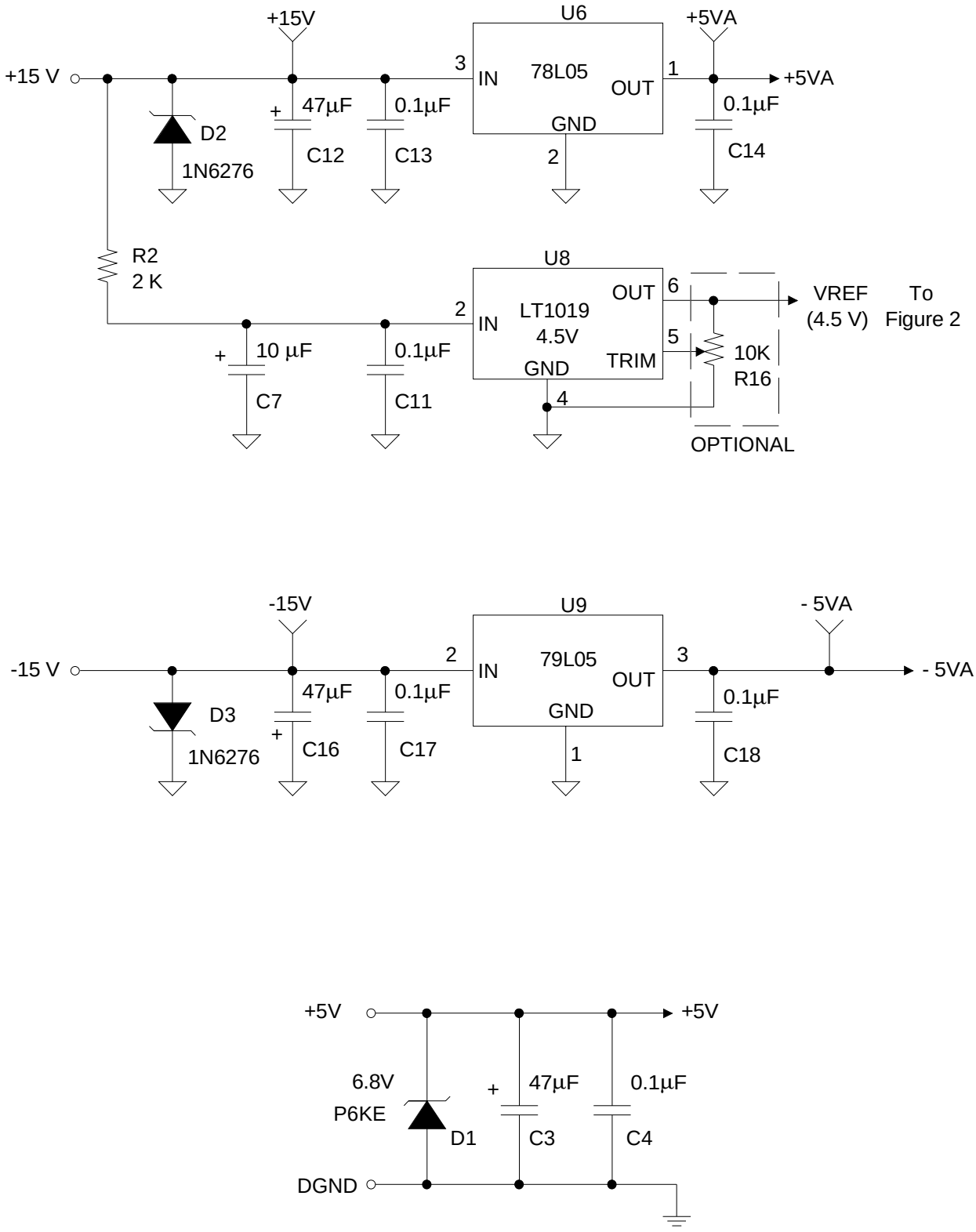

Figure 1. Power Supplies

OVERVIEW

The CDB5321 evaluation board requires three separate power supplies for proper operation. Figure 1 illustrates the power supply connections. The required power supply input voltages consist of +5V, +15V, and -15V. The CS5322 filter and logic support devices on the board operate from the +5V supply. The +15V and -15V inputs are regulated down to provide +5V and -5V supplies necessary for the CS5321 modulator. Figure 1 also illustrates the LT1019 4.5V reference used with the CS5321 modulator.

Figure 2 illustrates the CS5321 modulator circuitry, including the analog BNC input for the test signal source. Most often switch selections on S5 are set to HBR=1, LPWR=0, and

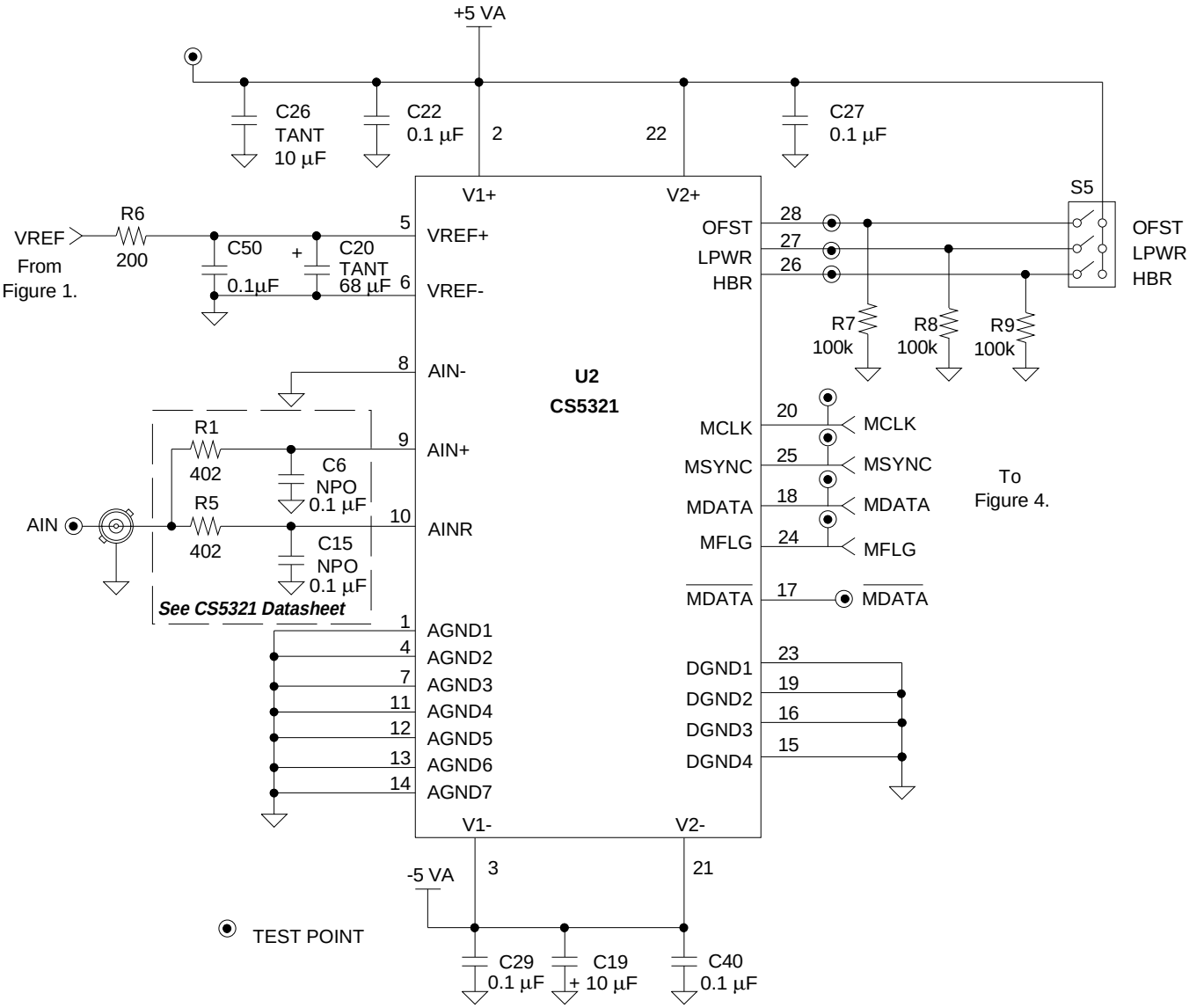

Figure 2. CS5321 Modulator Input Circuitry.

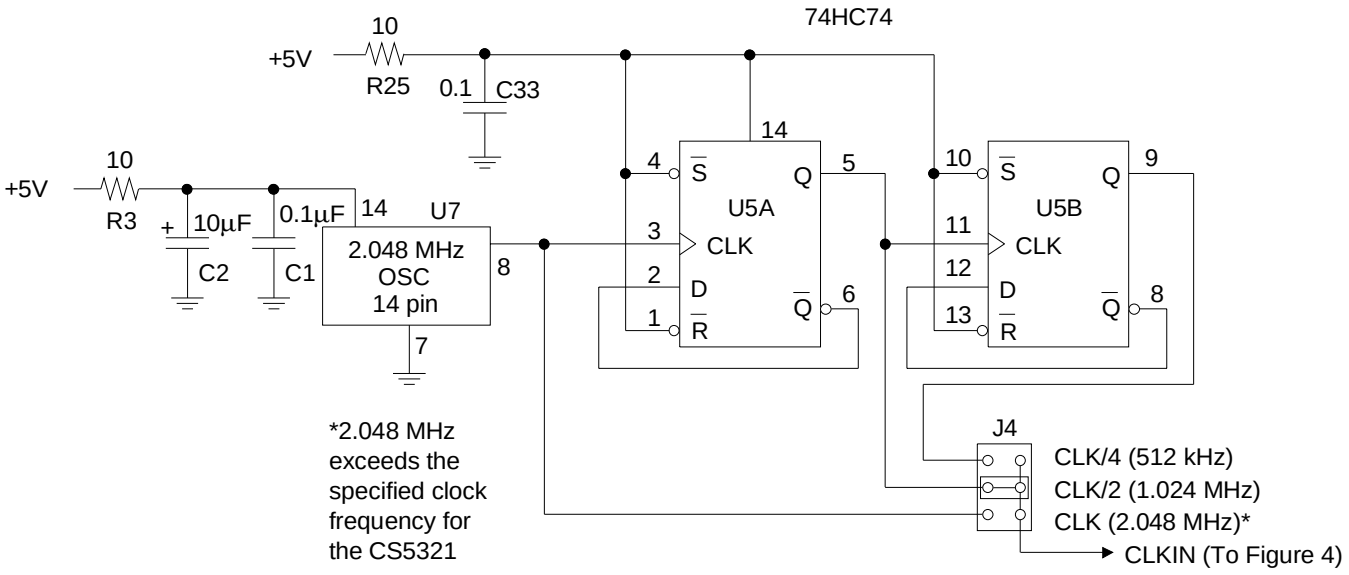

Figure 3. Oscillator / Divider

OFST=1. Figure 3 illustrates the 2.048 MHz oscillator and dual D flip flop clock divider. Note that both the oscillator and the divider are separately decoupled from the +5V supply to reduce clock jitter which can be introduced from noisy supplies. Jumper J4 should be set in the CLK/2 position to source 1.024 MHz to the CS5322 chip for normal operation. If operation from 512 kHz clock is desired, the J4 jumper should be changed to the CLK/4 position. The board can be tested at 512 kHz without modification.

The digital interface pins to the CS5322 filter chip are all available on the header connectors J1, J2, and J3 as shown in Figures 4, 5, and 6. Note that one row of pins on each of the headers is ground. It is advised that any connections made to control lines be done with twisted pair ribbon cable; with each twisted pair containing one signal and one ground connection. This minimizes radiated noise.

CAUTION!

Caution is advised when interfacing the evaluation board to any circuitry powered from another source. For example, when interfacing to a computer I/O card be sure that the evaluation board and the computer are both powered up before connecting to the evaluation board headers. Always disconnect header connections when powering down the board but not the computer. Failure to follow this advice may cause damage to either the computer I/O or to the CS5322, because the computer outputs try to power the CDB5321 board.

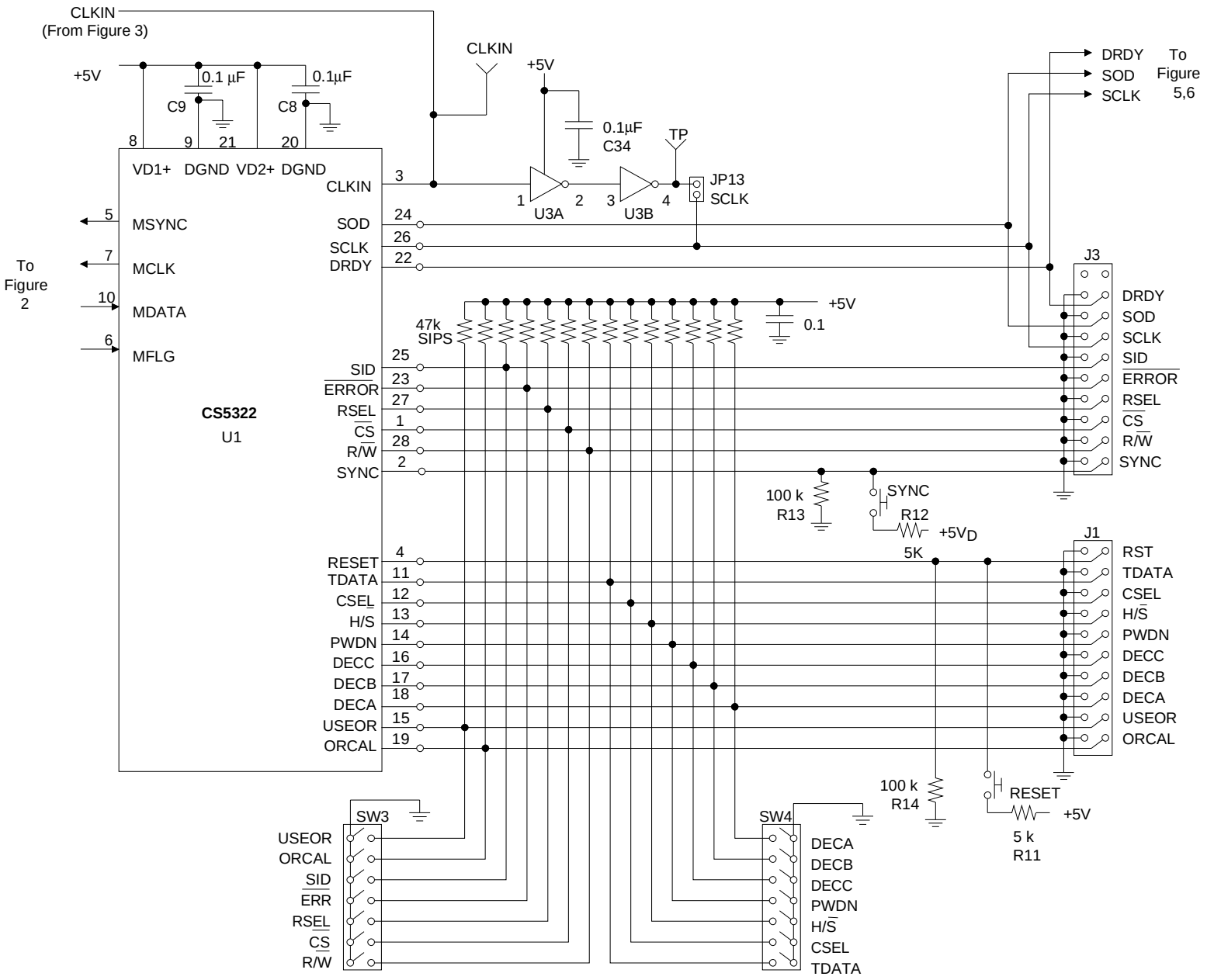

Figure 4. CS5322 Filter Interface

USEOR	ON*	Do not use offset register
	OFF	Use offset register
ORCAL	ON*	Disable offset register calibration
	OFF	Enable offset register calibration
SID	ON	Sets SID to Logic 0
	OFF*	Allows pull-up on SID line
ERR	ON	Sets ERR to logic 0
	OFF*	Allows CS5322 ERROR output
RSEL	ON	Select status register
	OFF*	Select conversion data register
CS	ON*	Chip select active
	OFF	Chip select inactive
R/$\overline{W}$	ON	Enables write mode via SID pin
	OFF*	Enables read mode via SOD pin

OFF = OPEN = 1

*Default to use Figure 6 interface.

Table 1. S3 DIP Switch Selections

DECA	Selection via hardware pins	ABC	Output Word Rate
		0 0 0	62.5
DECB		1 0 0	125
		0 1 0	250
		1 1 0	500
DECC		0 0 1	1000
		1 0 1	2000
		0 1 1	4000
PWDN	ON*	Normal Operation	
	OFF	Power down active	
H/$\overline{S}$	ON	Selects configuration register for operating mode	
	OFF*	Select hardware pins for operating mode	
CSEL	ON*	Selects MDATA from modulator	
	OFF	Selects TDATA as filter input	
TDATA	ON*	Sets TDATA input to logic 0	
	OFF	Enables TDATA from J1 header	

OFF = OPEN = 1

*Default to use Figure 6 interface.

Table 2. S4 DIP switch selections

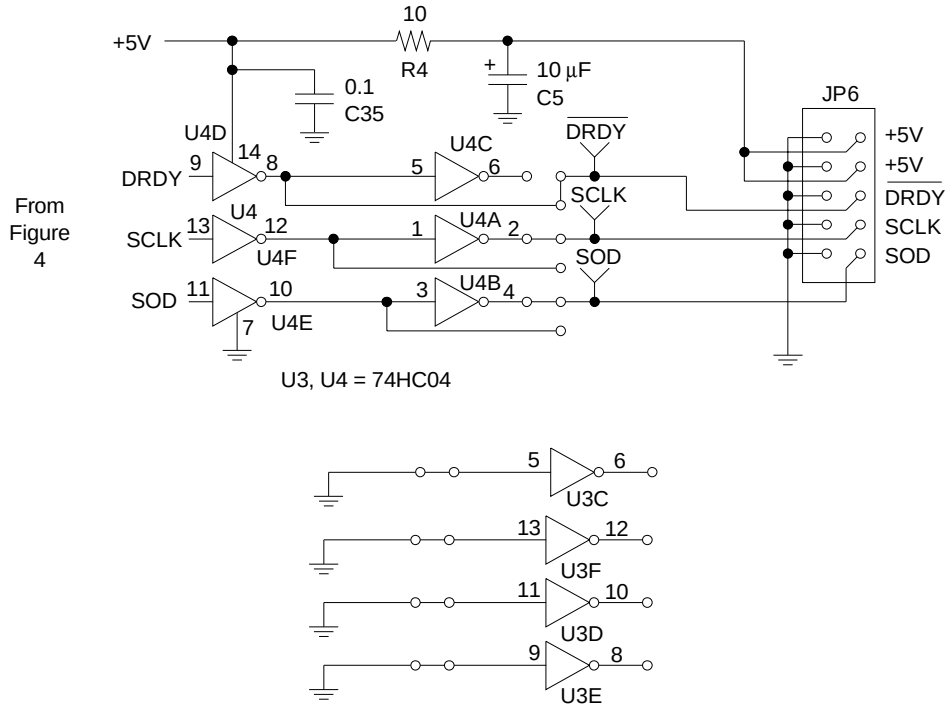

Figure 5. Serial Latch Interface on CDB5321 (Rev B) board

Figures 5 and 6 illustrate the logic used to drive connections at header JP6 (Rev. B Board) or J2 (Rev. C Board).

The Rev. C evaluation board can directly interface to the CDBCAPTURE board through connector J2. A D-type Flip-Flop must be added in the patch area of the Rev. B evaluation board to enable it to interface to the CDBCAPTURE board. The CDBCAPTURE can be used to perform FFT analysis and noise histograms.

Tables 1 and 2 illustrate the DIP switch positions of switches S3 and S4. The switch positions with asterisks indicate preferred settings for driving the interface on the CDBCAPTURE system.

The CS5322 filter should be set up for hardware mode (H/$\overline{S}$ on switch S4 open). DIP switch S4 can then be used to select the desired output word rate. After the selection on the DECA, DECB, and DECC positions of the S4 DIP switch, the S2 RESET switch must be activated, followed by the S1 SYNC switch (unless these signals are controlled via the J1 and J3 header signals).

Figure 7 illustrates the component layout of the board while figures 8 and 9 illustrate the board layout (not to scale).

Using the Evaluation Board

Connect the appropriate power supplies to the binding posts of the board. Twist the +5V digital supply lead with the digital ground lead from the board to the supply. Also twist the supply leads for the analog voltages. Use a high quality power supply which is low in noise and line frequency(50/60 Hz) interference.

Power up the supplies. Then connect a coaxial cable from the analog BNC to the signal source. Note that the performance of the A/D converter chip set will exceed the capability of most signal generators, with respect to noise, distortion, and line frequency interference.

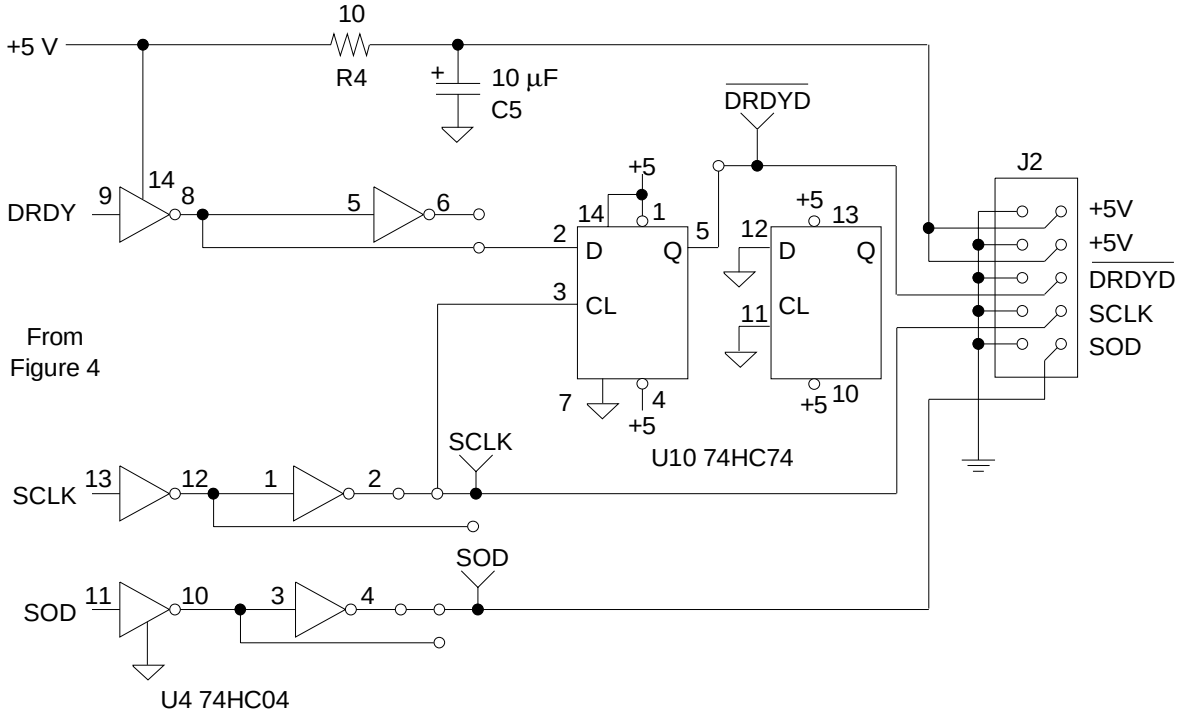

Figure 6. Serial Latch Interface on CDB5321 (Rev C) board.

Once power has been applied to the board, connect the ribbon cable to the appropriate headers (J1, J2, and/or J3). The reset and the sync signals to the CS5322 must be applied before normal operation can commence. This can be done by using the S2 RESET switch and the S1 SYNC switch or by interfacing to these signals via the J1 and J3 headers.

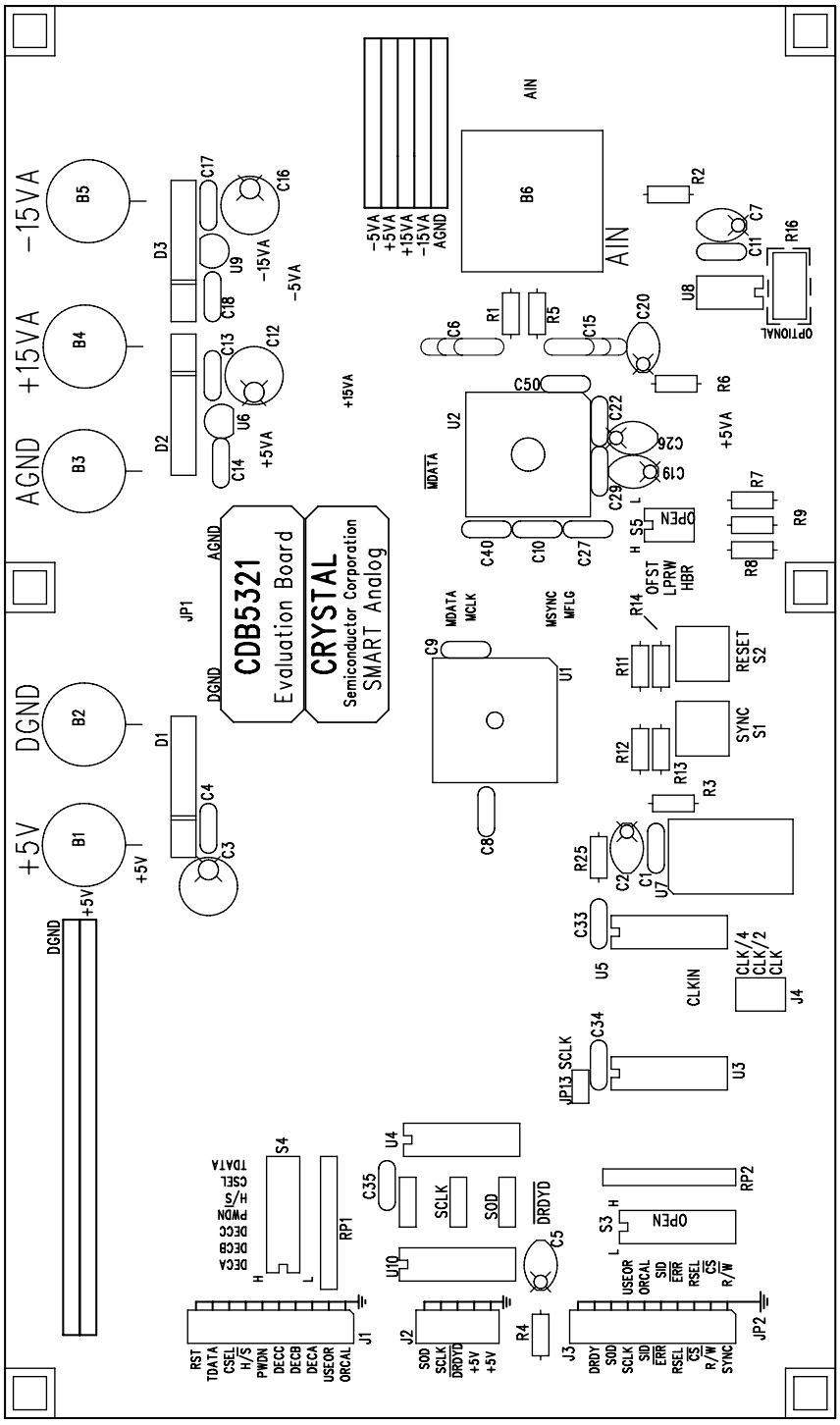

Figure 7. CDB5321 (Rev. C) Silk Screen Layout (Not to Scale)

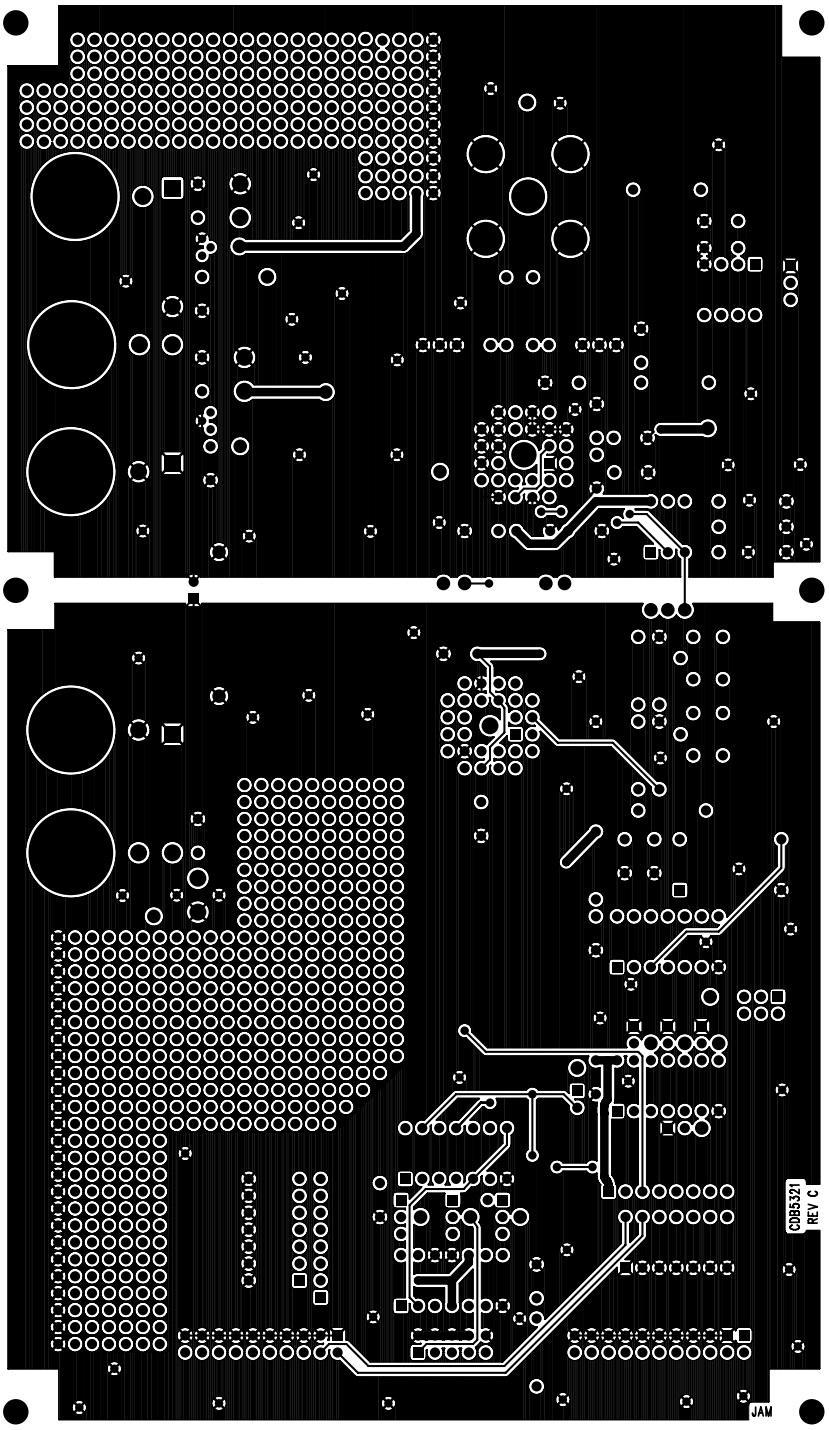

Figure 8. CDB5321 (Rev. C) Component Side Layer (Not to Scale)

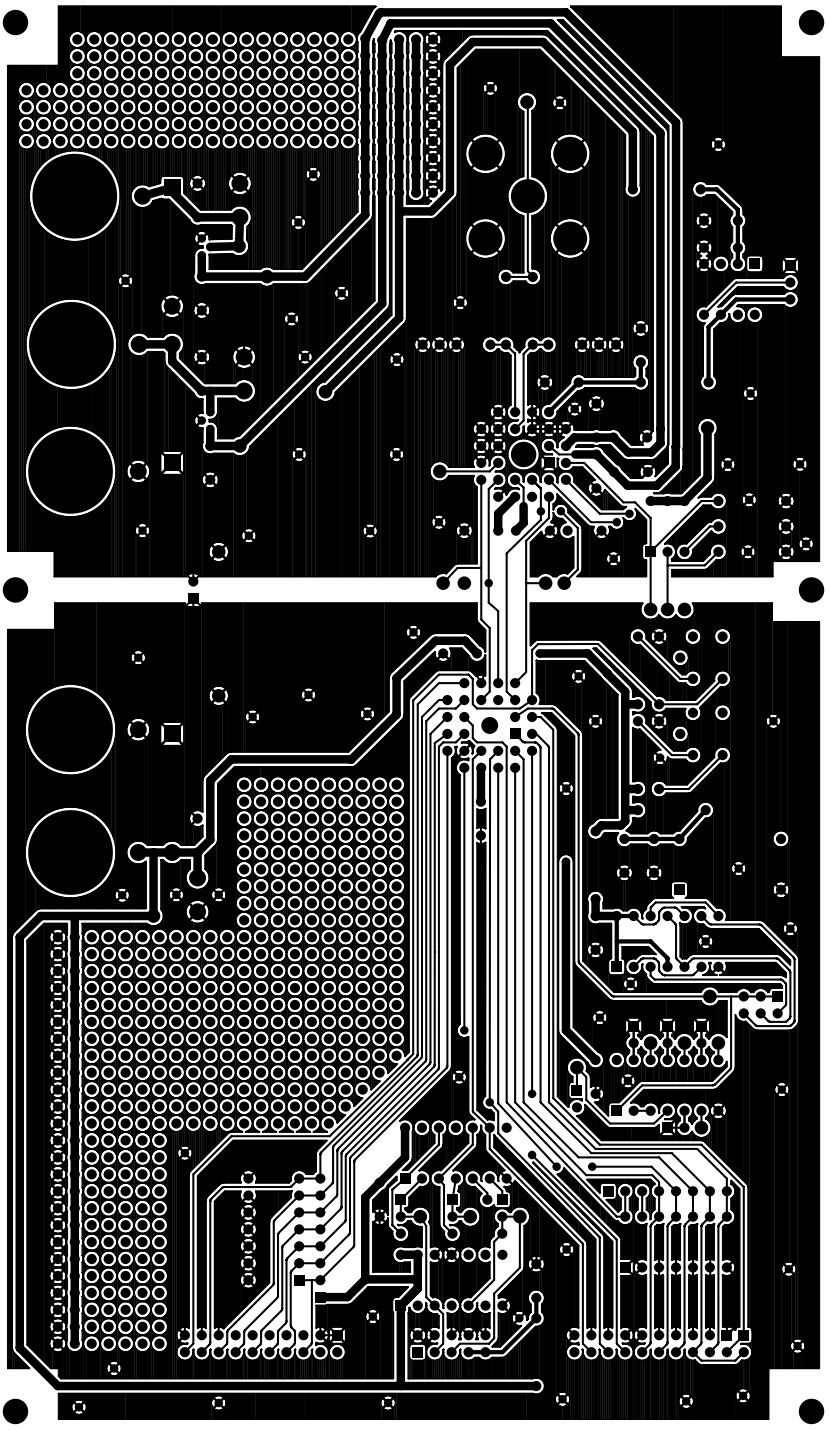

Figure 9. CDB5321 (Rev. C) Solder Side Layer (Not to Scale)


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