

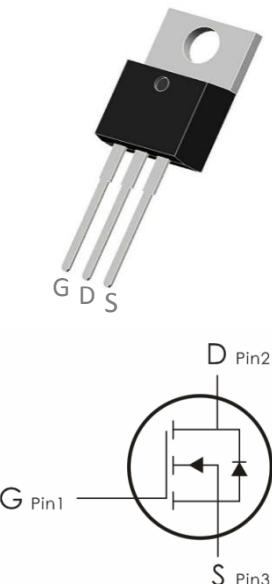
Description:

This N-Channel MOSFET uses advanced trench technology and design to provide excellent $R_{DS(on)}$ with low gate charge.

It can be used in a wide variety of applications.

Features:

- 1) $V_{DS}=30V, I_D=180A, R_{DS(ON)} \leq 3m\Omega @ V_{GS}=10V$
- 2) Low gate charge.
- 3) Green device available.
- 4) Advanced high cell density trench technology for ultra $R_{DS(ON)}$.
- 5) Excellent package for good heat dissipation.



Absolute Maximum Ratings: ($T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Ratings	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current ¹	180	A
	Continuous Drain Current- $T_C=100^\circ C$	127	
	Pulsed Drain Current ¹	720	
E_{AS}	Single Pulse Avalanche Energy ³	439	mJ
P_D	Power Dissipation ⁴	115	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +175	$^\circ C$

Thermal Characteristics:

Symbol	Parameter	Max	Units
R_{eJC}	Thermal Resistance,Junction to Case ¹	1.3	$^\circ C/W$
R_{eJA}	Thermal Resistance,Junction to Ambient ¹	62.5	

Electrical Characteristics: ($T_c=25^\circ\text{C}$ unless otherwise noted)

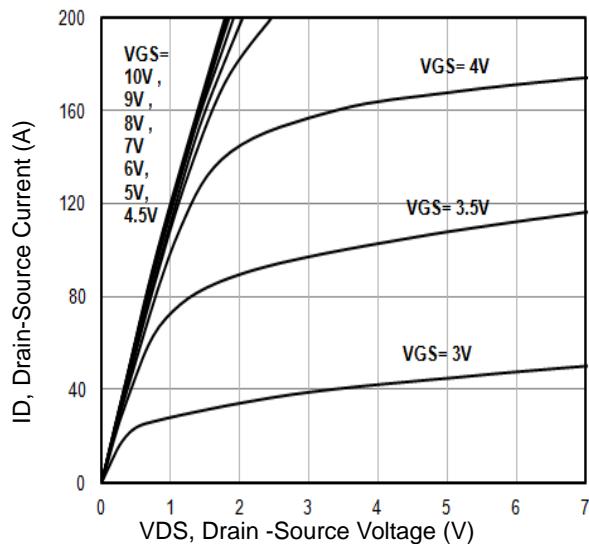
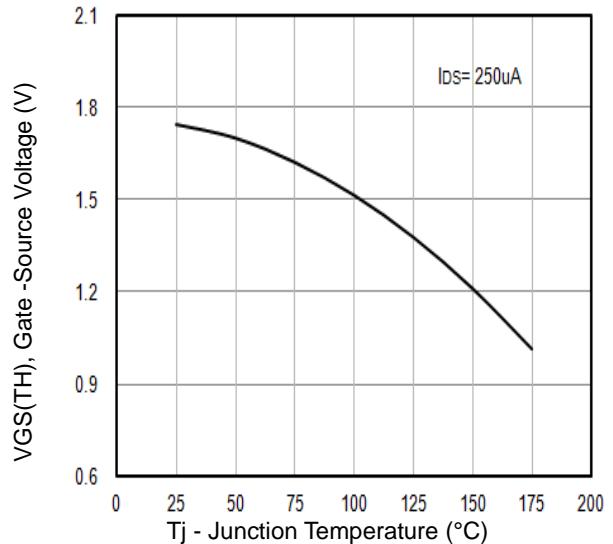
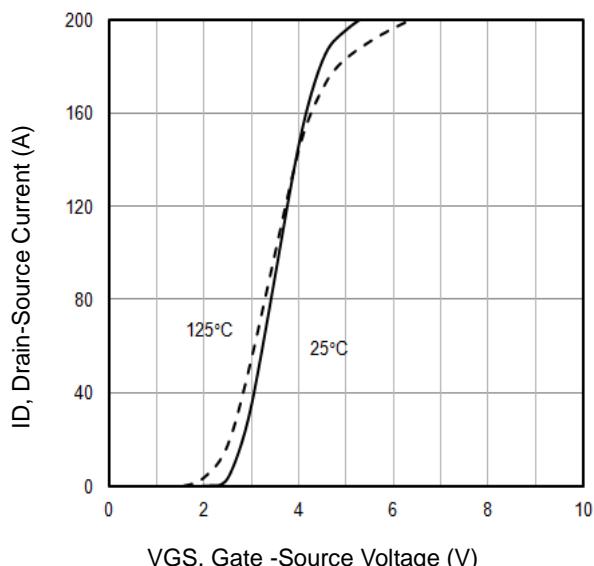
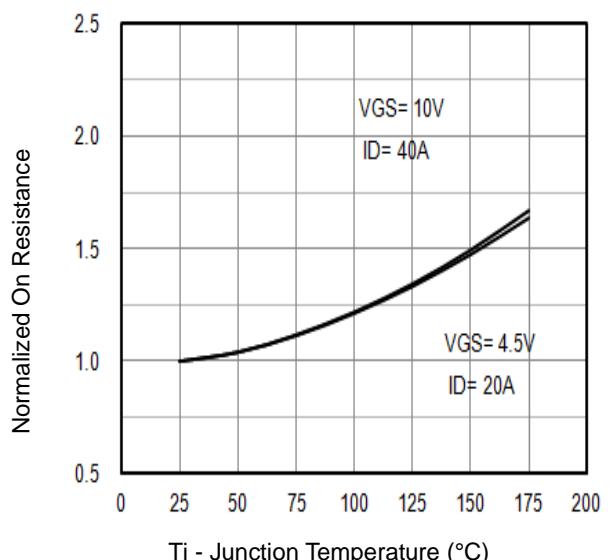
Symbol	Parameter	Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}, I_D=250\ \mu\text{A}$	30	---	---	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=30\text{V}$	---	---	1	μA
I_{GSS}	Gate-Source Leakage Current	$V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{A}$	---	---	± 100	nA
On Characteristics						
$V_{\text{GS}(\text{th})}$	GATE-Source Threshold Voltage	$V_{\text{GS}}=V_{\text{DS}}, I_D=250\ \mu\text{A}$	1.3	1.8	2.4	V
$R_{\text{DS}(\text{ON})}$	Drain-Source On Resistance ²	$V_{\text{GS}}=10\text{V}, I_D=40\text{A}$	---	2.1	3	$\text{m}\ \Omega$
		$V_{\text{GS}}=4.5\text{V}, I_D=20\text{A}$	---	2.8	4	
G_{FS}	Forward Transconductance	$V_{\text{DS}=0\text{V}}, I_D=0\text{A}$	---	---	---	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{\text{DS}}=15\text{V}, V_{\text{GS}}=0\text{V}, f=1\text{MHz}$	3500	4565	5500	pF
C_{oss}	Output Capacitance		570	785	1000	
C_{rss}	Reverse Transfer Capacitance		500	710	900	
Switching Characteristics						
$t_{\text{d(on)}}$	Turn-On Delay Time	$V_{\text{DD}}=15\text{V}, I_D=40\text{A}, R_{\text{GEN}}=3\ \Omega, V_{\text{GS}}=10\text{V}$	---	12	---	ns
t_r	Rise Time		---	8.5	---	ns
$t_{\text{d(off)}}$	Turn-Off Delay Time		---	77.5	---	ns
t_f	Fall Time		---	19.5	---	ns
Q_g	Total Gate Charge	$V_{\text{GS}}=10\text{V}, V_{\text{DS}}=15\text{V}, I_D=40\text{A}$	---	73	---	nC
Q_{gs}	Gate-Source Charge		---	12	---	nC
Q_{gd}	Gate-Drain "Miller" Charge		---	18	---	nC
Drain-Source Diode Characteristics						
V_{SD}	Source-Drain Diode Forward Voltage ²	$V_{\text{GS}}=0\text{V}, I_S=40\text{A}$	---	0.8	-1.2	V

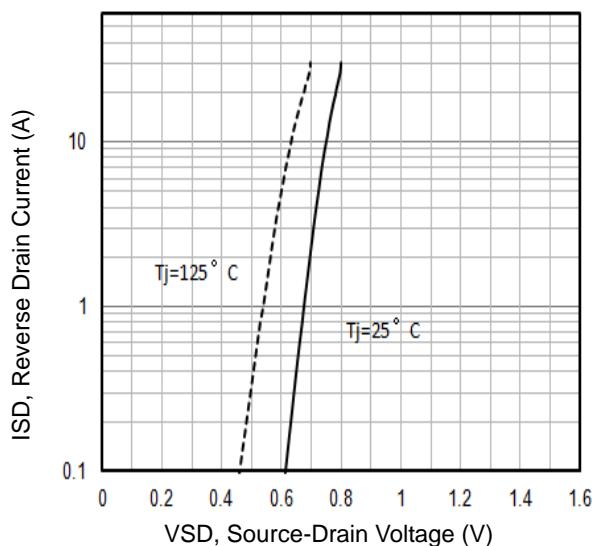
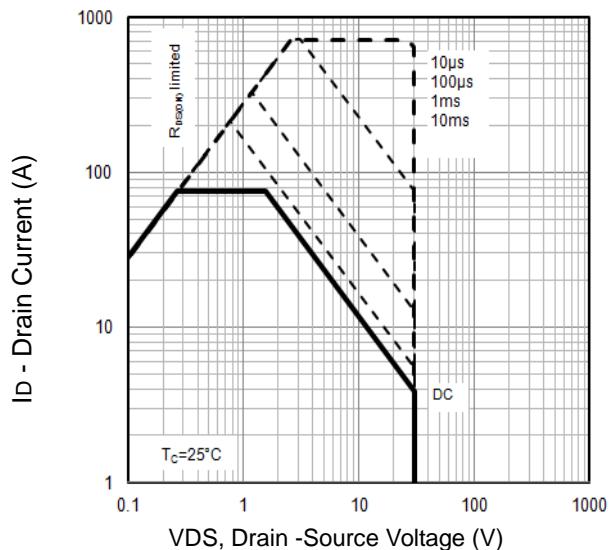
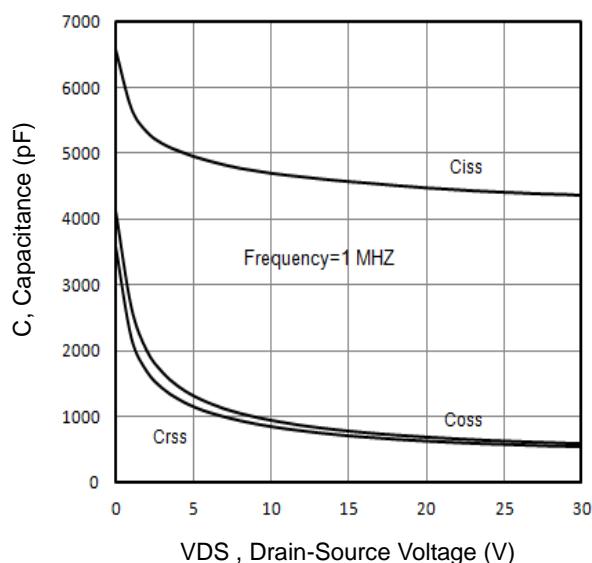
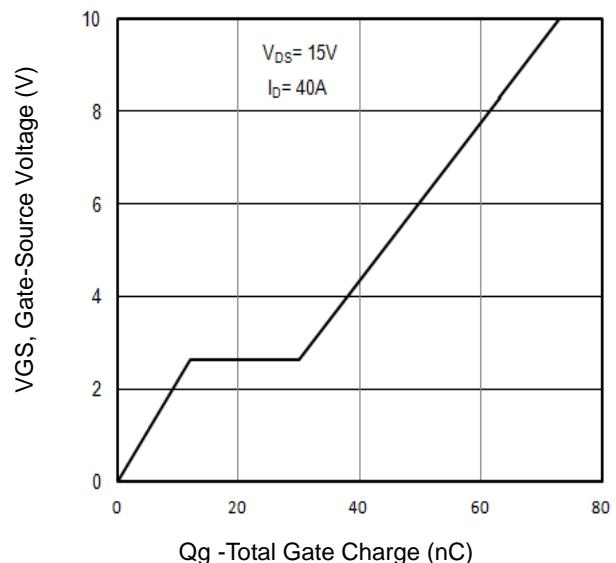
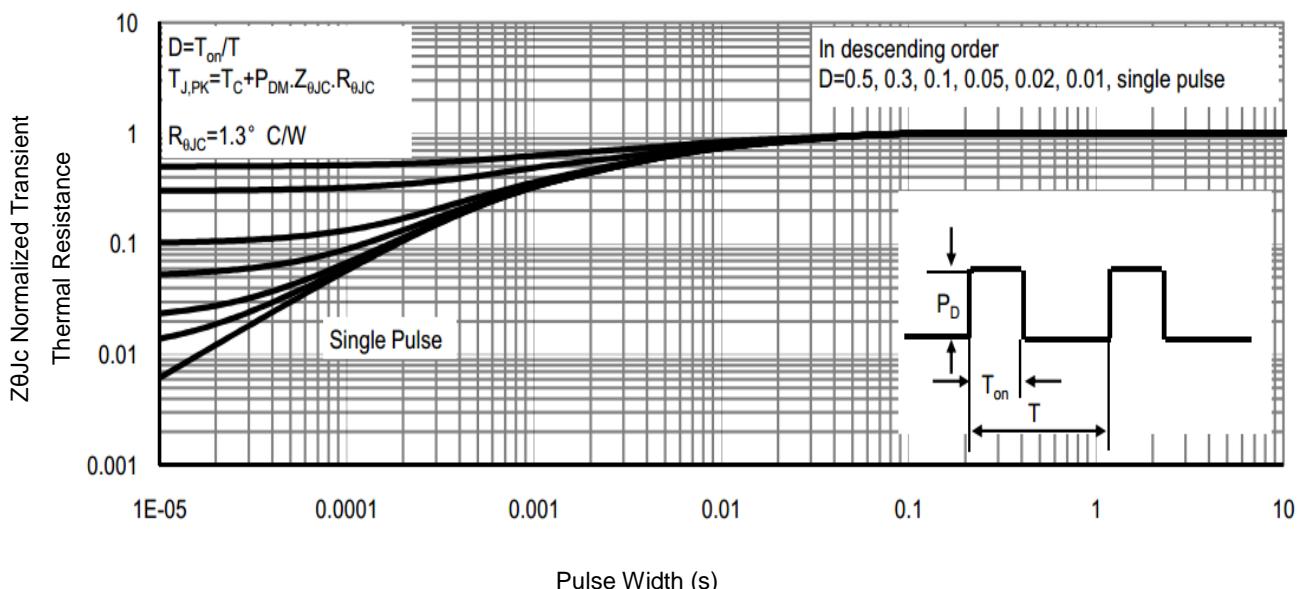


Ls	Diode Forward Current (Note 2)	---	---	---	---	A
Trr	Reverse Recovery Time	$T_j=25^\circ\text{C}$, $I_{sd}=40\text{A}$, $V_{GS}=0\text{V}$ $di/dt=500\text{A}/\mu\text{s}$	---	31	---	NS
Qrr	Reverse Recovery Charge		---	15.5	---	NC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production.

Typical Characteristics: ($T_c=25^\circ\text{C}$ unless otherwise noted)**Fig1.** Typical Output Characteristics**Fig2.** $V_{GS(TH)}$ Gate -Source Voltage Vs. T_j **Fig3.** Typical Transfer Characteristics**Fig4.** Normalized On-Resistance Vs. Temperature

**Fig5.** Typical Source-Drain Diode Forward Voltage**Fig6.** Maximum Safe Operating Area**Fig7.** Typical Capacitance Vs.Drain-Source Voltage**Fig8.** Typical Gate Charge Vs.Gate-Source Voltage**Fig9 .** Normalized Maximum Transient Thermal Impedance

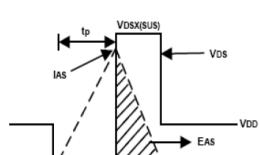
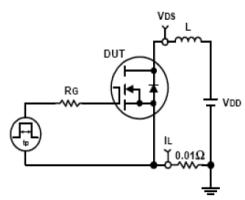


Fig10. Unclamped Inductive Test Circuit and waveforms

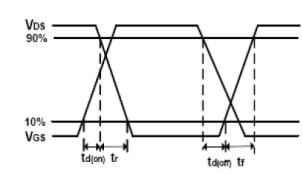
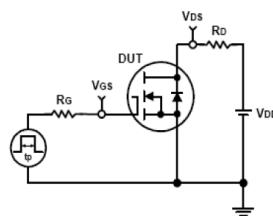


Fig11. Switching Time Test Circuit and waveforms



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