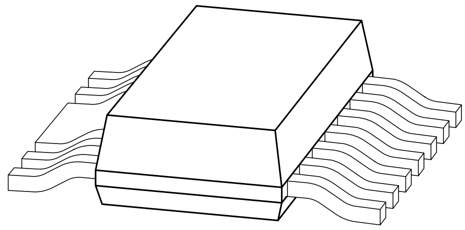
GaAs MMIC

CGY 180

Data Sheet

- Power amplifier for DECT, PHS, WLL applications
- Fully integrated 3 stage amplifier
- Operating voltage range: 2.7 to 6 V
- Overall power added efficiency 35%
- Easy external matching

ESD: **E**lectro**s**tatic **d**ischarge sensitive device, observe handling precautions!



Type	Marking	Ordering Code (taped)	Package[1)]
CGY 180	CGY 180	Q68000-A8882	MW-12

1) Plastic body identical to P-SOT-223, dimensions see **Page 17**.

Maximum Ratings	Symbol	Value	Unit
Positive supply voltage	V_D	8	V
Negative supply voltage[1)]	V_G	– 8	V
Supply current	I_D	1.2	A
Maximum input power	$P_{in,max}$	10	dBm
Channel temperature	T_{Ch}	150	°C
Storage temperature	T_{stg}	– 55 … + 150	°C
Total power dissipation ($T_s \leq 81$ °C) T_s: Temperature at soldering point	P_{tot}	2.3	W
Pulse peak power	P_{Pulse}	6.0	W

1) V_G = – 8 V only in combination with V_{TR} = 0 V; V_G = – 6 V while $V_{TR} \neq 0$ V

Thermal Resistance	Symbol	Value	Unit
Channel-soldering point	R_{thChS}	≤ 30	K/W

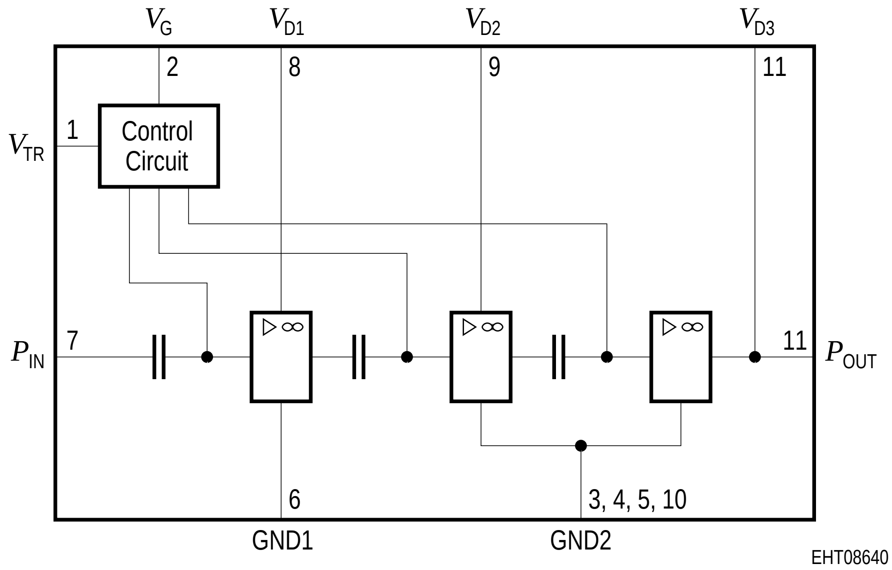


Figure 1 Functional Block Diagram

Pin #	Symbol	Configuration
1	VTR	Control voltage for transmit (0 V)/receive (open) mode
2	VG	Negative voltage at control circuit (– 4 V … – 8 V)
3	GND2	RF and DC ground of the 2nd and 3rd stage
4	GND2	RF and DC ground of the 2nd and 3rd stage
5	GND2	RF and DC ground of the 2nd and 3rd stage
6	GND1	RF and DC ground of the 1st stage
7	RFin	RF input power
8	VD1	Pos. drain voltage of the 1st stage
9	VD2	Pos. drain voltage of the 2nd stage
10	GND2	RF and DC ground of the 2nd and 3rd stage
11	VD3, Pout	Pos. drain voltage of the 3rd stage, RF output power
12	n.c.	–

Control Circuit

VG supply: Negative voltage (stabilization is not necessary) in the range of
– 4 V … – 8 V.

VTR supply:

During transmit operation: 0 V, negative supply current 1 mA … 2.5 mA.

During receive operation: not connected (shut off mode)

The operation current ID of CGY 180 is adjusted by the internal control circuit.

DC Characteristics

Characteristics	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Drain current stage 1	I_{DSS1}	150	220	320	mA	V_D = 3 V, V_G = 0 V, V_{TR} n.c.
stage 2	I_{DSS2}	150	220	320	mA	
stage 3	I_{DSS3}	675	1000	1440	mA	
Drain current with active current control	I_D	260	450	620	mA	V_D = 3 V, V_G = – 4 V, V_{TR} = 0 V
Transconductance (stage 1 - 3)	G_{fs1}	70	100	140	mS	V_D = 3 V, I_D = 90 mA
	G_{fs2}	70	100	140	mS	V_D = 3 V, I_D = 90 mA
	G_{fs3}	350	500	630	mS	V_D = 3 V, I_D = 400 mA
Pinch off voltage	V_p	– 3.8	– 2.8	– 1.8	V	V_D = 3 V, I_D < 170 µA (all stages)

Electrical Characteristics

T_A = 25 °C, f = 1.89 GHz, Z_S = Z_L = 50 Ω, V_D = 3 V, V_g = – 4 V, VTR pin connected to ground; unless otherwise specified

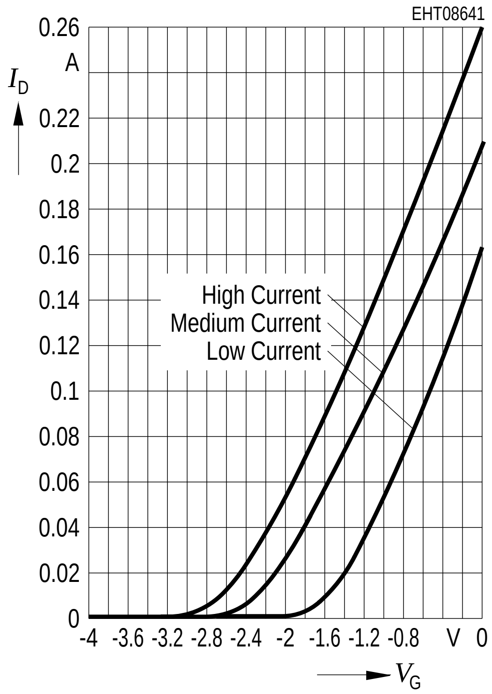
Characteristics	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Supply current	I_{DD}	–	450	–	mA	P_{in} = 0 dBm
Negative supply current (transmit operation)	I_G	–	1	2.5	mA	–
Shut-off current	I_D	–	50	180	µA	VTR n.c.
Negative supply current	I_G	–	10	50	µA	shut off mode, VTR pin n.c.
Gain	G	28	30	–	dB	P_{in} = – 20 dBm
Output Power	P_o	25.5	27	–	dBm	P_{in} = 0 dBm
Output Power	P_o	–	30	–	dBm	V_D = 5 V; P_{in} = 0 dBm
Overall Power added Efficiency	η	30	35	–	%	P_{in} = 0 dBm
Harmonics 2 f_0 3 f_0	– –	– –	– –	– 28 – 25	dBc	P_{in} = 0 dBm, V_D = 3 V P_{out} = 27 dBm
Harmonics 2 f_0 3 f_0	– –	– –	– –	– 25 – 22	dBc	P_{in} = 0 dBm, V_D = 5 V, P_{out} = 30 dBm
Input VSWR	–	–	2:1	2.5:1	–	V_D = 3 V
Third order intercept point	IP_3	–	33.5	–	dBm	V_D = 3 V; pulsed with a duty cycle of 10%; f_1 = 1.8900 GHz; f_2 = 1.891728 GHz
Third order intercept point	IP_3	–	38.5	–	dBm	V_D = 4.8 V; pulsed with a duty cycle of 10%; f_1 = 1.8900 GHz; f_2 = 1.891728 GHz

Electrical Characteristics (cont'd)
T_A = 25 °C, f = 1.89 GHz, Z_S = Z_L = 50 Ω, V_D = 3 V, V_g = – 4 V, VTR pin connected to ground; unless otherwise specified

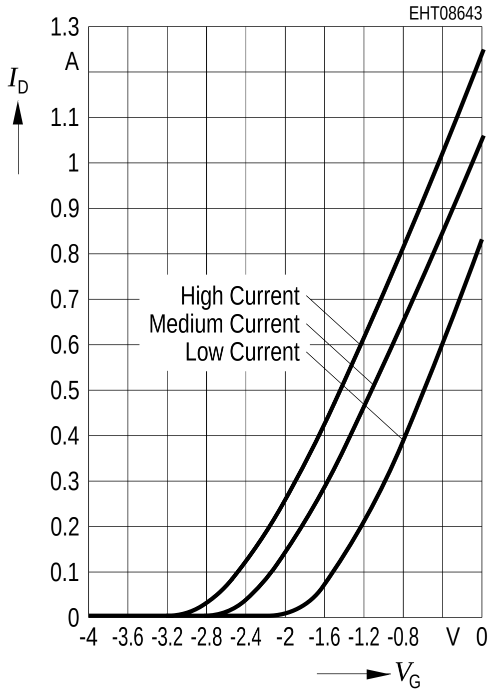
Characteristics	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Load mismatch	–	No module damage for 10 s			–	P_{in} = 0 dBm, $V_D \leq$ 6 V, Z_S = 50 Ω, Load VSWR = 20:1 for all phase, V_{TR} = 0 V, V_G = – 4 V
Stability	–	All spurious output more than 60 dB below desired signal level			–	P_{in} = 0 dBm, V_D = 2 - 7 V, Z_S = 50 Ω, Load VSWR = 3:1 for all phase, V_{TR} = 0 V, V_G = – 4 V

DC - Characteristics

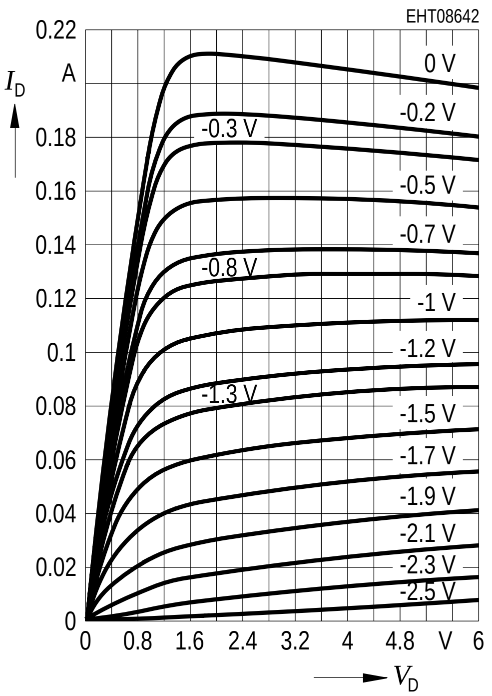
Input Characteristics - Typical Measured Values of Stage 1 and 2, V_{D1} or V_{D2} = 3 V



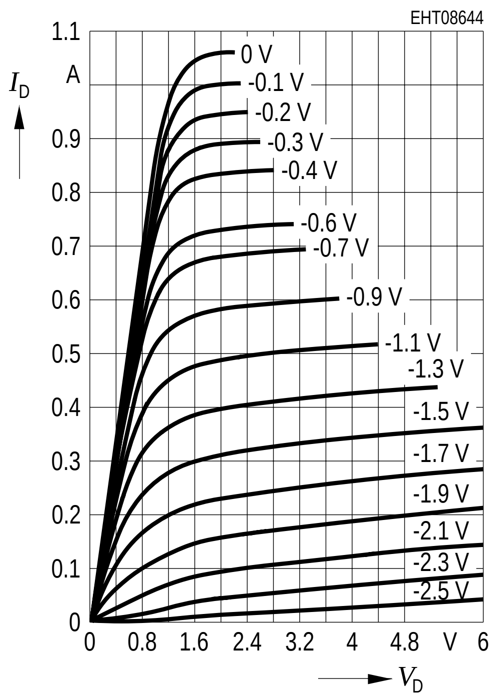
Input Characteristics - Typical Measured Values of Stage 3, V_{D3} = 3 V



Output Characteristics - Typical Measured Values of Stage 1 and 2

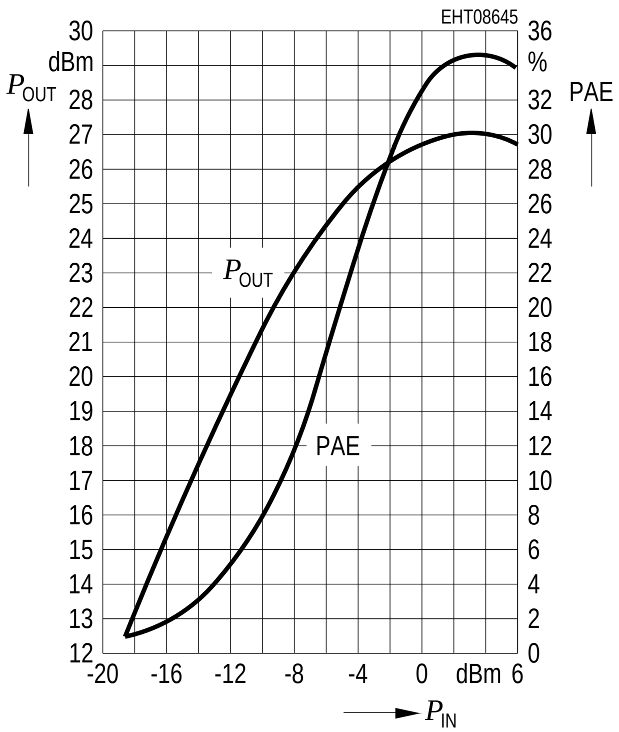


Output Characteristics - Typical Measured Values of Stage 3

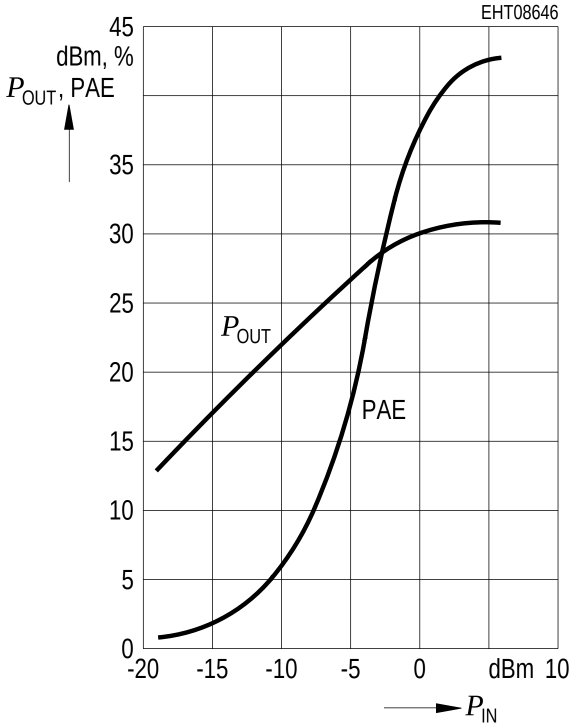


Output Power and Power Added Efficiency

P_{out} and PAE vs. P_{in}, f = 1.89 GHz, V_D = 3 V, V_G = – 4 V, V_{TR} = 0 V

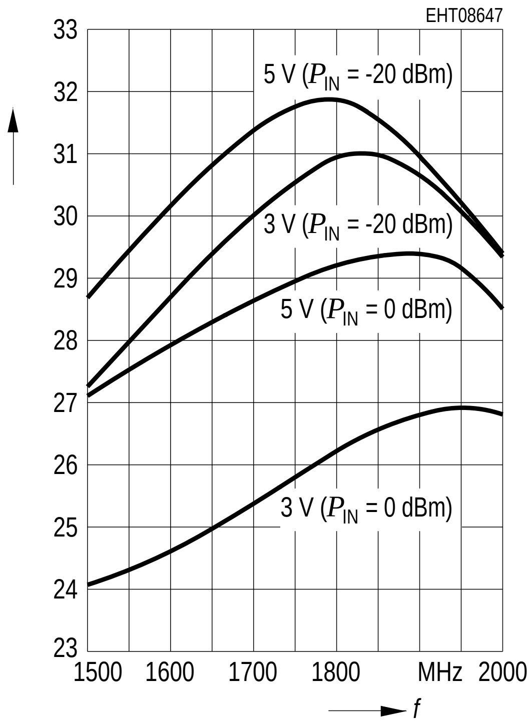


P_{out} and PAE vs. P_{in}, f = 1.89 GHz, V_D = 3 V, V_G = – 4 V, V_{TR} = 0 V

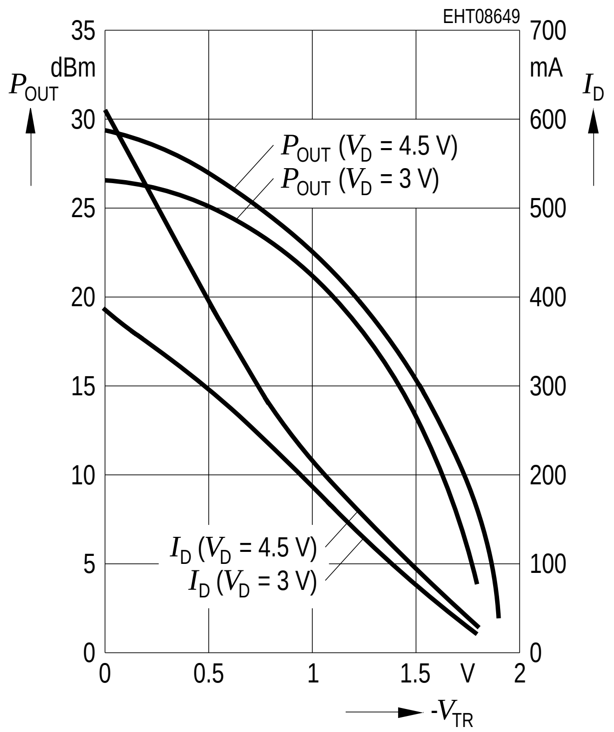


pulsed mode: t_{on} = 1 ms, duty cycle 10%

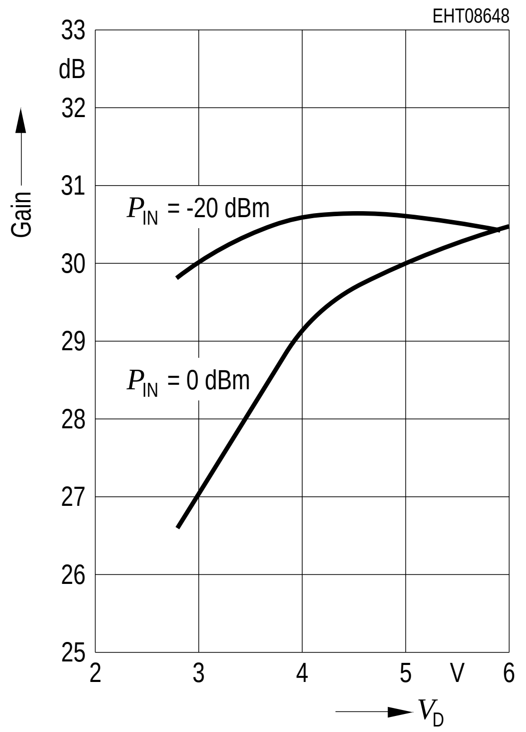
Gain vs. Frequency
(V_G = – 4 V, V_{TR} = 0 V)



Output Power Control vs. V_{TR}

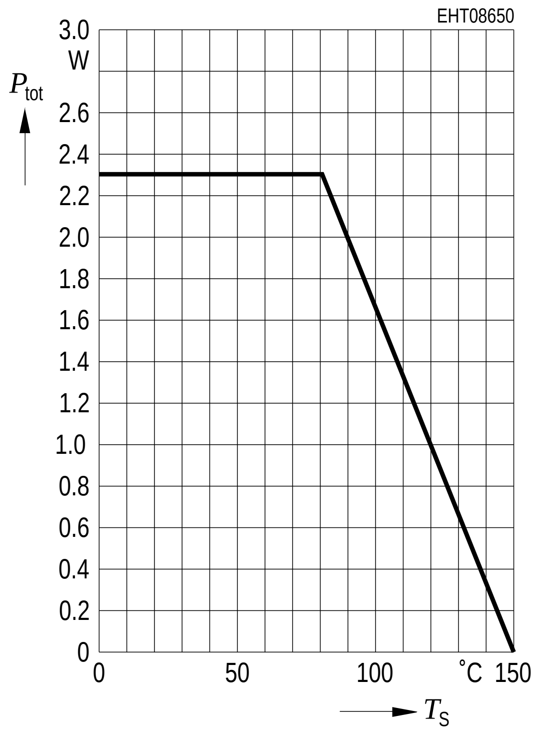


Gain vs. Drain Voltage, f = 1.89 GHz,
V_D = 3 V, V_G = – 4 V, V_{TR} = 0 V



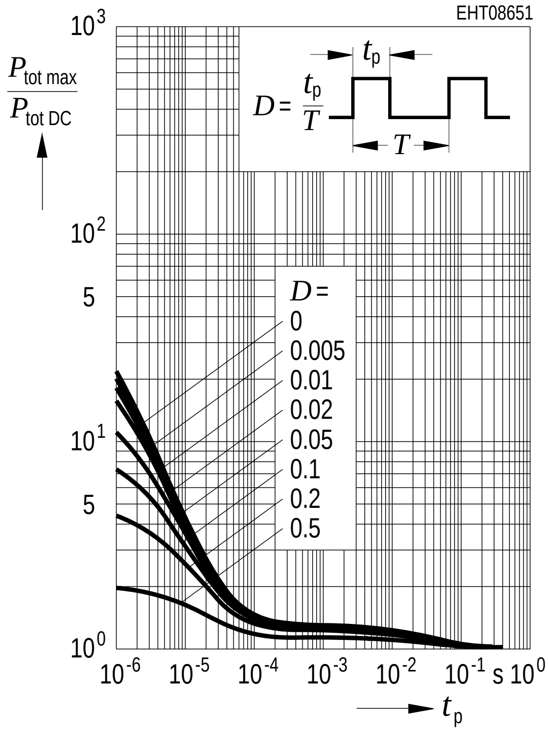
Total Power Dissipation

$P_{tot} = f(T_S)$



Permissible Pulse Load

$P_{tot\_max}/P_{tot\_DC} = f(t_{\_p})$



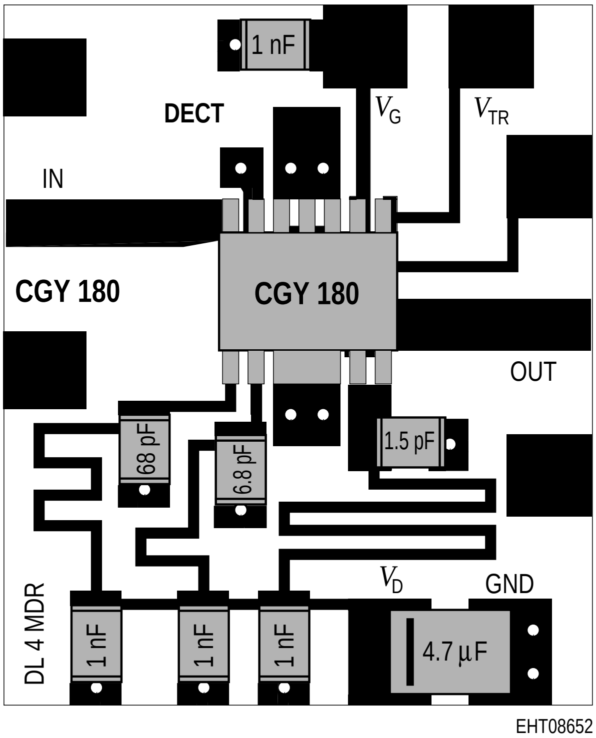


Figure 2 Test Circuit Board

Size: 20 × 25 mm; In, Out: 50 Ω

The Following Impedances of the Bias Circuit Should be Seen from the CGY 180 Ports (values measured at *f* = 1.89 GHz)

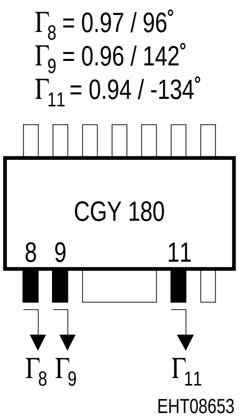


Figure 3

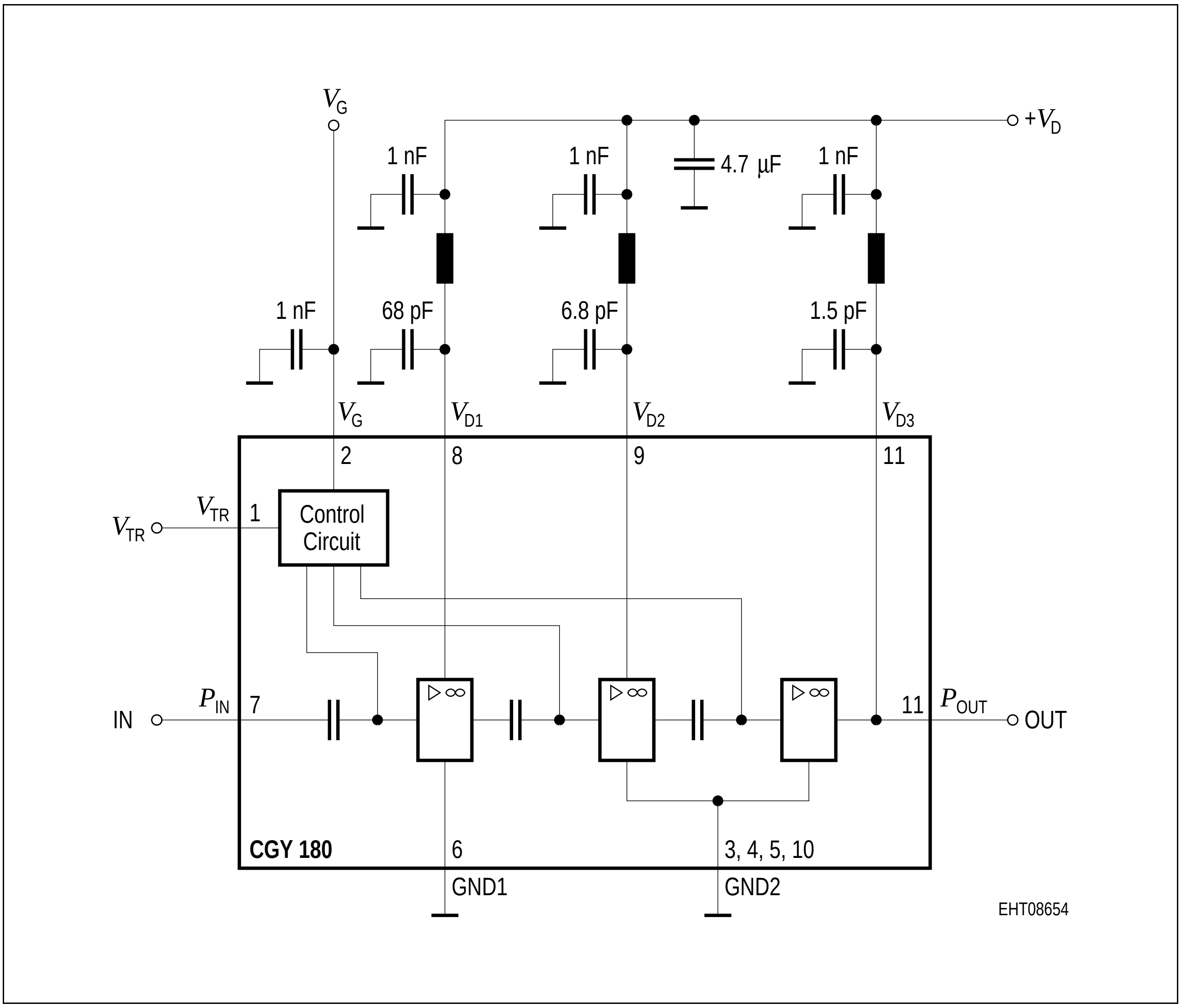
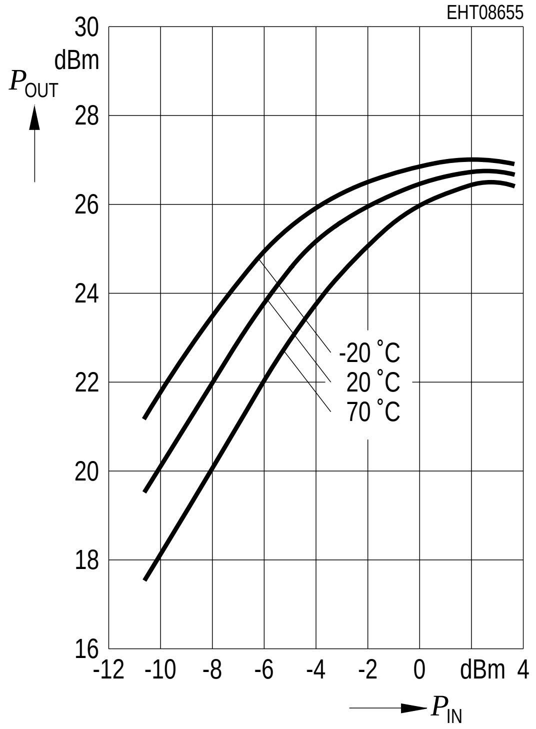
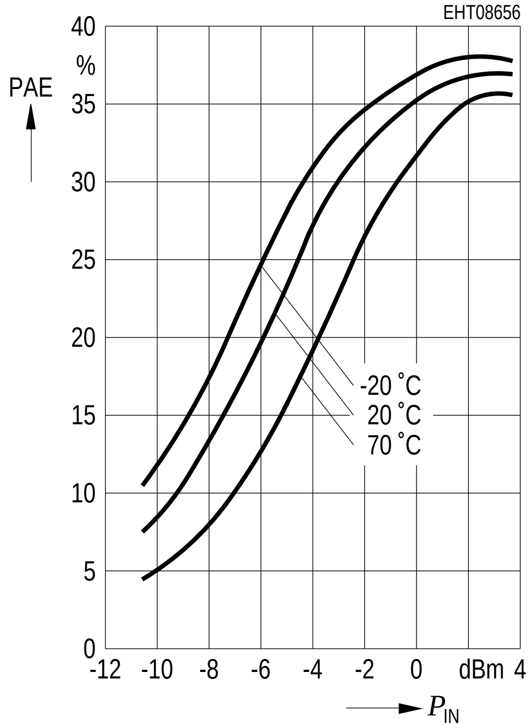


Figure 4 Principal Circuit

Output Power at Different Temperatures*



Power Added Efficiency at Different Temperatures*



* measured with a CGY 180 test circuit board (see **Page 10**),
V_D = 3 V, V_G = – 4 V, V_{TR} = 0 V

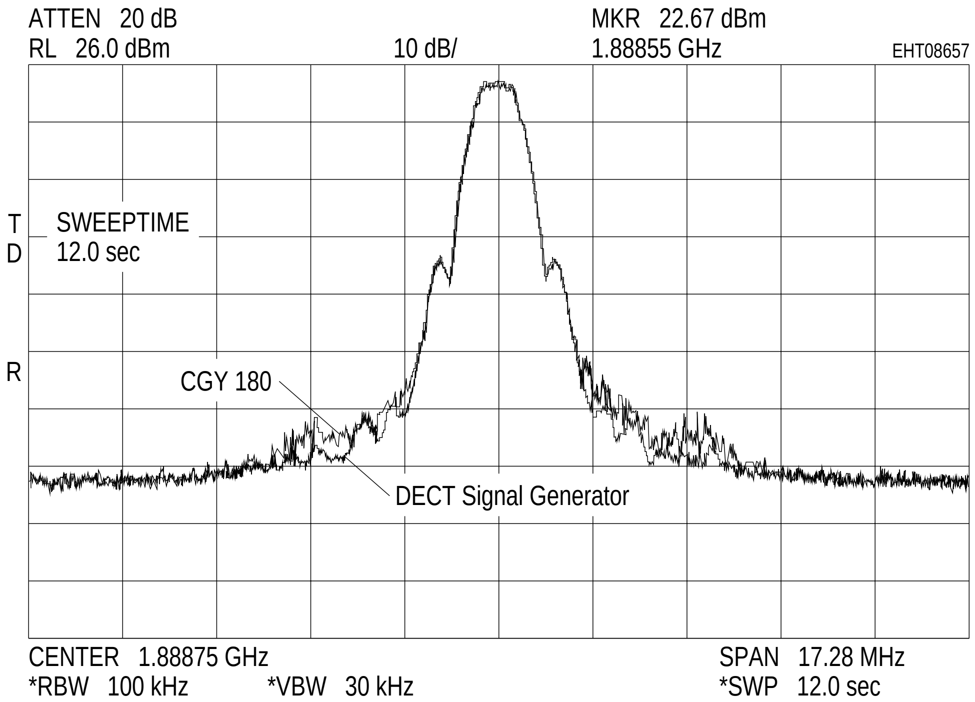


Figure 5 Emissions due to Modulation*
Spectrum of amplified DECT signal

* measured with a CGY 180 test circuit board (see **Page 10**),
V_D = 3 V, V_G = – 4 V, V_{TR} = 0 V

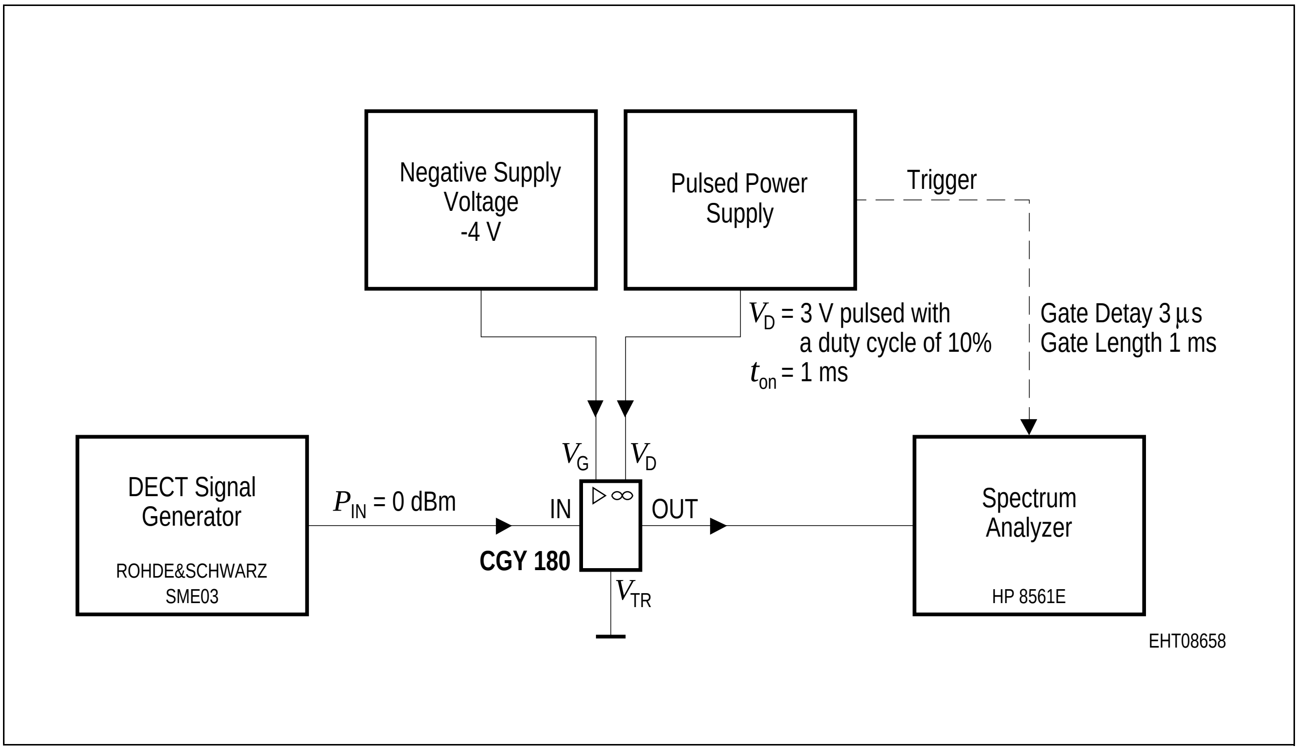


Figure 6 Measurement was done with the Following Equipment

Application Hints

1. CW - Capability of the CGY 180

1.1 V_D = 3 V

Proving the possibility of CW - operations there must be known the total power dissipation of the device. This value can be found as a function of the temperature in the data sheet (see **Page 9**). The CGY 180 has a maximum total power dissipation of P_{tot} = 2.3 W.

As an example we take the operating point with a drain voltage V_D = 3 V. The possible ratings of the drain current adjusted by the internal current control of the CGY 180 (V_G = – 4 V, V_{TR} = 0 V) are shown in the following table.

	min.	typ.	max.
I_D/mA	325	450	650

At worst case you see a current of I_D = 650 mA. So the maximum DC - power can be calculated to:

$P_{DC} = V_D \times I_D$ = 1.95 W

This value is smaller than 2.3 W and CW - operation is possible.

1.2 $\times$ V_D = 4 V

If you want to use the whole capability of the CGY 180, you must consider the power added efficiency PAE. You want to take an operation point of V_D = 4 V. Now there will be a higher current than at V_D = 3 V. We assume a current of I_D = 650 mA and a PAE = 35%. With these values the DC - power is P_{DC} = 2.6 W. That exceeds the P_{totDC} of 2.3 W. Decoupling RF-Power from the CGY 180 results in less power dissipation of the device. This is directly correlated with the achieved PAE. To calculate total power dissipation use the formula:

$P_{totDC} = P_{DC} \times (1 - \text{PAE})$

P_{tot} for the used operating point shown above will be

P_{tot} = 2.6 W $\times$ (1 – 0.35) = 1.69 W

It is possible to use the CGY 180 for CW - operations up to a drain voltage of V_D = 4 V, if at the same time a PAE of 35% is achieved.

The calculation can be done for any operating point to prove the capability of CW - operation.

2. Not Using the Internal Current Control

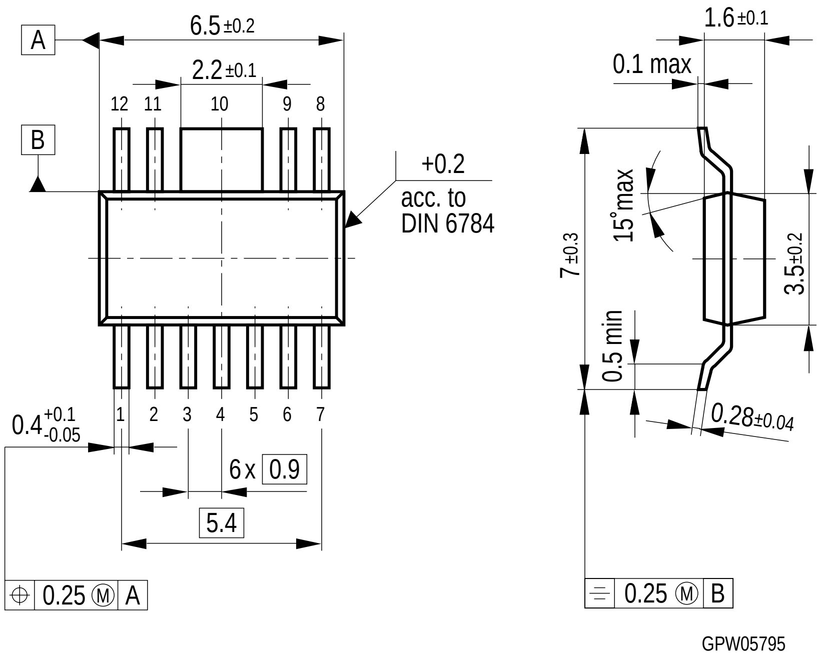
If you don’t want to use the internal current control, it is recommended to connect the negative supply voltage at pin 1 (V_{TR}) instead of pin 2 (V_G).

3. Biasing and Use Considerations

In all cases, RF input power should not be applied until the bias voltages have been applied, and RF input power should be turned off prior to removing the bias voltages. Bias application should be timed such that gate voltage (V_{GG}) is always applied before the drain voltages (V_{DD}), and when returning to the standby mode, gate voltage should only be removed once the drain voltages have been removed.

Package Outlines

MW-12
(Special Package)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm