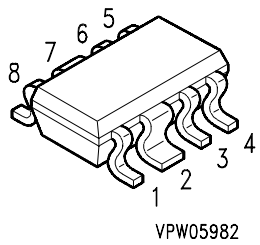
Datasheet

* Multiband Power Amplifier [800..3500 Mhz]
* DECT,PHS,PWT,Bluetooth,ISM900,ISM2400,WLL
* Single Voltage Supply
* Operating voltage range: 2V to 6 V
* Pout = 25.5dBm at Vd=2.4V
* Pout = 26.0dBm at Vd=3.0V
* Pout = 29.0dBm at Vd=5.0V
* Overall power added efficiency up to 50 %
* Easy external matching



ESD: **E**lectro**s**tatic **d**ischarge sensitive device, observe handling precautions!

Type	Marking	Ordering code (taped)	Package
CGY 196	D6s	Q62702-G0080	SCT598

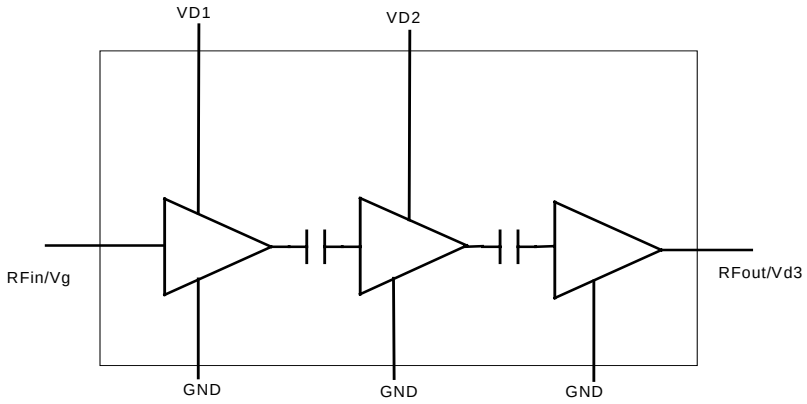
Maximum ratings

Characteristics	Symbol	max. Value	Unit
Positive supply voltage	V_D	6	V
Supply current	I_D	1.0	A
Maximum input power	*Pinmax*	20	dBm
Channel temperature	T_{Ch}	150	°C
Storage temperature	T_{stg}	-55...+150	°C
Total power dissipation *(Ts ≤ 80 °C)* *Ts: Temperature at soldering point*	P_{tot}	1.0	W
Pulse peak power	P_{Pulse}	2.0	W

Thermal Resistance

Channel-soldering point	R_{thChS}	70	K/W

Functional Block Diagram



Pin #		Configuration
1	**RFin/Vg**	RF input power + Gate voltage [0V internal]
2	**GND**	RF and DC ground
3	**VD2**	Pos. drain voltage of the 2nd stage
4	**n.c.**	not connected
5	**n.c.**	not connected
6	**RFout/VD3**	RF output power / Pos. drain voltage of the 3rd stage
7	**GND**	RF and DC ground
8	**VD1**	Pos. drain voltage of the 1st stage

DC characteristics

Characteristics		Symbol	Conditions	min	typ	max	Unit
Drain current	stage 1	*IDSS1*	VD1=3V	30	45	75	mA
	stage 2	*IDSS2*	VD2=3V	45	65	110	mA
	stage 3	*IDSS2*	VD2=3V	230	340	515	mA
Transconductance	stage 1	*gfs1*	VD=3V, ID=50mA	50	90	130	mS
	stage 2	*gfs2*	VD=3V, ID=300mA	80	130	170	mS
	stage 3	*gfs3*	VD=3V, ID=300mA	150	220	300	mS

Determination of Permissible Total Power Dissipation for Continuous and Pulse Operation

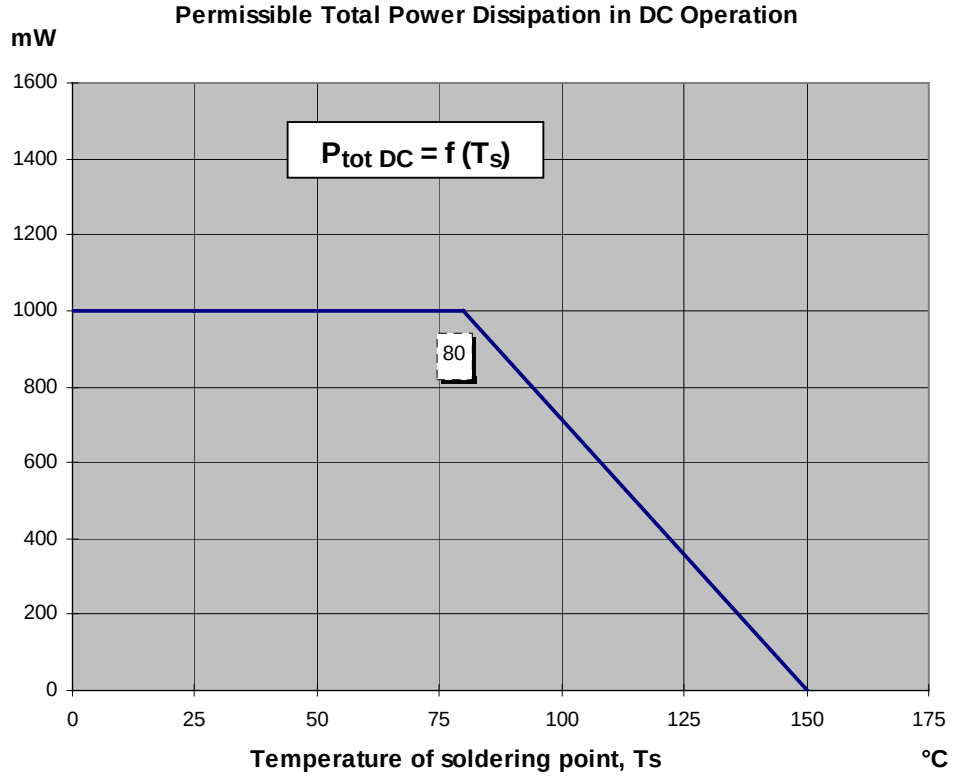
The dissipated power is the power which remains in the chip and heats the device. It does not contain RF signals which are coupled out consistently.

a) Continuous Wave / DC Operation

For the determination of the permissible total power dissipation $\mathbf{P_{tot\text{-}DC}}$ from the diagram below it is necessary to obtain the temperature of the soldering point T_S first. There are two cases:

- When R_{thSA} (soldering point to ambient) is not known: Measure T_S with a temperature sensor at the leads were the heat is transferred from the device to the board (normally at the widest source or ground lead for GaAs). Use a small sensor of low heat transport, for example a thermoelement (< 1mm) with thin wires or a temperature indicating paper while the device is operating.

- When R_{thSA} is already known: $T_S = P_{diss} \times R_{thSA} + T_A$



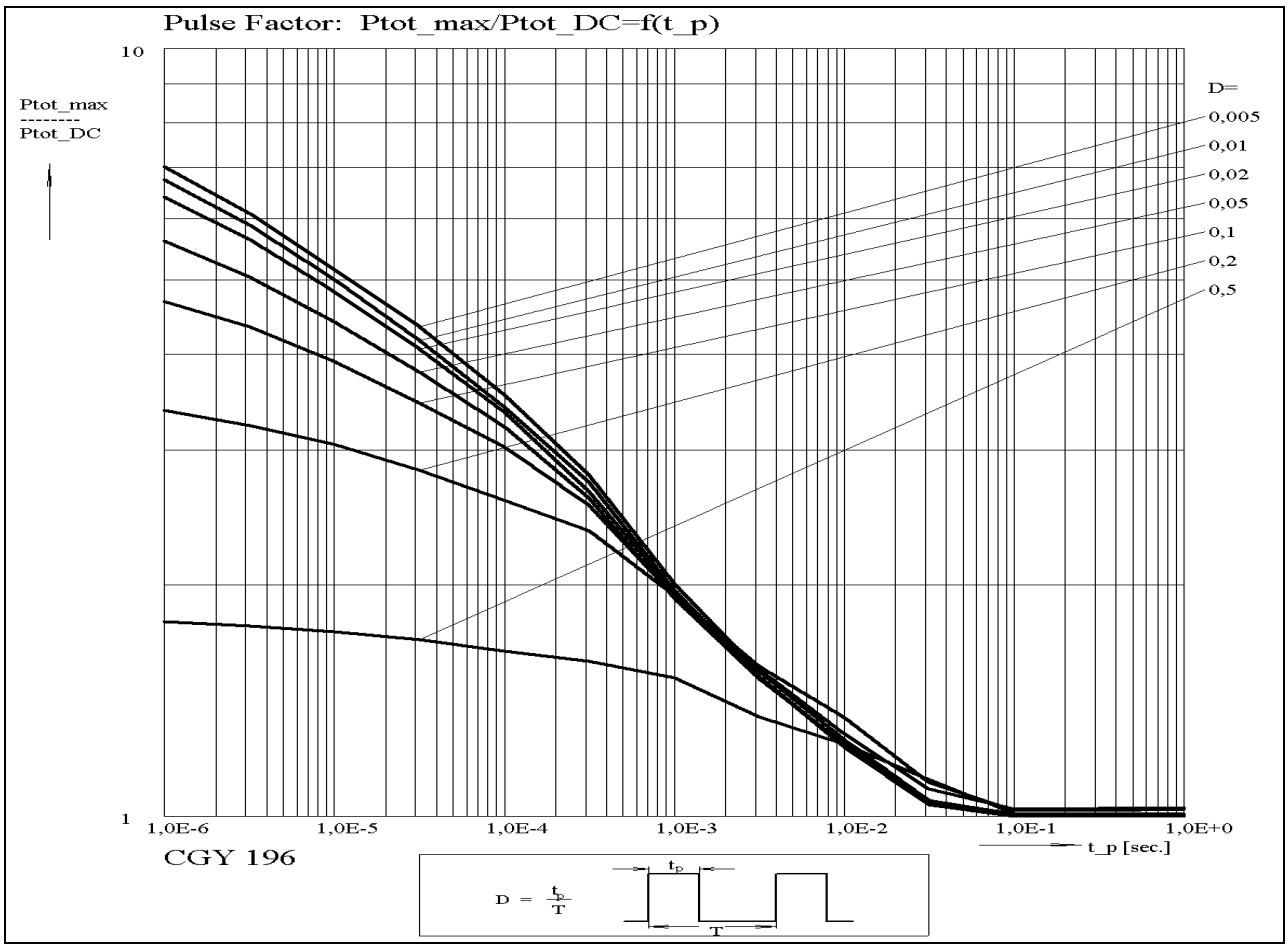
b) Pulsed Operation

For the calculation of the permissible pulse load $P_{tot\text{-}max}$ the following formula is applicable:

- $P_{tot\text{-}max} = P_{tot\text{-}DC} \times \text{Pulse factor}$
  $= P_{tot\text{-}DC} \times (P_{tot\text{-}max} / P_{tot\text{-}DC})$

Use the values for $P_{tot\text{-}DC}$ as derived from the above diagram and for the $\text{pulse factor} = P_{tot\text{-}max} / P_{tot\text{-}DC}$ from the following diagram to get a specific value.

Pulse factor:



$P_{tot\text{-}max}$ should not exceed the absolute maximum rating for the dissipated power P_{Pulse} = " Pulse peak power " = 2 W

c) Reliability Considerations

This procedure yields the upper limit for the power dissipation for continuous wave (cw) and pulse applications which corresponds to the maximum allowed channel temperature. For best reliability keep the channel temperature low. The following formula allows to track the individual contributions which determine the channel temperature.

T_{ch} =	(P_{diss} / Pulse Factor **x**	R_{thChS}) +	T_S
Channel temperature (= junction temperature)	Power dissipated in the chip, divided by the applicable puls factor (= 1 for DC and CW). It does not contain decoupled RF-power	Rth of device from channel to soldering point	Temperature of soldering point, measured or calculated

Electrical characteristics [3.0V DECT-Application f=1.89GHz]

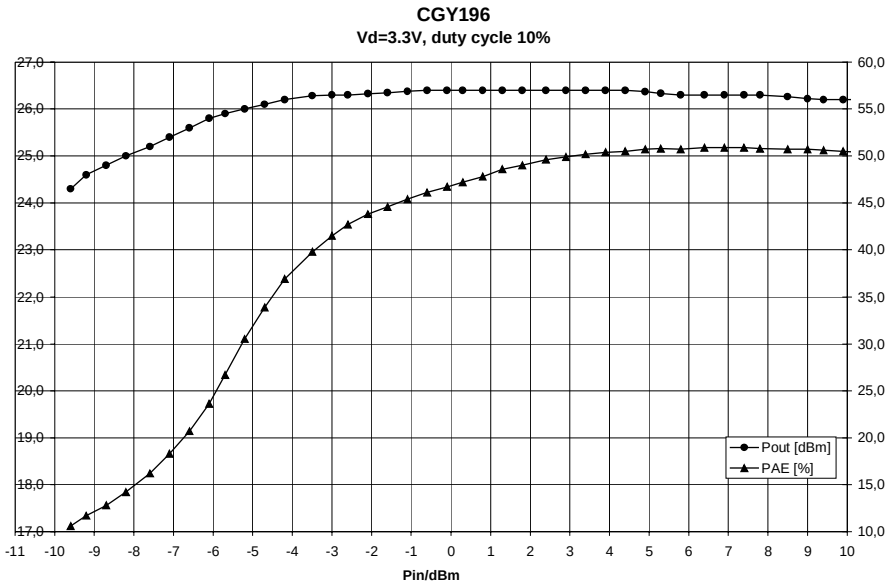
(T_A = 25°C , f=1.89 GHz, Z_S=Z_L=50 Ohm, unless otherwise specified)

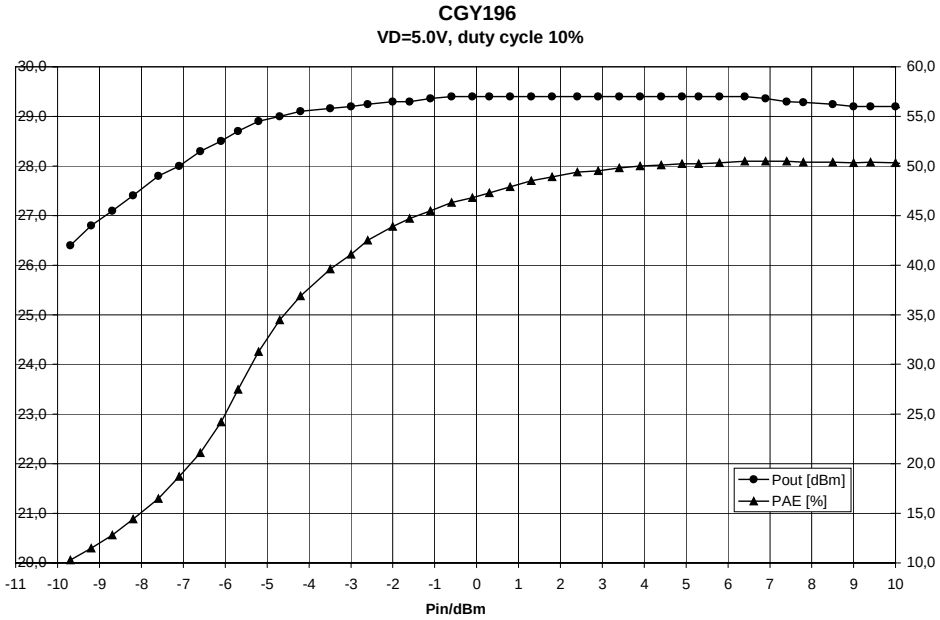
Characteristics	Symbol	min	typ	max	Unit
Supply current *VD=3.0V; Pin = +0 dBm*	I_{DD}	-	300	500	mA
Supply current *VD=3.0V; Pin = -10 dBm*	I_{DD}	-	450	700	mA
Gain *VD=3.0V; P_{in} = -10 dBm*	*G*	27	30	33	dB
Output Power *VD=3.0V; P_{in} = 0 dBm*	P_O	24.0	26.0	27.0	dBm
Overall Power added Efficiency *VD=3.0V; P_{in} = +0 dBm*	*PAE*	35	45	-	%
Overall Power added Efficiency *VD=3.0V; P_{in} = 3 dBm*	*PAE*		50	-	%
Supply current *VD=4.8V; Pin = -10 dBm*	I_{DD}	-	450	-	mA
Supply current *VD=4.8V; Pin = 0 dBm*	I_{DD}	-	330	600	mA
Gain *VD=4.8V; P_{in} = -10 dBm*	*G*	-	32	-	dB
Output Power *VD=4.8V; P_{in} = 3 dBm*	P_O	26.5	28	30	dBm
Overall Power added Efficiency *VD=4.8V; P_{in} = 3 dBm*	*PAE*	30	40	-	%
Overall Power added Efficiency *VD=4.8V; P_{in} = 5 dBm*	*PAE*		45	-	%
Off Isolation *VD=0V; P_{in} = 0 dBm*	*-S21*		40		dB
Load mismatch *Pin=0dBm , VD≤3.6V , Z_S=50 Ohm, Load VSWR = 20:1 for all phase,*	-	No module damage for 10 sec.			-
Load mismatch *Pin=3dBm , VD≤5.0V , Z_S=50 Ohm, Load VSWR = 20:1 for all phase,*	-	No module damage for 10 sec.			-
Stability *Pin=0dBm, VD=3.6V, Z_S=50 Ohm, Load VSWR = 10:1 for all phase*	-	All spurious output more than 70 dB below desired signal level			-
Stability *Pin=3dBm , VD=5.0V , Z_S=50 Ohm, Load VSWR = 10:1 for all phase,*	-	All spurious output more than 70 dB below desired signal level			-

Electrical characteristics [3.0V DECT-Application f=1.89GHz]

Output power and power added efficiency

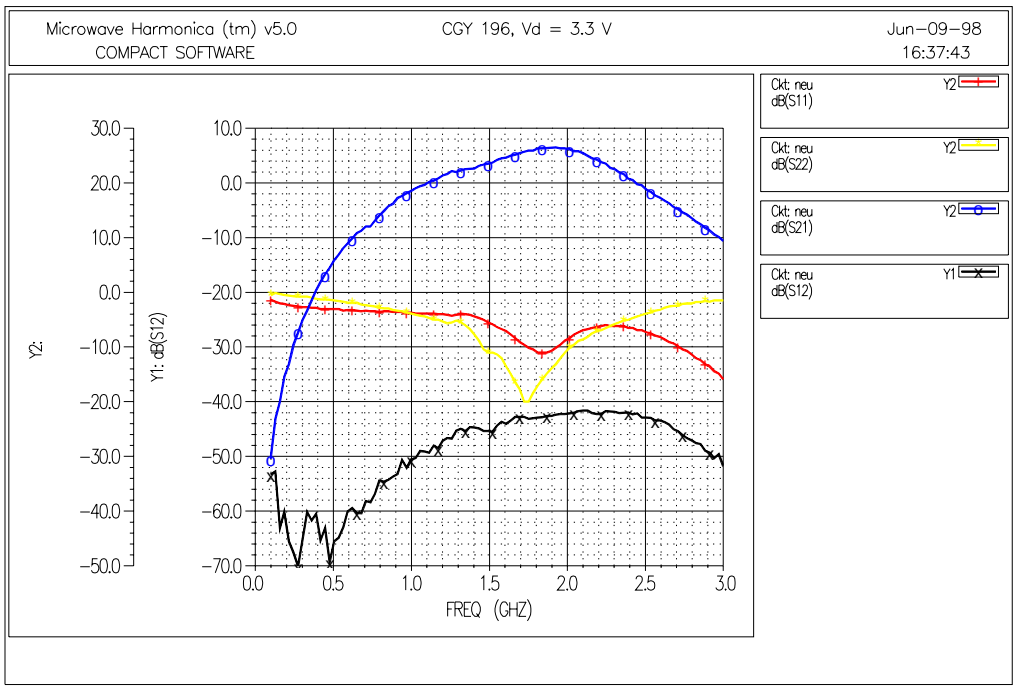
pulsed mode: T=417µs, duty cycle 12.5%



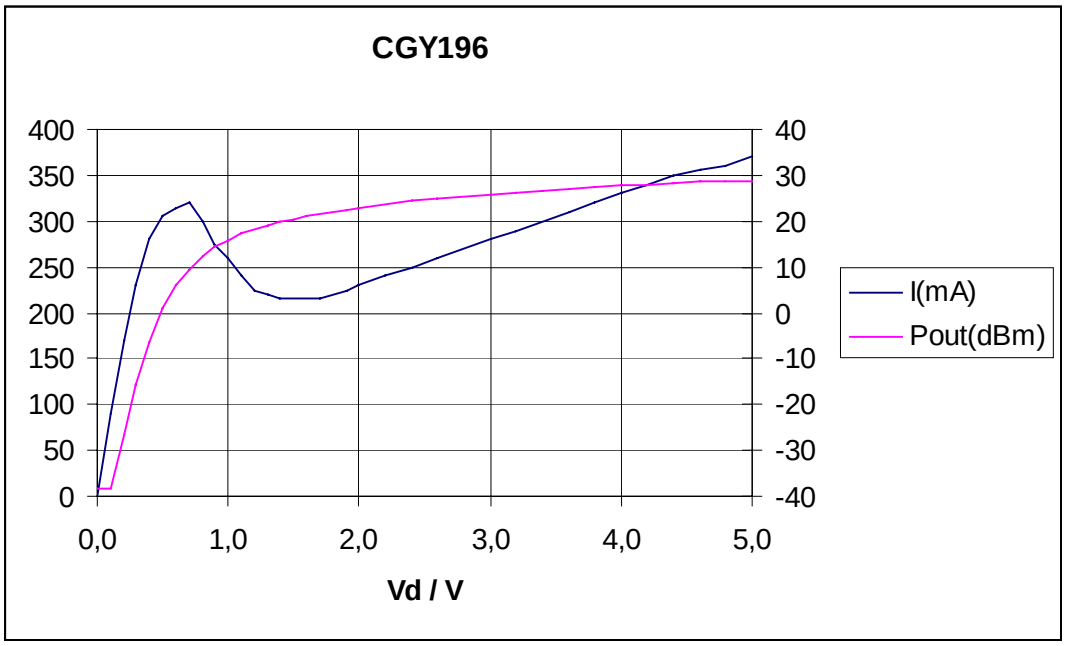


Electrical characteristics [3.0V DECT-Application f=1.89GHz]

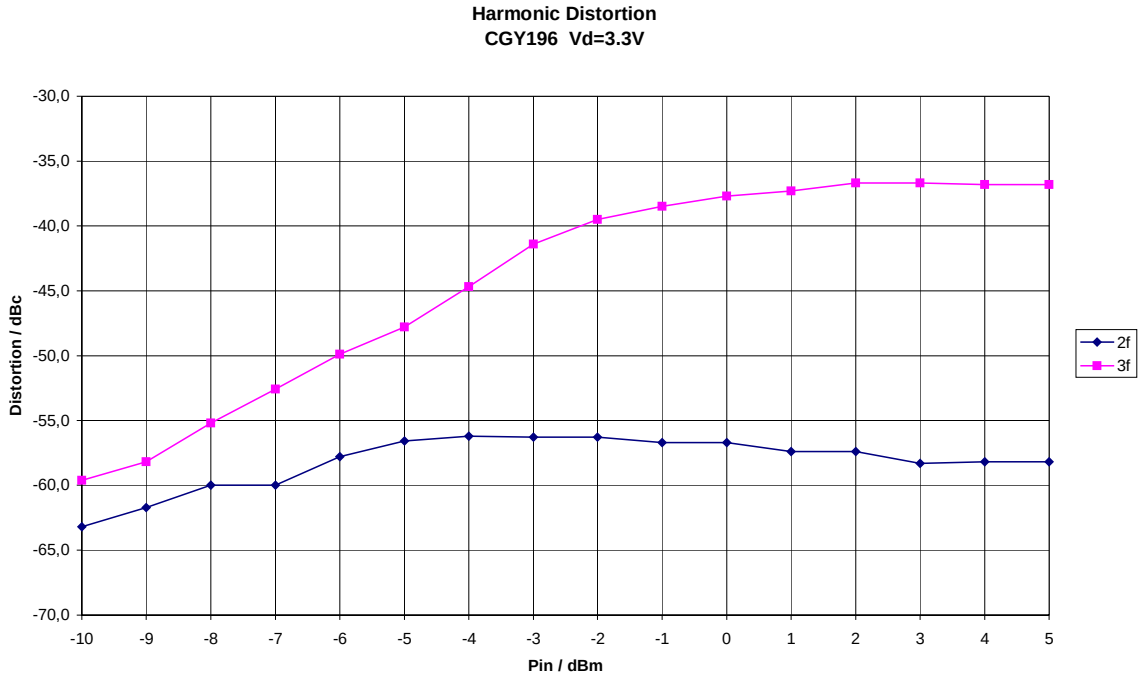
S-Parameter [pulsed mode: T=417µs, duty cycle 12.5%, Pin=0dBm,Vd=3.3V**]**

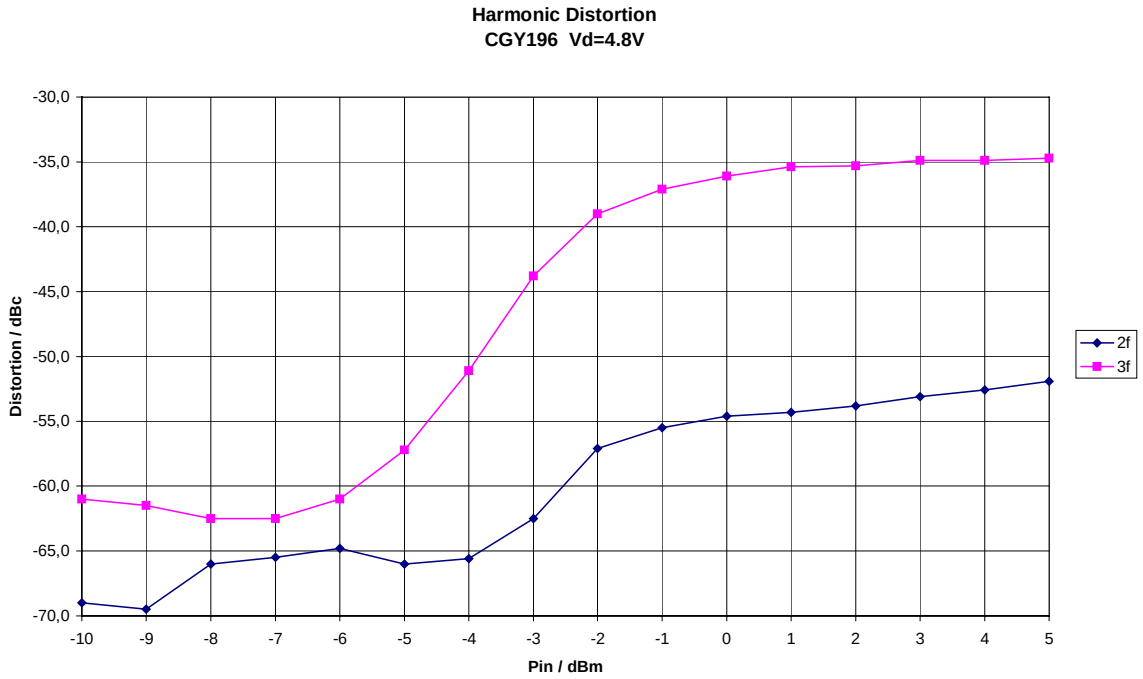


Pout,Id = f (Vd) | Pin=0dBm [pulsed mode: T=417µs, duty cycle 12.5%]

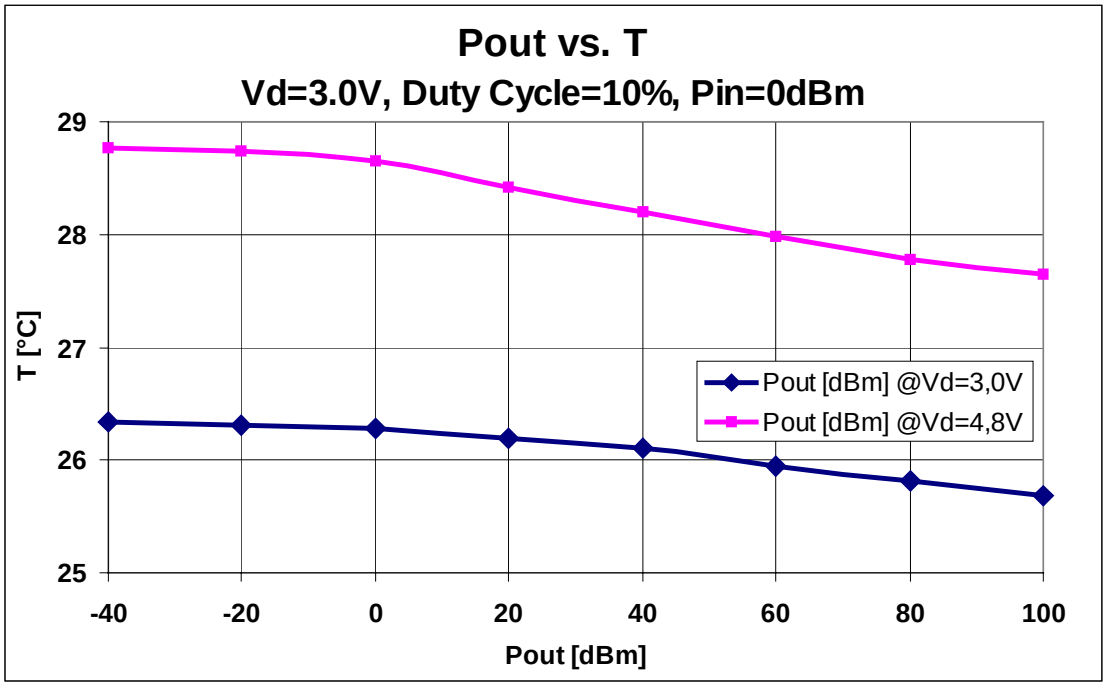


Electrical characteristics [3.0V DECT-Application f=1.89GHz]

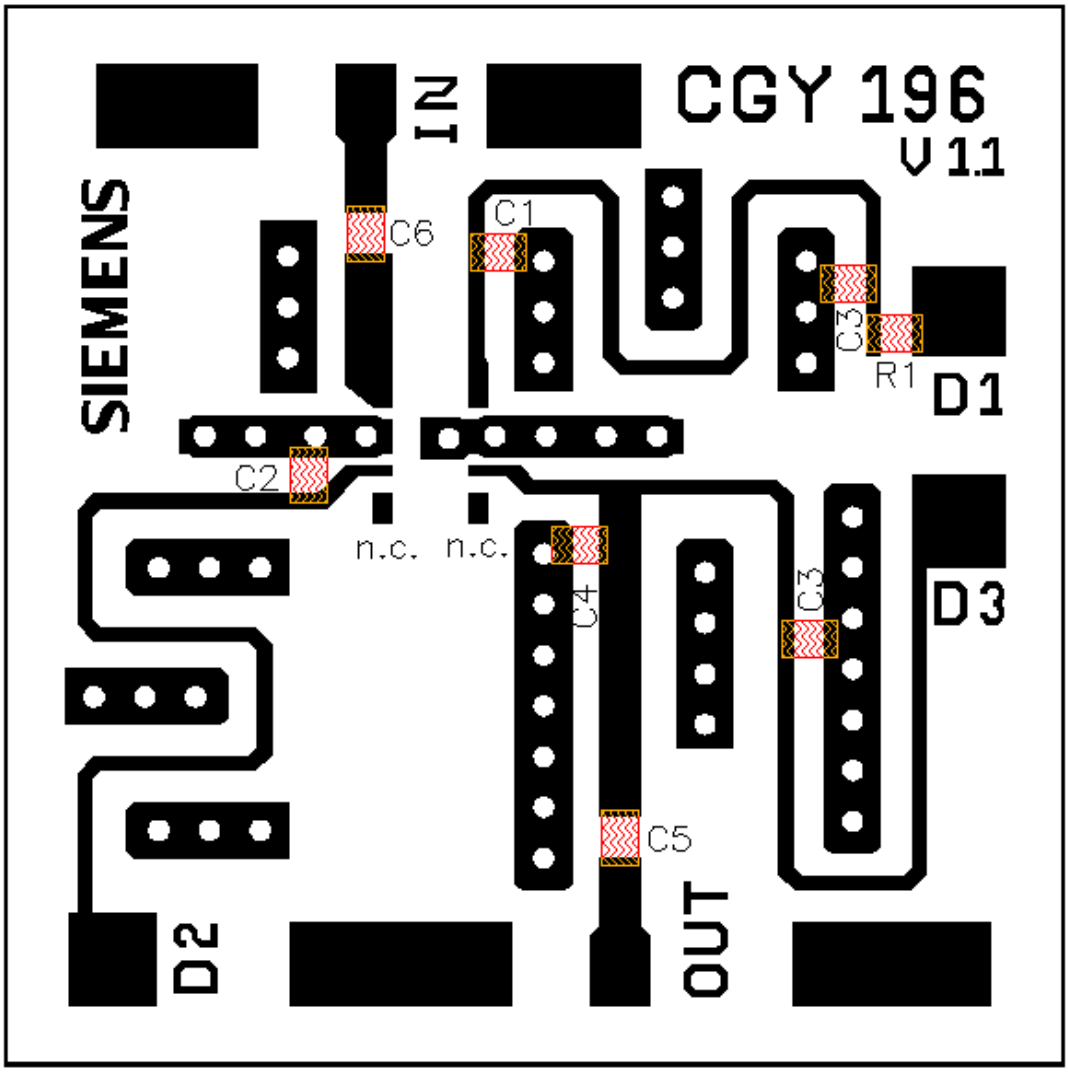




Electrical characteristics [3.0V DECT-Application f=1.89GHz]



Test Board Layout [3.0V DECT-Application f=1.89GHz]



C1 = C2 = C3 = 100nF
C4 = 3.3 pF
C5 = C6 = 680 pF
R1 = 2.7 Ohm

Electrical characteristics [2.4V DECT-Application f = 1.89 GHz]

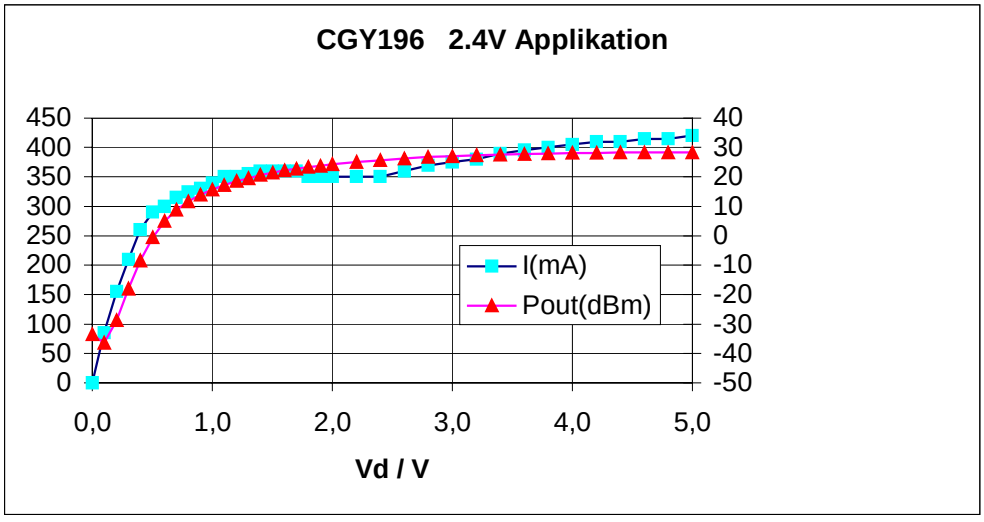
(T_A = 25°C , f=1.89 GHz, Z_S=Z_L=50 Ohm, unless otherwise specified)

Characteristics	Symbol	min	typ	max	Unit
Supply current *VD=2.4V; Pin = +0 dBm*	I_{DD}	-	340	-	mA
Supply current *VD=2.4V; Pin = -10 dBm*	I_{DD}	-	450	-	mA
Output Power *VD=2.4V; P_{in} = 0 dBm*	P_O		25.5		dBm
Overall Power added Efficiency *VD=2.4V; P_{in} = +0 dBm*	*PAE*		44	-	%
Supply current *VD=2.2V; Pin = +0 dBm*	I_{DD}	-	320	-	mA
Supply current *VD=2.2V; Pin = -10 dBm*	I_{DD}	-	450	-	mA
Output Power *VD=2.2V; P_{in} = 0 dBm*	P_O		24.7		dBm
Overall Power added Efficiency *VD=2.2V; P_{in} = +0 dBm*	*PAE*		42	-	%
Supply current *VD=3.0V; Pin = +0 dBm*	I_{DD}	-	380	-	mA
Supply current *VD=3.0V; Pin = -10 dBm*	I_{DD}	-	450	-	mA
Output Power *VD=3.0V; P_{in} = 0 dBm*	P_O		27.0		dBm
Overall Power added Efficiency *VD=3.0V; P_{in} = +0 dBm*	*PAE*		44	-	%
Off Isolation *VD=0V; P_{in} = 0 dBm*	*-S21*		35		dB

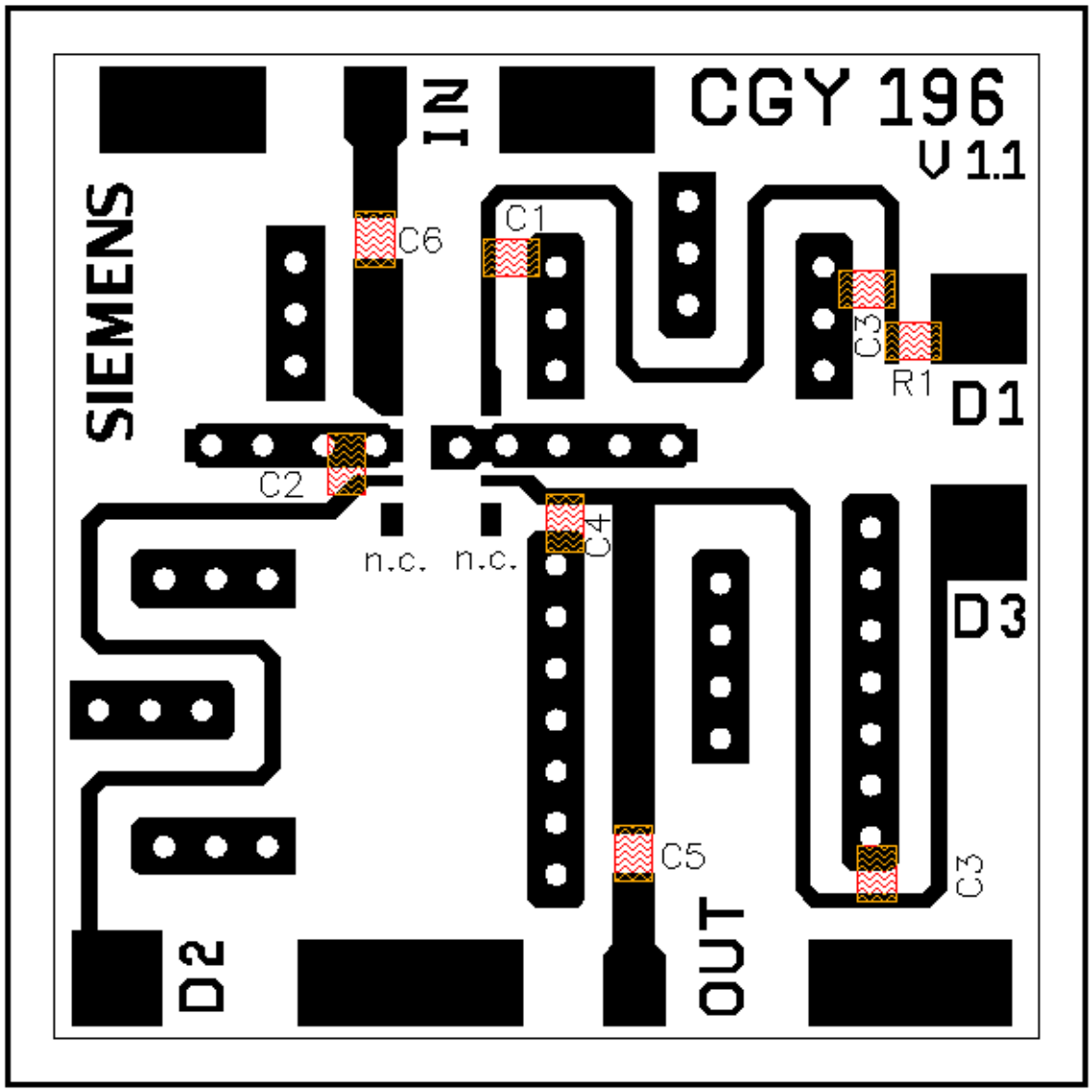
Electrical characteristics [2.4V DECT-Application f = 1.89 GHz]

Load mismatch *Pin=0dBm , VD≤3.0V , Z_S=50 Ohm,* *Load VSWR = 20:1 for all phase,*	-	No module damage for 10 sec.	-
Load mismatch *Pin=3dBm , VD≤5.0V , Z_S=50 Ohm,* *Load VSWR = 20:1 for all phase,*	-	No module damage for 10 sec.	-
Stability *Pin=0dBm, VD=3.0V, Z_S=50 Ohm,* *Load VSWR = 3:1 for all phase*	-	All spurious output more than 70 dB below desired signal level	-
Stability *Pin=3dBm , VD=5.0V , Z_S=50 Ohm,* *Load VSWR = 3:1 for all phase,*	-	All spurious output more than 70 dB below desired signal level	-

Pout,Id = f (Vd) | Pin=0dBm [pulsed mode: T=417µs, duty cycle 12.5%]



Test Board Layout [2.4V DECT-Application f=1.89GHz]



C1 = C2 = C3 = 100nF
C4 = 3.3 pF
C5 = C6 = 680 pF
R1 = 2.7 Ohm

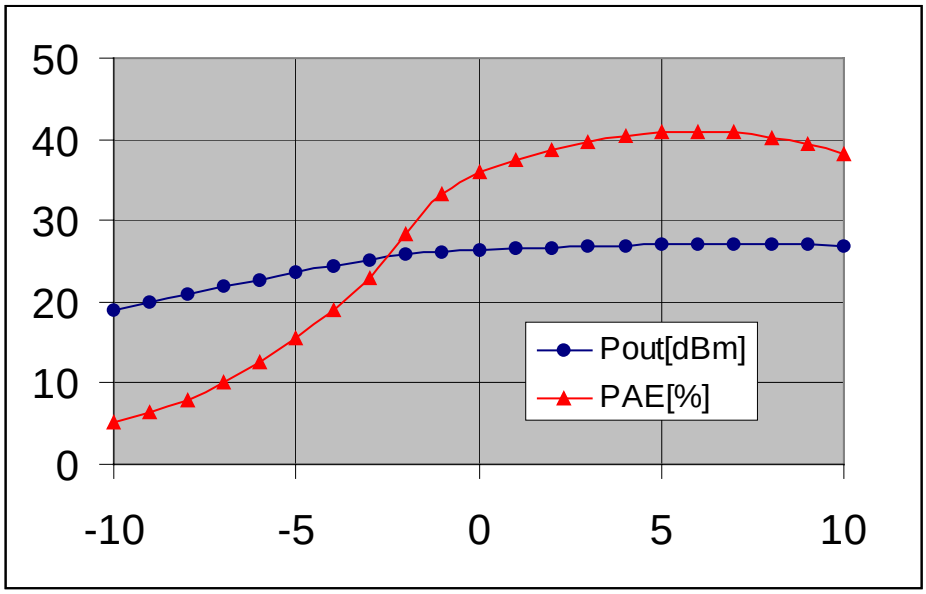
Electrical characteristics [2.4GHZ ISM-Application]

(T_A = 25°C , f=1.89 GHz, Z_S=Z_L=50 Ohm, unless otherwise specified)

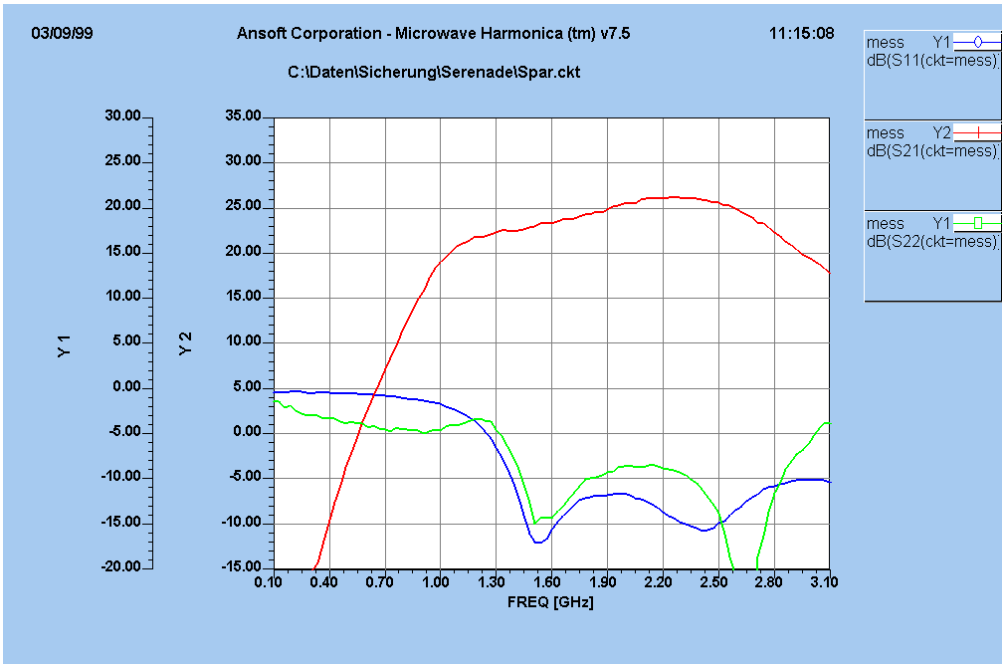
Characteristics	Symbol	min	typ	max	Unit
Supply current *VD=3.3V; Pin = +3 dBm*	I_{DD}	-	300	-	mA
Supply current *VD=3.3V; Pin = -10 dBm*	I_{DD}	-	450	-	mA
Output Power *VD=3.3V; P_{in} = +3 dBm*	P_O		26.0		dBm
Overall Power added Efficiency *VD=3.3V; P_{in} = +3 dBm*	*PAE*		40	-	%
Off Isolation *VD=0V; P_{in} = 3 dBm*	*-S21*		34		dB
Supply current *VD=4.8V; Pin = +6 dBm*	I_{DD}	-	300	-	mA
Supply current *VD=4.8V; Pin = -10 dBm*	I_{DD}	-	450	-	mA
Output Power *VD=4.8V; P_{in} = +6 dBm*	P_O		27.5		dBm
Overall Power added Efficiency *VD=4.8V; P_{in} = +6 dBm*	*PAE*		40	-	%
Off Isolation *VD=0V; P_{in} = 3 dBm*	*-S21*		34		dB
Load mismatch *Pin=3 dBm , VD≤3.6V , Z_S=50 Ohm, Load VSWR = 20:1 for all phase,*	-	No module damage for 10 sec.			-
Load mismatch *Pin=6 dBm , VD≤5.0V , Z_S=50 Ohm, Load VSWR = 20:1 for all phase,*	-	No module damage for 10 sec.			-
Stability *Pin=3 dBm, VD=3.6V, Z_S=50 Ohm, Load VSWR = 10:1 for all phase*	-	All spurious output more than 70 dB below desired signal level			-
Stability *Pin=6 dBm , VD=5.0V , Z_S=50 Ohm, Load VSWR = 10:1 for all phase,*	-	All spurious output more than 70 dB below desired signal level			-

Electrical characteristics [2.4GHZ ISM-Application]

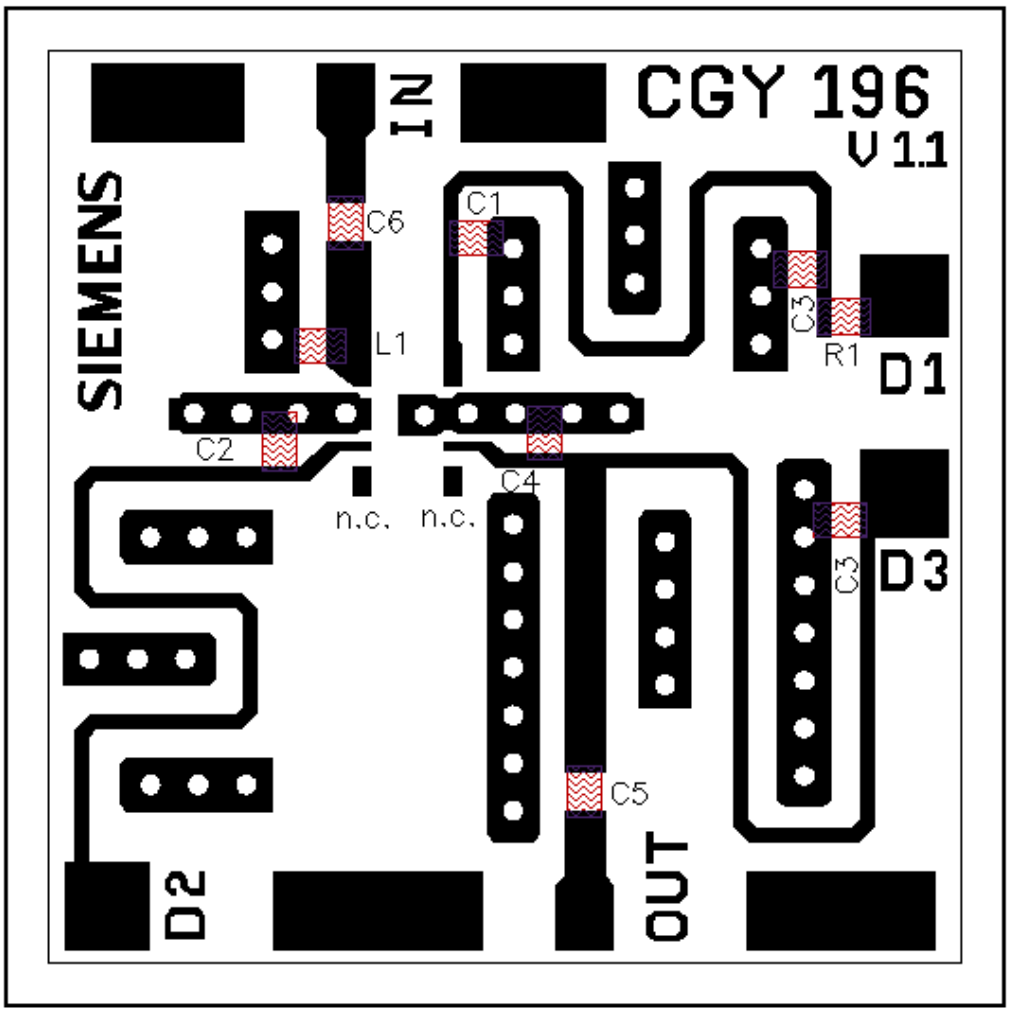
Pout,PAE = f (Pin) | Vd=3.3V f=2.4GHz [pulsed mode: T=417µs, duty cycle 12.5%]



S-Parameter Vd=3.3V Pin=0dBm [pulsed mode: T=417µs, duty cycle 12.5%]



Test Board Layout [2.4 GHz ISM - Application]



C1 = C2 = C3 = 100nF L1 = 3n9
C4 = 1p8
C5 = C6 = 1 nF
R1 = 2.7 Ohm

Electrical characteristics [900 MHz ISM-Application]

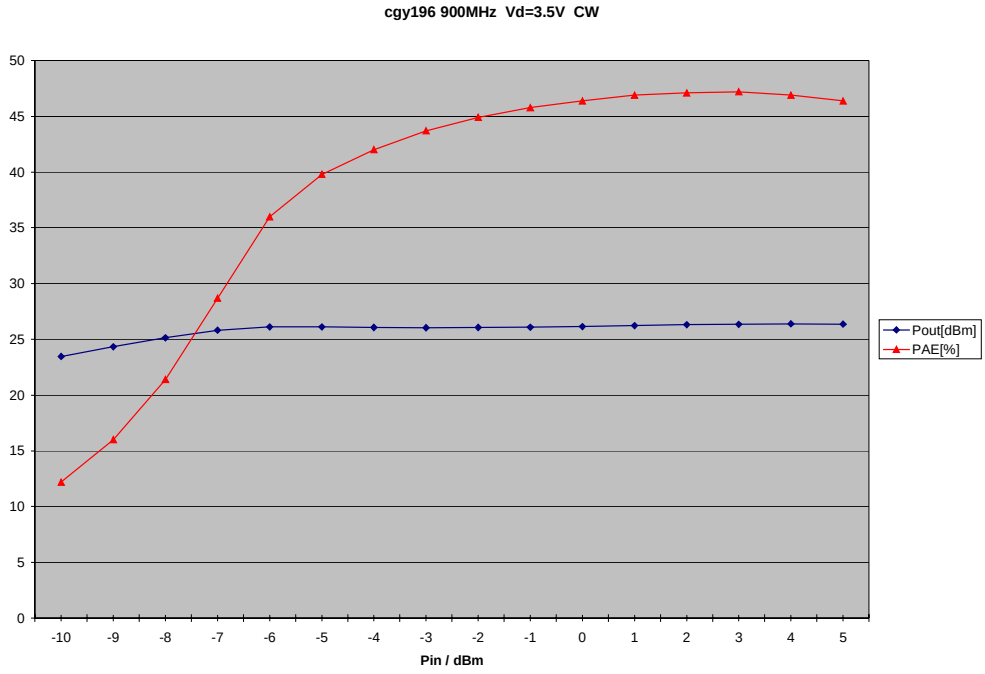
(T_A = 25°C , f=1.89 GHz, Z_S=Z_L=50 Ohm, unless otherwise specified)

Characteristics	Symbol	min	typ	max	Unit
Supply current *VD=3.3V; Pin = +3 dBm*	I_{DD}	-	300	-	mA
Supply current *VD=3.3V; Pin = -10 dBm*	I_{DD}	-	450	-	mA
Output Power *VD=3.3V; P_{in} = +3 dBm*	P_O		26.0		dBm
Overall Power added Efficiency *VD=3.3V; P_{in} = +3 dBm*	*PAE*		40	-	%
Off Isolation *VD=0V; P_{in} = 3 dBm*	*-S21*		34		dB
Supply current *VD=4.8V; Pin = +6 dBm*	I_{DD}	-	300	-	mA
Supply current *VD=4.8V; Pin = -10 dBm*	I_{DD}	-	450	-	mA
Output Power *VD=4.8V; P_{in} = +6 dBm*	P_O		27.5		dBm
Overall Power added Efficiency *VD=4.8V; P_{in} = +6 dBm*	*PAE*		40	-	%
Off Isolation *VD=0V; P_{in} = 3 dBm*	*-S21*		34		dB

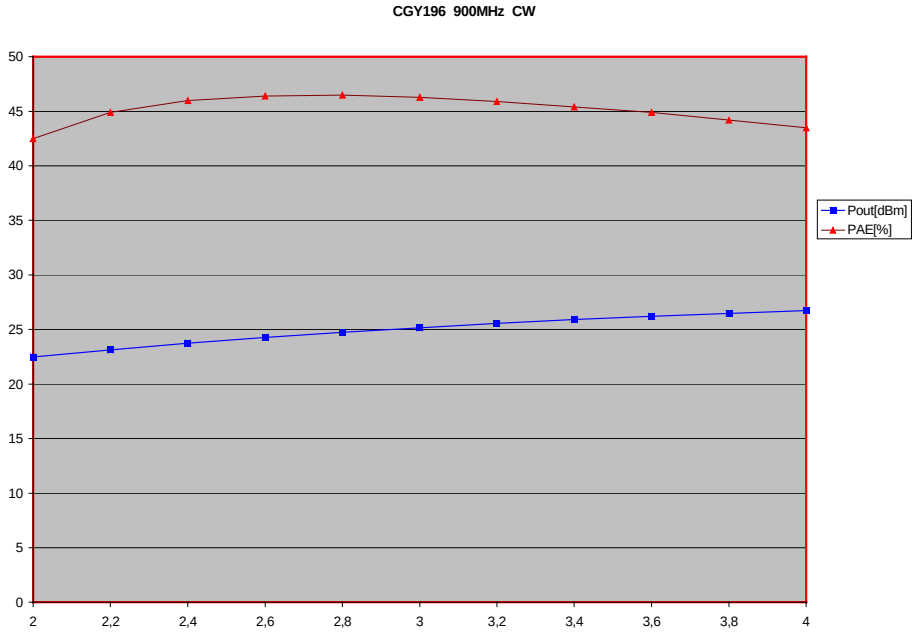
Load mismatch *Pin=3 dBm , VD≤3.6V , Z_S=50 Ohm, Load VSWR = 20:1 for all phase,*	-	No module damage for 10 sec.	-
Load mismatch *Pin=6 dBm , VD≤5.0V , Z_S=50 Ohm, Load VSWR = 20:1 for all phase,*	-	No module damage for 10 sec.	-
Stability *Pin=3 dBm, VD=3.6V, Z_S=50 Ohm, Load VSWR = 10:1 for all phase*	-	All spurious output more than 70 dB below desired signal level	-
Stability *Pin=6 dBm , VD=5.0V , Z_S=50 Ohm, Load VSWR = 10:1 for all phase,*	-	All spurious output more than 70 dB below desired signal level	-

Electrical characteristics [900 MHz ISM-Application]

Pout,PAE = f (Pin) | Vd=3.5V f=900 MHz [CW]

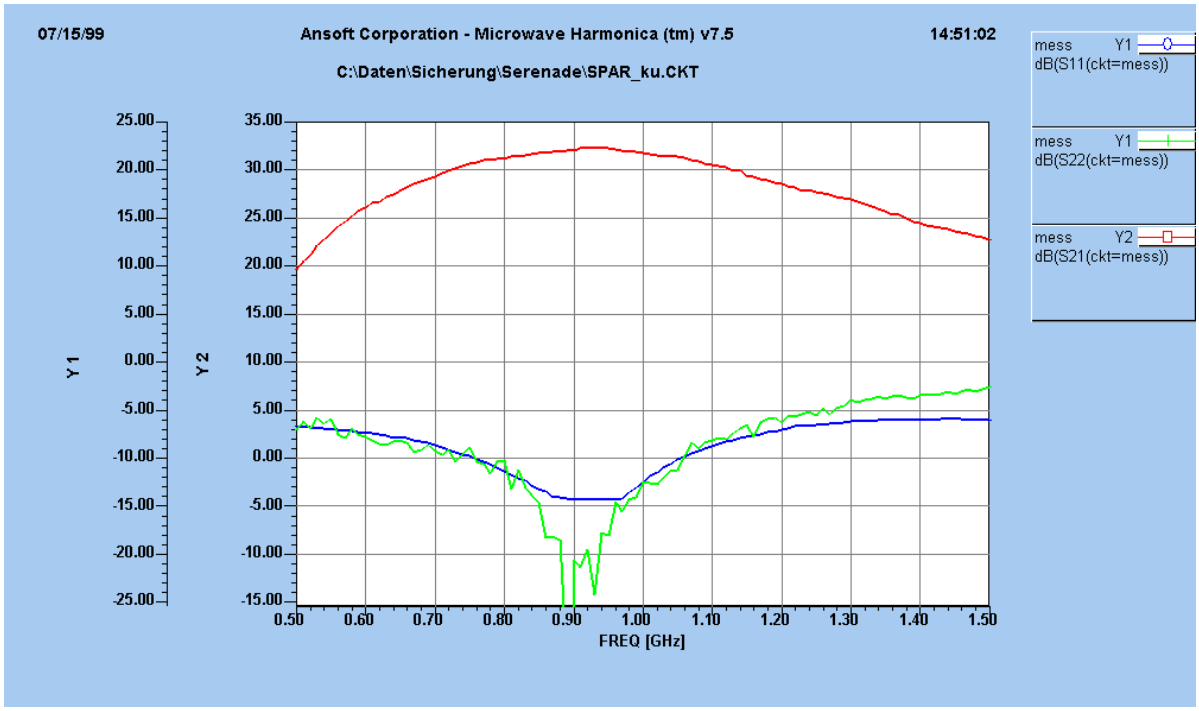


Pout,PAE = f (Vd) | Pin=0 dBm f=900 MHz [CW]

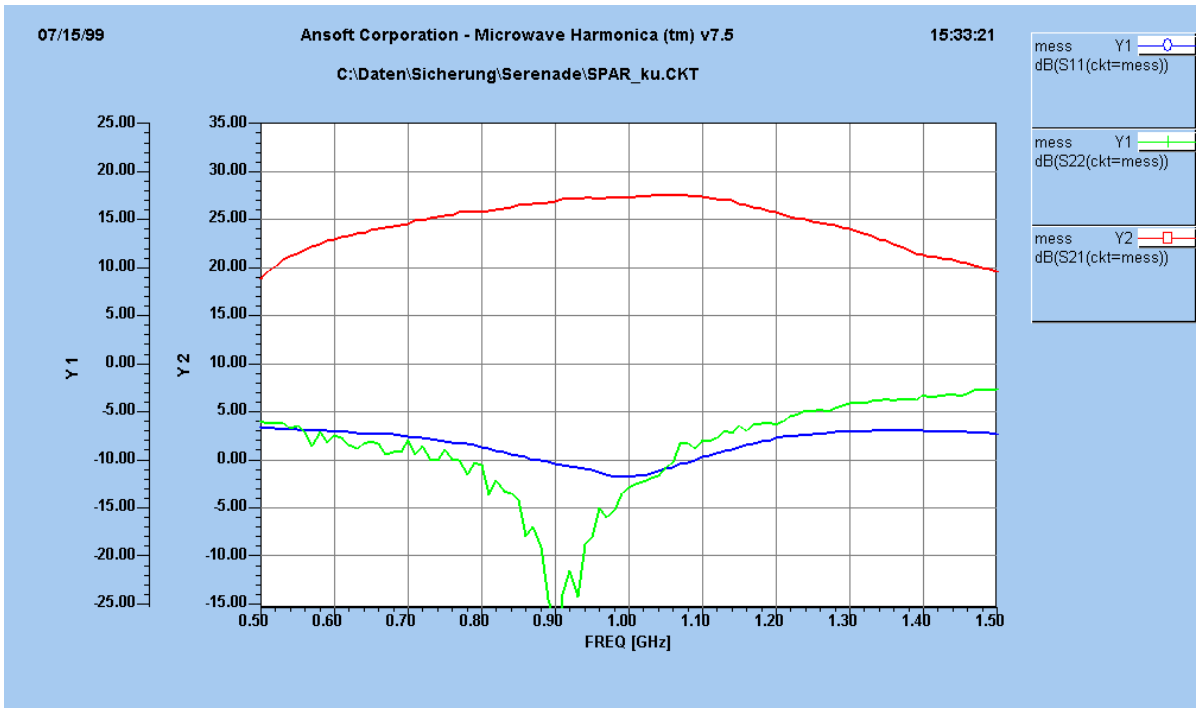


Electrical characteristics [900 MHz ISM-Application]

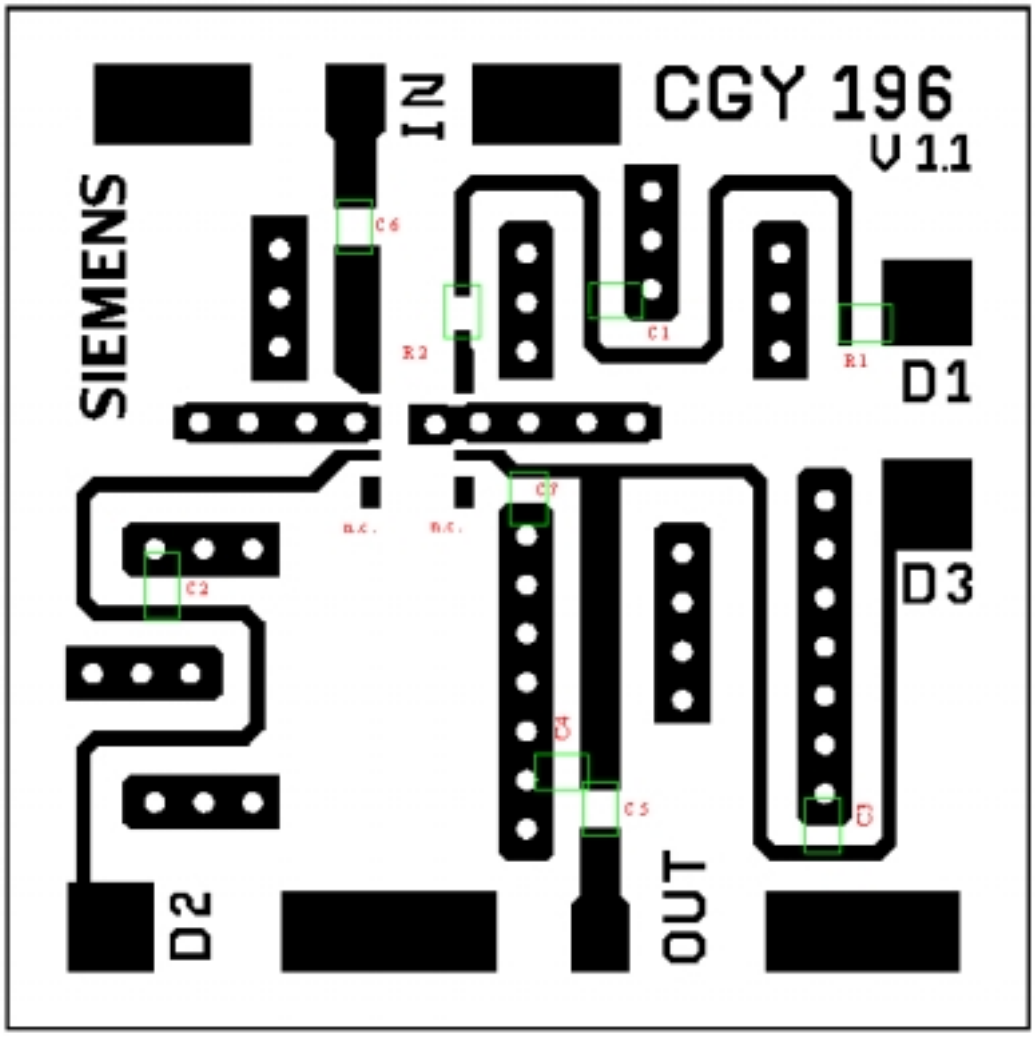
S-Parameter Vd=3.5V Pin=-5.5 dBm [cw mode]



S-Parameter Vd=3.5V Pin=-0.5 dBm [cw mode]



Test Board Layout [900 MHz ISM - Application]



C1 = 47pF
C3 = 100nF
C4 = 5.6pF
C2 = 47pF
C5 = C6 = 680 pF
C7 = 1pF
R1 = 2.7 Ohm
R2 = 10 Ohm

Scale: 8.99:1

SIEMENS	High Frequency Semiconductors		
Type CGY196 GaAs MMIC	*Package* SCT598	*File* C:\TEMP\SCT595-C196_PriLötempf.doc	*Date* 05.02.1999
Key-word Notes on Processing			

Preliminary soldering recommendation

- **Foot Print** — drawing C63060-A2123-A001-01-0027

- **Soldering**

  wave soldering: unsuitable
  reflow soldering: suitable, max. 3 times (IR or VPR)

  soldering profile:

ramp-up preheating	temperature gradient:	max. + 2 K/sec
	time at 100 - 150 °C:	min. 90 sec.
ramp-up peak	temperature gradient	max. + 6 K/sec
exposure to molten solder	above 183°C	max. 150 sec
typ. solder temperature	typ. 215-245°C	max. 30 sec.
peak temperature	max. peak 260°C	max. 10 sec.
ramp-down	temperature gradient:	min. - 6°C/sec

  (see also soldering standard profile of databook ‘package information’)

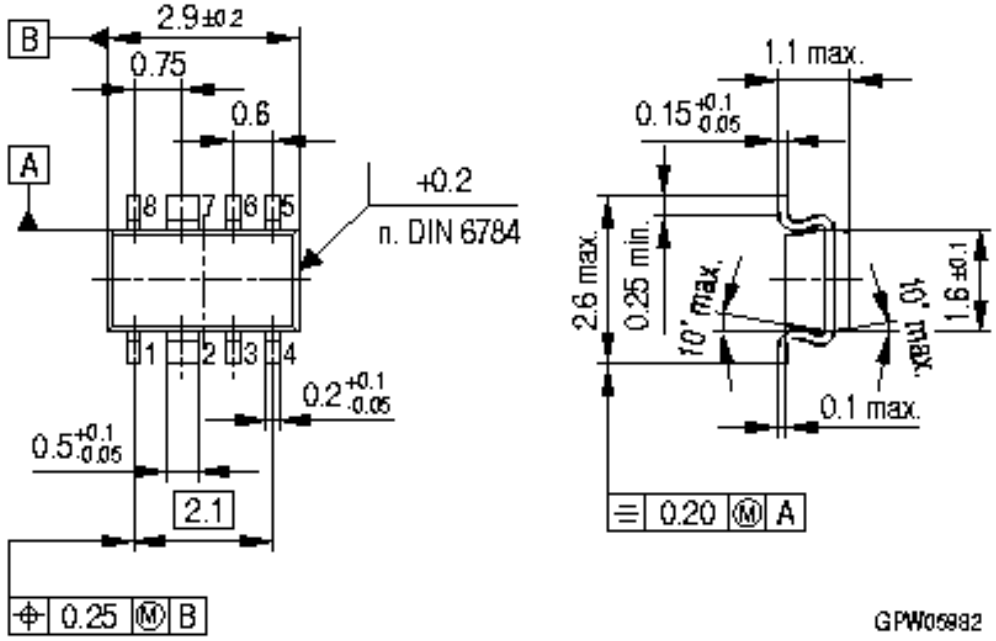
  comments: slow ramp-up, long preheating phase and low max. temperature recommended

- **Solder paste thickness** — 150 - 200 µm

- **Control of soldering** (voids)
  - visual inspection
  - cross sectioning
  - measurement of case temperature / thermal resistance case to ambient

- **Jedec A-112A** — level 1 — storage floor life at 30°C/90% unlimited

- **IPC-9501 (IPC-4202)** — level 111 — storage floor life at 30°C/60% unlimited IR/Convection; max. 245°C; < 6K/sec.



Published by Infineon AG, Bereich Wireless Systems, Marketing-Kommunikation,
Balanstraße 73, D-81541 München.

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