

DATA SHEET

CGY2105ATS

High dynamic range dual LNA
MMIC

Preliminary specification
File under Integrated Circuits, IC17

1999 Dec 23

High dynamic range dual LNA MMIC

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FEATURES

- Dual Low Noise Amplifier (LNA) Monolithic Microwave Integrated Circuit (MMIC)
- Typical noise figure of 0.55 dB
- Typical gain of 16.3 dB at 1810 MHz
- Input IP3 of 13.5 dBm at 1810 MHz
- Low current of 58 mA at 2.5 V for each channel
- Low cost SSOP16 plastic package.

APPLICATIONS

- DCS1800
- PCS1900.

GENERAL DESCRIPTION

The CGY2105 is a dual Gallium Arsenide (GaAs) MMIC amplifier designed for use in very low noise figure applications, where high linearity is also required.

Excellent tracking between the two amplifiers is obtained. Gain and noise figure variations with temperature are very small.

The device is suitable for use in DCS1800 and PCS1900 base station applications.

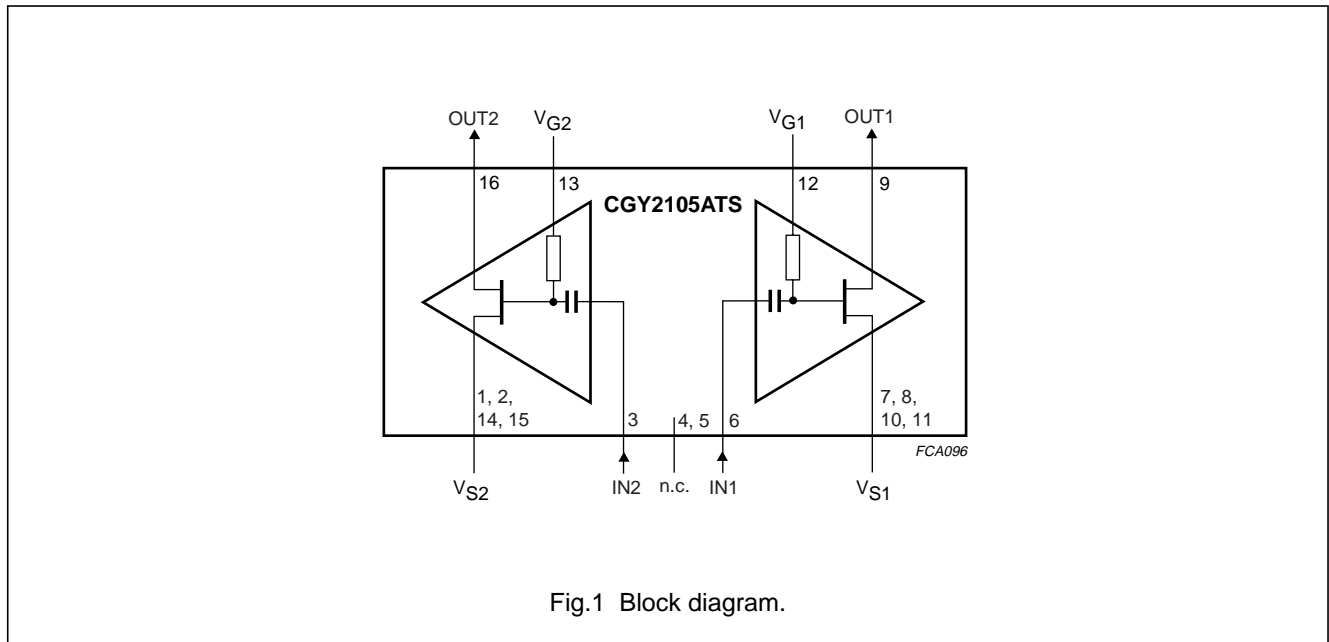
It also provides high gain and very low noise performance at frequencies between 1.0 and 2.5 GHz, as used in Wireless Local Area Network (WLAN) applications.

A rematching of the application board might be necessary for optimum performance.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
CGY2105ATS	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1

BLOCK DIAGRAM



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PINNING

SYMBOL	PIN	DESCRIPTION
V _{S2}	1, 2, 14 and 15	amplifier 2 source
IN2	3	amplifier 2 input
n.c.	4	not connected
n.c.	5	not connected
IN1	6	amplifier 1 input
V _{S1}	7, 8, 10 and 11	amplifier 1 source
OUT1	9	amplifier 1 drain output
V _{G1}	12	amplifier 1 gate bias
V _{G2}	13	amplifier 2 gate bias
OUT2	16	amplifier 2 drain output

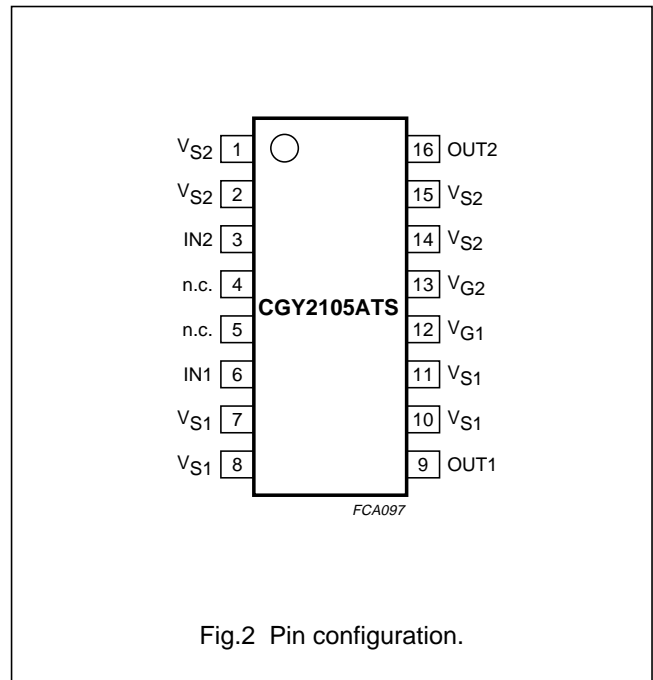


Fig.2 Pin configuration.

LIMITING VALUES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{DS}	drain-source voltage		–	–	5	V
V _{GS}	gate-source voltage		–3	–	+1	V
V _{DG}	drain-gate voltage		–	–	7	V
V _{supply}	positive supply voltage	see Chapter “Application and test information”	–	–	6	V
V _{neg}	negative supply voltage	see Chapter “Application and test information”	–6	–	–	V
T _{amb}	ambient temperature		–40	–	+85	°C
T _j	junction temperature		–	–	150	°C
T _{stg}	storage temperature		–	–	150	°C
P _{tot}	total power dissipation	T _{amb} < 85 °C	–	–	430	mW

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
R _{th(j-a)}	thermal resistance from junction to ambient	138	K/W

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CHARACTERISTICS

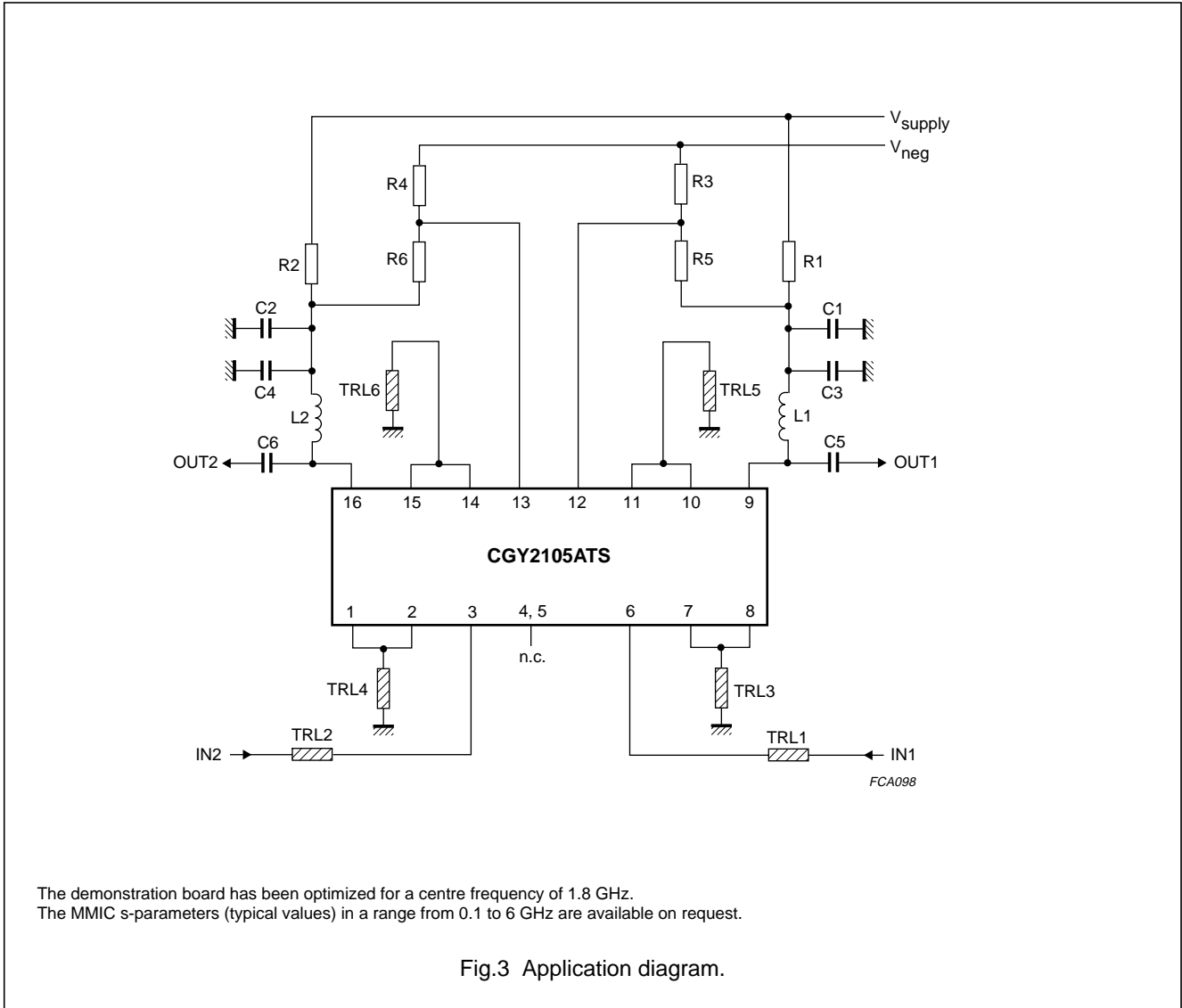
$T_{amb} = 25\text{ °C}$; measured and guaranteed only for the application shown in Chapter "Application and test information"; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
I_{supply}	positive supply current (for each LNA)	$V_{supply} = 5.0\text{ V};$ $V_{neg} = -5.0\text{ V}$	42	58	72	mA
I_{neg}	negative supply current (for each LNA)	$V_{supply} = 5.0\text{ V};$ $V_{neg} = -5.0\text{ V}$	–	0.3	0.4	mA
Amplifiers: $V_{supply} = 5.0\text{ V}; V_{neg} = -5.0\text{ V}; Z_0 = 50\text{ }\Omega$; both LNAs biased; duty cycle 100%						
f_i	input frequency		1710	–	1910	MHz
G	gain	$f_i = 1710\text{ MHz}$	16	16.9	17.8	dB
		$f_i = 1710\text{ to }1910\text{ MHz}$	14.8	16.3	17.8	dB
$\Delta G_{(T)}$	gain variation with temperature	$-40\text{ °C} < T_{amb} < +85\text{ °C}$	–	± 0.45	–	dB
NF	noise figure		–	0.55	0.8	dB
$\Delta NF_{(T)}$	noise figure variation with temperature	$-40\text{ °C} < T_{amb} < +85\text{ °C}$	–	± 0.25	–	dB
IP3 _i	input third-order intercept point	$\Delta f = \pm 0.5\text{ MHz}$	11	13.5	–	dBm
$\Delta IP3_{i(T)}$	input third-order intercept point variation with temperature	$-40\text{ °C} < T_{amb} < +85\text{ °C}$	–	± 0.45	–	dB
ISO _r	reverse isolation		18	20	–	dB
ISO _i	isolation between inputs		21	23	–	dB
s_{11}	input reflection coefficient	50 Ω source	–	–8.5	–	dB
s_{22}	output reflection coefficient	50 Ω load	–	–22	–	dB

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APPLICATION AND TEST INFORMATION

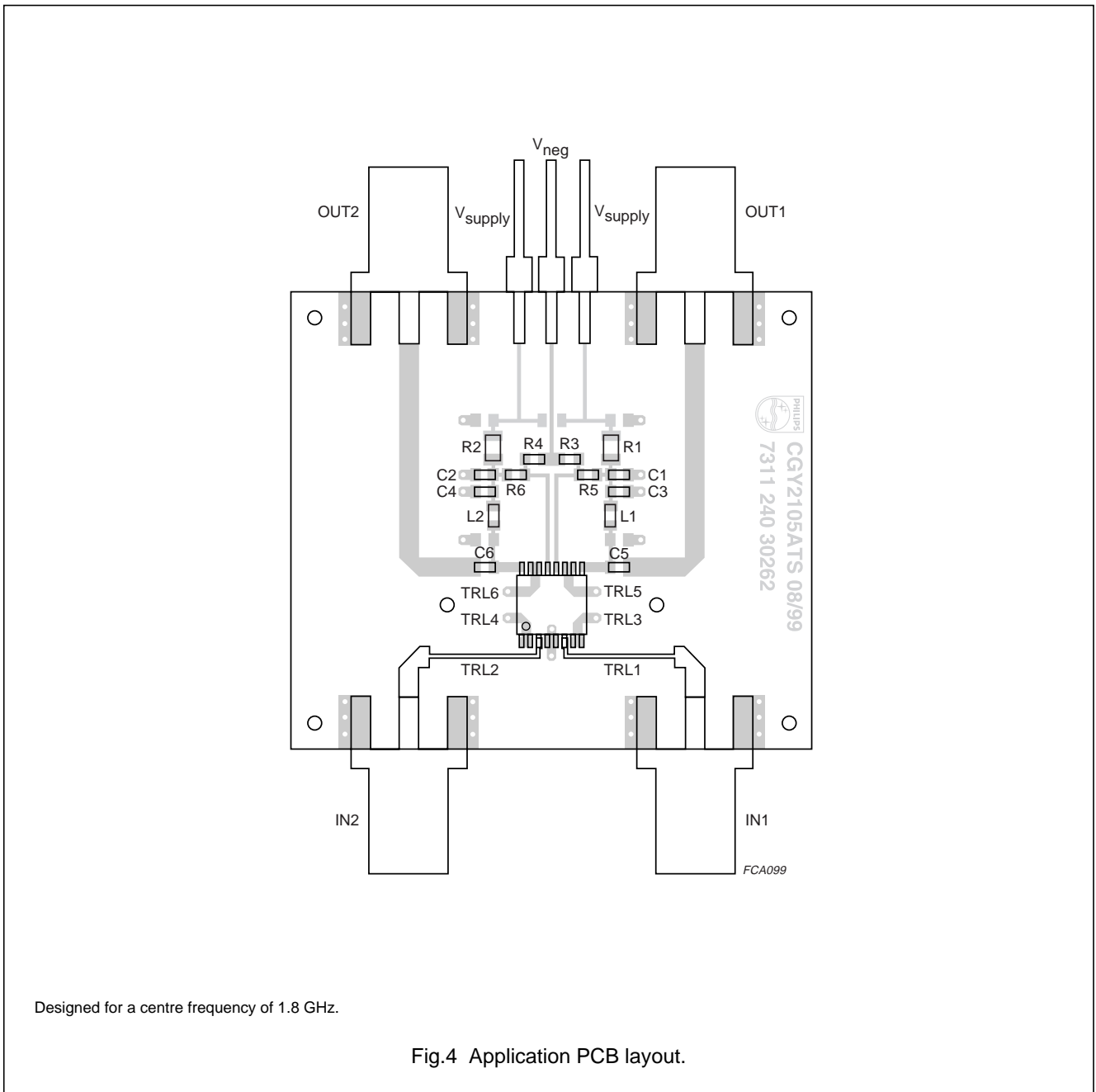


The demonstration board has been optimized for a centre frequency of 1.8 GHz.
 The MMIC s-parameters (typical values) in a range from 0.1 to 6 GHz are available on request.

Fig.3 Application diagram.

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Table 1 List of components; see Figs 3 and 4

COMPONENT	DESCRIPTION	VALUE	REFERENCE
C1, C2	decoupling capacitor	1 nF	Philips; NPO, 0603
C3, C4	decoupling capacitor	47 pF	Philips; NPO, 0603
C5, C6	decoupling capacitor	47 pF	Philips; NPO, 0603
R1, R2	drain biasing resistor	39 Ω	Philips; XR7, 0805
R3, R4	gate biasing resistor	15 k Ω	Philips; 0603
R5, R6	gate biasing resistor	10 k Ω	Philips; 0603
L1, L2	drain biasing inductor	18 nH	Coilcraft; 0603

Table 2 Transmission lines; see Figs 3 and 4

COMPONENT	Z_0	LENGTH IN λ	LENGTH IN mm ⁽¹⁾	WIDTH IN mm ⁽¹⁾
TRL1, TRL2	100 Ω	0.08 λ at 1800 MHz	10 mm	0.25 mm
TRL3, TRL4	100 Ω	0.08 λ at 1800 MHz	4 mm	0.80 mm
TRL5, TRL6	100 Ω	0.08 λ at 1800 MHz	3.4 mm	0.80 mm

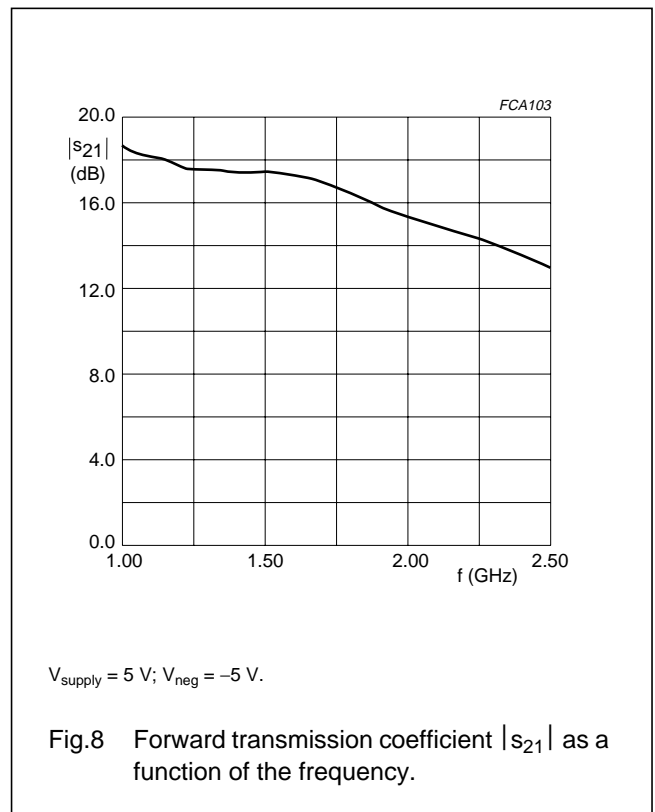
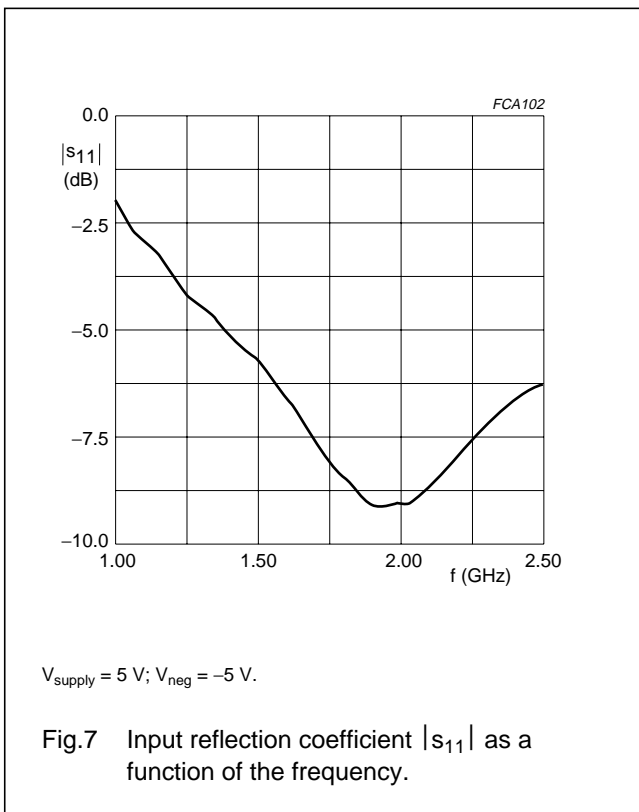
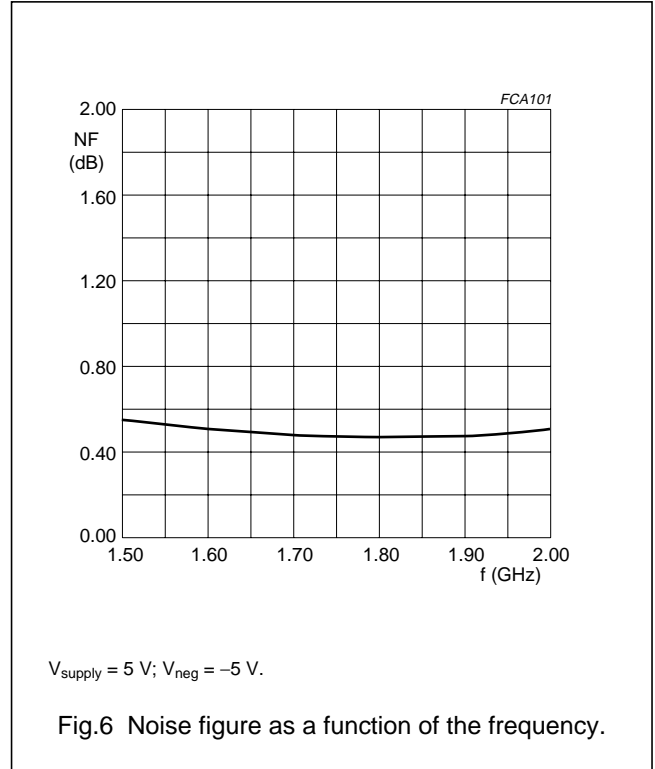
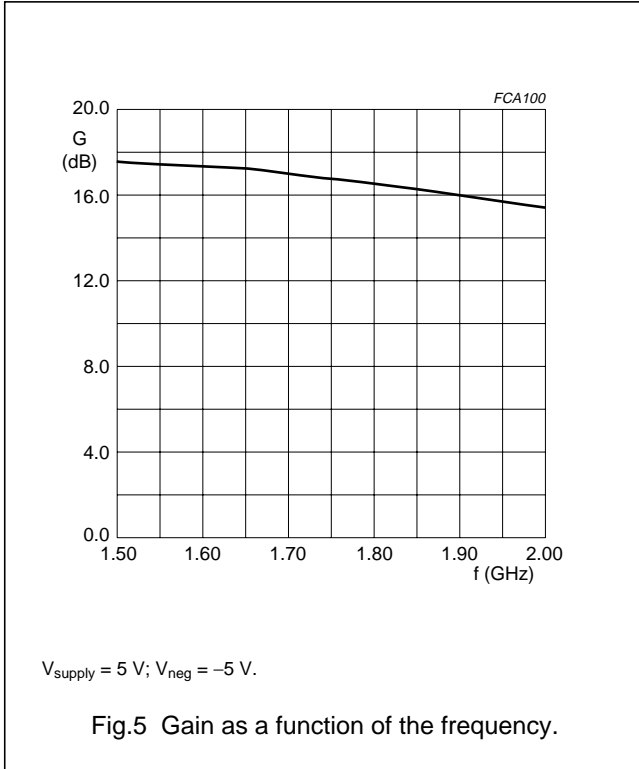
Note

1. Transmission line lengths and widths in mm are valid for a double sided PCB; thickness of 0.8 mm in FR4 material ($\epsilon = 4.7$).

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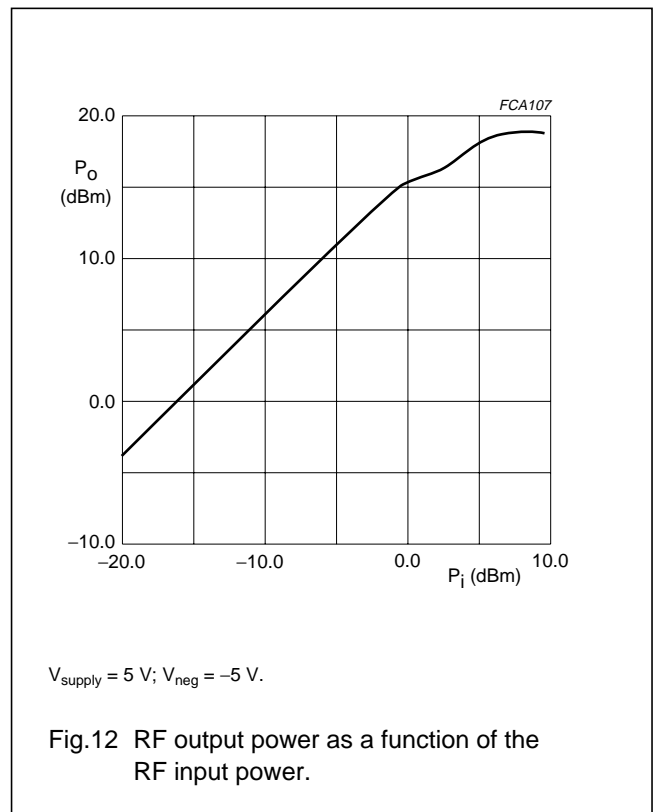
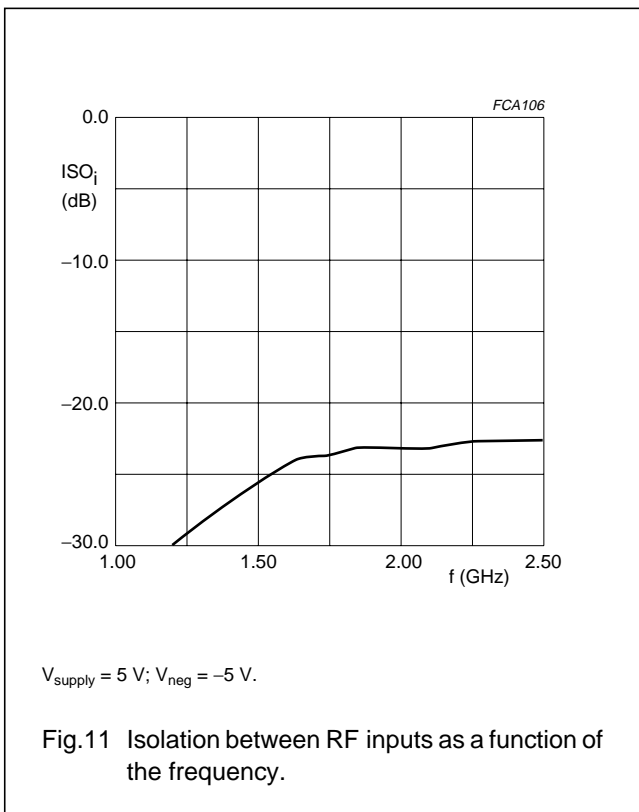
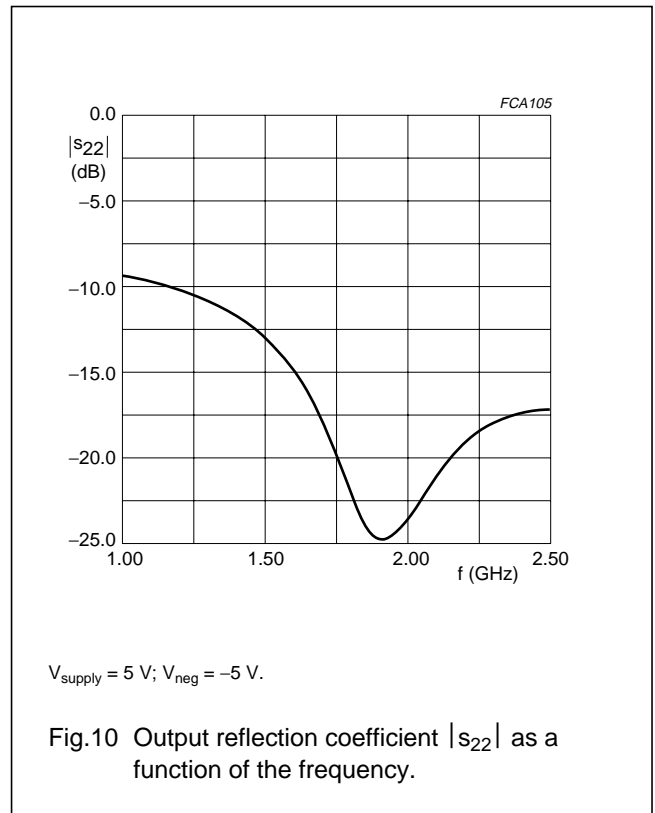
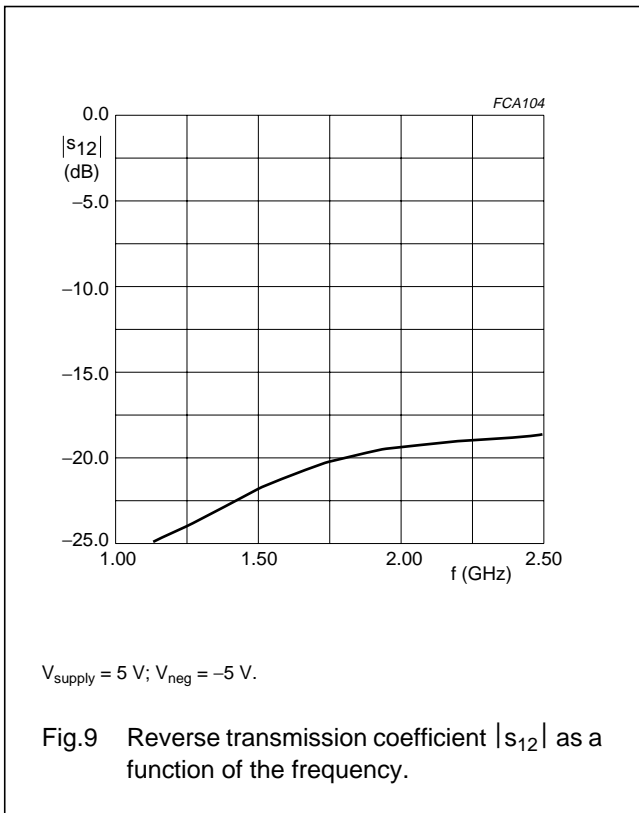
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Measured performance



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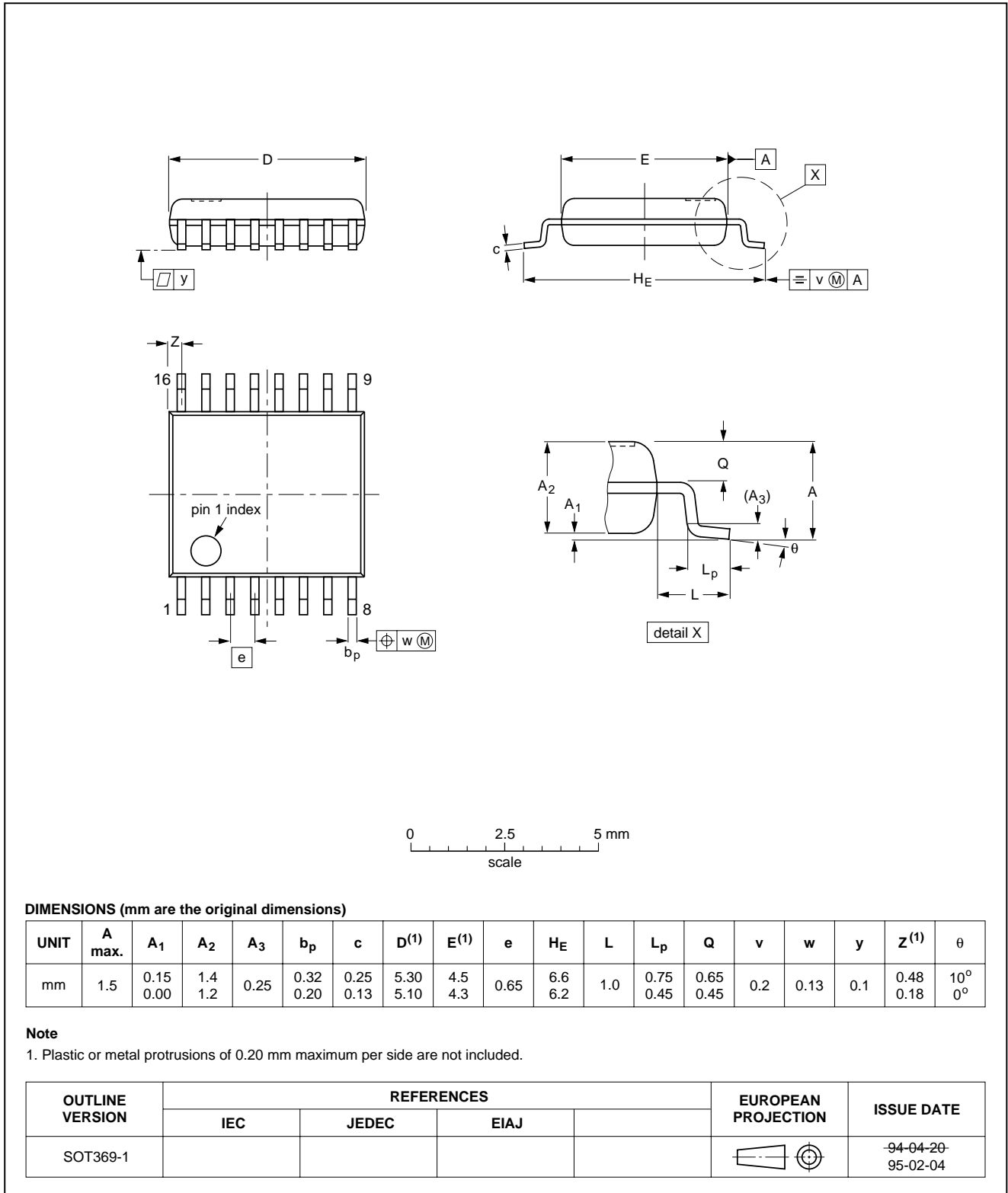
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PACKAGE OUTLINE

SSOP16: plastic shrink small outline package; 16 leads; body width 4.4 mm

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DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.5	0.15 0.00	1.4 1.2	0.25	0.32 0.20	0.25 0.13	5.30 5.10	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10° 0°

Note
1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT369-1						94-04-20 95-02-04

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SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW ⁽¹⁾
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable ⁽²⁾	suitable
PLCC ⁽³⁾ , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended ⁽³⁾⁽⁴⁾	suitable
SSOP, TSSOP, VSO	not recommended ⁽⁵⁾	suitable

Notes

- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods".
- These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
- If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 3 Figtree Drive, HOMEBUSH, NSW 2140,
Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 68 9211, Fax. +359 2 68 9102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Sydhavnsgade 23, 1780 COPENHAGEN V,
Tel. +45 33 29 3333, Fax. +45 33 29 3905

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615 800, Fax. +358 9 6158 0920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Via Casati, 23 - 20052 MONZA (MI),
Tel. +39 039 203 6838, Fax +39 039 203 6800

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Al.Jerozolimskie 195 B, 02-222 WARSAW,
Tel. +48 22 5710 000, Fax. +48 22 5710 001

Portugal: see Spain

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Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
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Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

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South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
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Tel. +27 11 471 5401, Fax. +27 11 471 5398

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2886, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye,
ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
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Uruguay: see South America

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Printed in The Netherlands

465008/01/pp16

Date of release: 1999 Dec 23

Document order number: 9397 750 06527

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