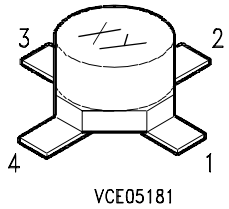
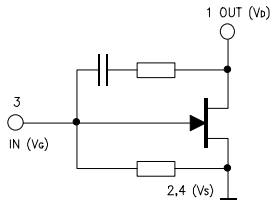
D a t a s h e e t

- ***** Single-stage monolithic microwave IC (MMIC-amplifier)
- * Application range: 100 MHz to 3 GHz
- ***** Gain: 9 dB typ. @ 1.6 GHz
- ***** Low noise figure: 2.7 dB typ. @ 1.6 GHz
- ***** Bandwidth: 3 GHz typ. @ -3 dB, VSWR < 2 : 1
- ***** Operating voltage range: 3 to 5.5 V
- * Individual current control with neg. gate bias
- * Hermetically sealed ceramic stripline package Cerec-X



ESD: **E**lectro**s**tatic **d**ischarge sensitive device, observe handling precautions!

Type	Marking	Ordering code (tape and reel)	Circuit Diagram (Pin Configuration)	Package 1)
CGY 40	40	Q68000-A4444		Cerec-X

Maximum ratings	**Symbol**	**Value**	**Unit**
Drain-voltage	V_D	5.5	V
Current control gate voltage	V_G	-3 ... 0	V
Drain-gate voltage	V_{DG}	8.5	V
Input power	P_{IN}	16	dBm
Channel temperature	T_{Ch}	150	°C
Storage temperature range	T_{stg}	-55...+150	°C
Total power dissipation (TS ≤ 82°C) 2)	P_{tot}	440	mW
Thermal resistance			
Channel-soldering point 2)	R_{thChS}	155	K/W

Note: Exceeding any of the max. ratings may cause permanent damage to the device. Appropriate handling is required to protect the electrostatic sensitive MMIC against degradation due to excess voltage or current spikes. Proper ground connection of leads 2 and 4 (with min. inductance) is required to achieve the guaranteed RF performance, stable operating conditions and adequate cooling.

1) Dimensions see chapter Package Outlines
2) Ts is measured on the source lead at the soldering point to the PCB.

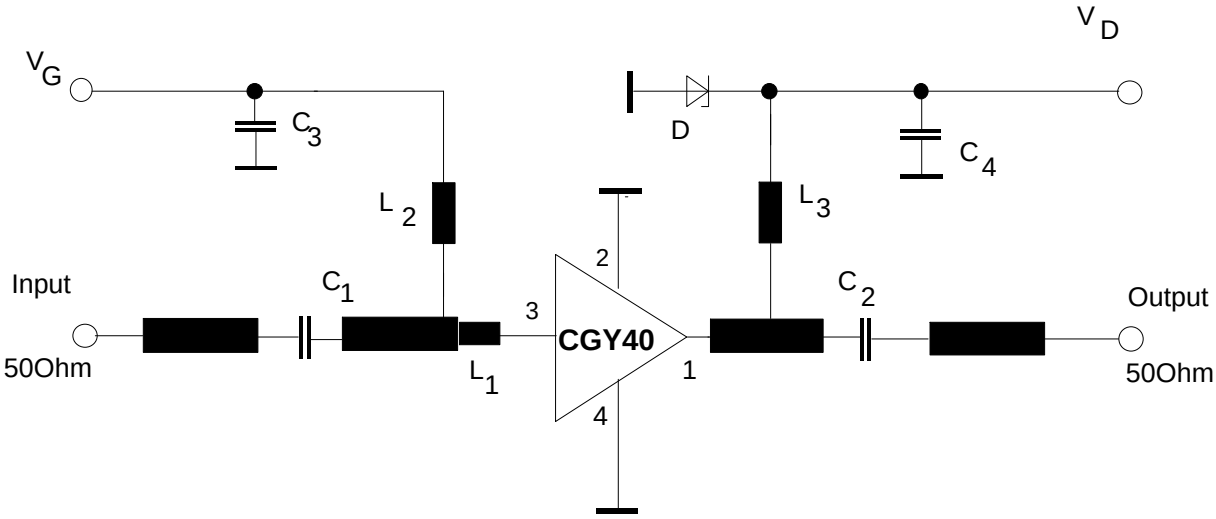
Electrical Characteristics

T_A = 25 °C, V_G = 0 V, V_D = 4.5 V, $R_S = R_L$ = 50 Ω, unless otherwise specified

(for application circuit see next page)

Characteristics	Symbol	min	typ	max	Unit
Drain current	I_D	-	60	80	mA
Power gain	G				dB
f = 200 MHz		9.5	10.5	12	
f = 1800 MHz		8	9	10.5	
Gain flatness	ΔG				dB
f = 200 to 1000 MHz		-	0.4	-	
f = 800 to 1800 MHz		-	1.1	2	
Noise figure	F				dB
f = 200 to 1000 MHz		-	2.5	-	
f = 800 to 1800 MHz		-	2.8	4.0	
Input return loss	RL_{IN}				dB
f = 200 to 1000 MHz		-	13	-	
f = 800 to 1800 MHz		-	12	9.5	
Output return loss	RL_{OUT}				dB
f = 200 to 1000 MHz		-	12	-	
f = 800 to 1800 MHz		-	12	9.5	
Third order intercept point	$IP3$				dBm
Two tone intermodulation test					
f_1 = 806 MHz, f_2 = 810 MHz		31	32	-	
P_0 = 10 dBm (both carriers)					
1dB gain compression	$P_{1\,dB}$				dBm
f = 200 to 1800 MHz		-	18	-	
Gain control dynamic range	ΔG				dB
f = 200 to 1000 MHz		-	30	-	
f = 800 to 1800 MHz		-	20	-	

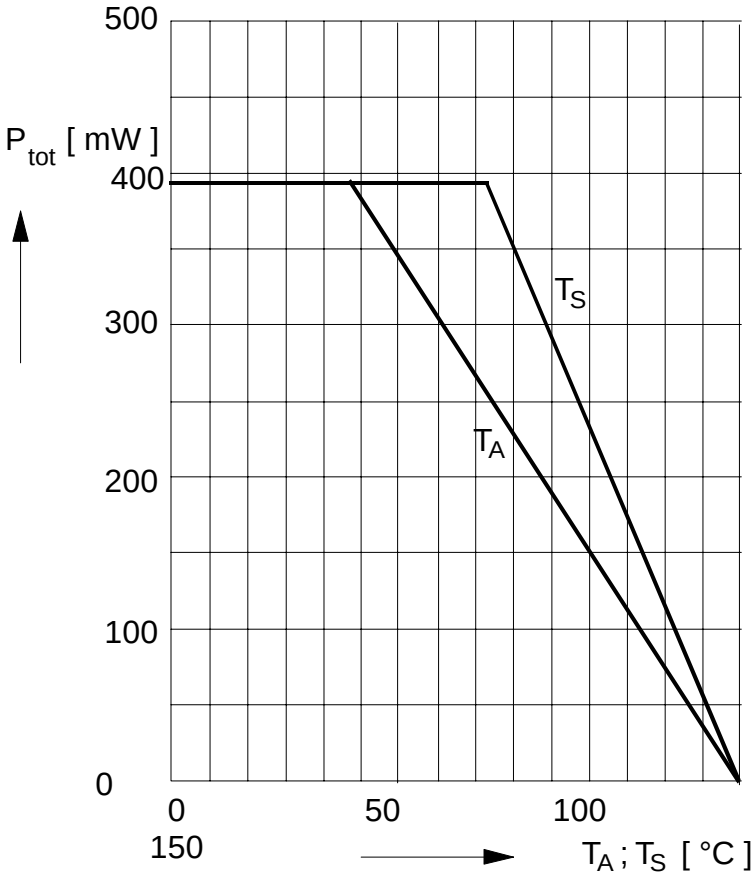
Application Circuit (f = 800 to 1800 MHz)



Legend of components

C_1 , C_2 C_3 , C_4	Chip capacitors 100 pF Chip capacitors 1 nF
L_1	For optimized input matching - discrete inductor: approx. 3nH, or - printed microstripline inductor: Z approx. 100 Ω, l_e approx. 5 mm
L_2, L_3	- discrete inductor: approx. 40 nH, as e.g. 5 turns 0.25 mm copper wire on nylon rod with M3-thread, or - printed microstripline inductor
D	Z diode 5.6 V (type BZW 22 C5 V 6)

Total Power Dissipation $P_{tot} = f(T_s;T_A)$



Typical Common Source S-Parameters

V_G = 0V V_D = 4.5 V Z_0 = 50 Ω

f	S11		S21		S12		S22	
GHz	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
0.2	0.20	-47	3.32	165	0.14	2	0.09	-150
0.4	0.16	-49	3.24	158	0.14	-2	0.09	148
0.6	0.15	-60	3.17	149	0.14	-6	0.11	117
0.8	0.16	-72	3.09	141	0.14	-8	0.13	97
1.0	0.15	-87	3.02	132	0.13	-10	0.16	84
1.2	0.14	-105	2.95	124	0.13	-12	0.19	76
1.4	0.15	-124	2.88	116	0.13	-13	0.21	68
1.6	0.15	-139	2.82	107	0.12	-14	0.22	60
1.8	0.16	-151	2.75	100	0.12	-15	0.24	54
2.0	0.17	-166	2.69	93	0.11	-15	0.25	48
2.2	0.18	-176	2.62	86	0.11	-15	0.26	41
2.4	0.21	173	2.56	80	0.11	-14	0.27	37
2.6	0.21	163	2.48	73	0.11	-14	0.27	32
2.8	0.23	154	2.40	67	0.11	-14	0.27	28
3.0	0.24	146	2.32	61	0.11	-13	0.27	24
3.2	0.26	140	2.24	55	0.11	-12	0.27	20
3.4	0.29	136	2.15	51	0.11	-14	0.26	18
3.6	0.31	127	2.05	44	0.11	-12	0.25	17
3.8	0.32	123	1.94	39	0.11	-11	0.24	14
4.0	0.34	118	1.83	34	0.11	-11	0.23	10
4.2	0.36	115	1.80	29	0.11	-11	0.22	6