CH9294 Dual Clock Generator

Features

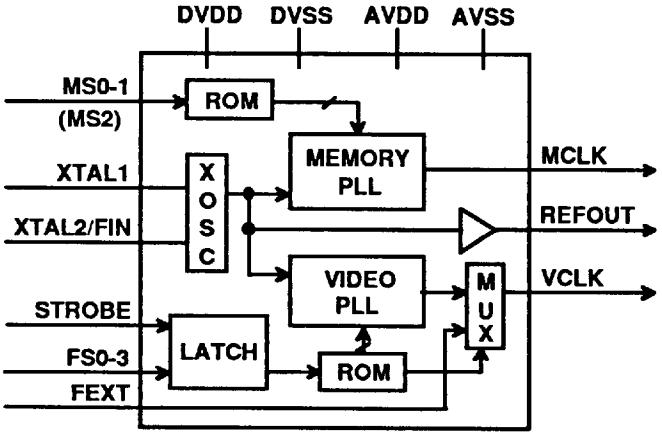
- 16 video clock frequencies, 4 memory clock frequencies (8 memory clock frequencies available on selected versions), and a buffered reference output
- Provision for external frequency input
- No external loop filter components required
- Supports output frequencies up to 135 MHz
- Optional power down mode that draws less than 1µA if activated
- Only two external components: one 14.318 MHz crystal and one decoupling capacitor
- No need for external VDD dropping resistor
- Supports graphics standards such as VGA, SuperVGA, XGA, and 8514A
- Drop-in replacement for ICS2494 or AV9194
- High performance, low power CMOS technology
- Available in 20-pin plastic DIP or SOIC
- Proprietary VCO design for low phase jitter
- 5V supply

Description

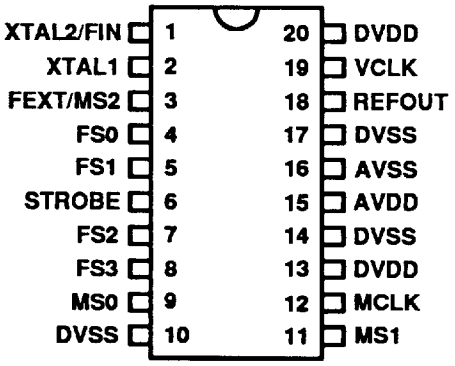
The Chrontel CH9294 is a dual phase-locked loop frequency synthesizer designed for low power and high performance applications, such as graphics systems based on the VGA, SuperVGA, XGA, and 8514A formats. Internal loop filter elements are employed to minimize external part-count. It can also be used in any application that requires multiple clocks, such as PC motherboards, disk drives, CD-ROM systems, FAX-modems, etc.

To support the latest generation of high performance graphics controllers, CH9294 provides separate memory clock (MCLK) and video clock (VCLK) outputs. CH9294 also buffers the 14.318 MHz reference frequency in addition to video and memory clock outputs. Other input frequencies can be used to obtain non-standard output frequencies.

The STROBE pin should be tied high or left open for direct FS0 through FS3 selection of video clock frequencies. Frequency select inputs are latched on the falling edge of STROBE.



BLOCK DIAGRAM



PINOUT DIAGRAM

CH9294 Frequency Table (Versions E and G shown below)

Video Clock

FS				VCLK (MHz)	
3	2	1	0	Version E	Version G
0	0	0	0	50.35	25.18
0	0	0	1	56.65	28.32
0	0	1	0	65.0	40.0
0	0	1	1	72.0	72.0
0	1	0	0	80.0	50.0
0	1	0	1	89.8	77.0
0	1	1	0	63.0	36.0
0	1	1	1	75.0	44.9
1	0	0	0	25.18	130.0
1	0	0	1	28.32	120.0
1	0	1	0	31.5	80.0
1	0	1	1	36.0	31.5
1	1	0	0	40.0	110.0
1	1	0	1	44.9	65.0
1	1	1	0	50.0	75.0
1	1	1	1	65.0 (default)	94.5 (default)

Memory Clock

MS			MCLK (MHz)	
2	1	0	Version E	Version G
0	0	0	40.0	55.0
0	0	1	41.61	65.0
0	1	0	44.74	70.0
0	1	1	50.0 (default)	80.0
1	0	0	52.5	45.0
1	0	1	55.0	40.0
1	1	0	57.5	60.0
1	1	1	60.0	50.0 (default)

Consult Chrontel for other standard frequency table versions and exact output frequencies.
Custom patterns are also available. Please contact Chrontel for details.

Pin Description

Pin	Type	Symbol	Description
1	Out/In	XTAL2 / FIN	Crystal output/external FREF input
2	In	XTAL1	Crystal input
3	In	FEXT / MS2	External frequency input (internal pull-down) or memory clock select 2
4, 5, 7, 8	In	FS0, FS1, FS2, FS3	Video clock select (internal pull-up)
6	In	STROBE	FS0 through FS3 strobe input (internal pull-up)
9, 11	In	MS0, MS1	Memory clock select (internal pull-up)
10, 14, 17	Power	DVSS	Digital ground
12	Out	MCLK	Memory clock output
13, 20	Power	DVDD	Digital 5V supply
15	Power	AVDD	Analog 5V supply
16	Power	AVSS	Analog ground
18	Out	REFOUT	Buffered reference frequency output
19	Out	VCLK	Video clock output

Absolute Maximum Ratings

Symbol	Description	Value	Unit
V_{DD}	Power supply voltage with respect to Vss	−0.5 to +7.0	V
V_{IN}	Input voltage on any pins with respect to Vss	−0.5 to V_{DD}+0.5	V
T_{STOR}	Storage temperature	−55 to +150	°C

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated under parametric values of the DC or AC Specifications below is not recommended or guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

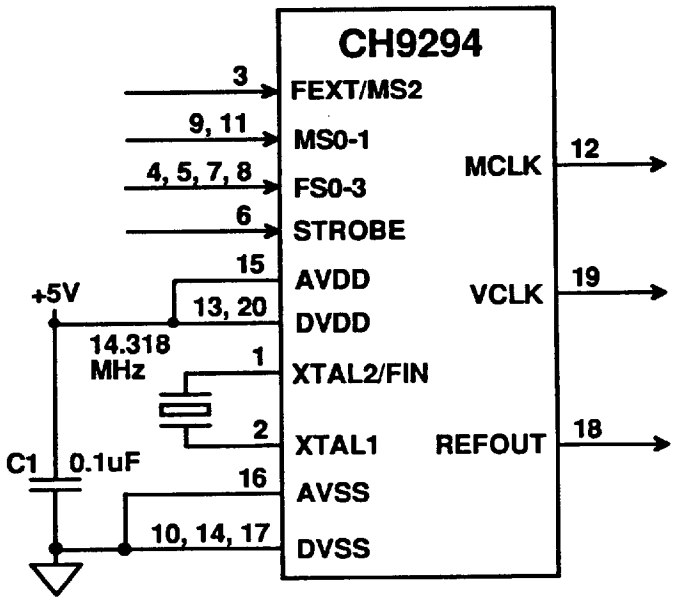
DC Specifications (T_A = 0°C – 70°C, V_{DD} = 5V ±5%)

Symbol	Description	Test Condition @T_A=25°C	Min	Typ	Max	Unit
V_{OH}	Output high voltage	V_{DD}=4.75V, I_{OH}=4mA	2.4			V
V_{OL}	Output low voltage	V_{DD}=4.75V, I_{OL}=8mA			0.4	V
V_{IH}	Input high voltage		2.0			V
V_{IL}	Input low voltage				0.8	V
I_{PU}	Input pull-up current			5	20	µA
I_L	Input leakage current		−10		10	µA
I_{DD}	Operating current	V_{CLK}=50MHz, M_{CLK}=50MHz, V_{DD}=5.0V		45		mA

AC Specifications (T_A = 0°C – 70°C, V_{DD} = 5V ±5%)

Symbol	Description	Test Condition @T_A=25°C	Min	Typ	Max	Unit
F_{IN}	Crystal/F_{REF} input			14.318		MHz
T_{SU}	Setup time, data to strobe		25			ns
T_{HOLD}	Hold time, strobe to data		25			ns
T_{STROBE}	Strobe pulse width		50			ns
T_{DELAY}	Prop. delay for F_{EXT} to V_{CLK}				50	ns
V_{CLK}	Video clock frequency		8		135	MHz*
M_{CLK}	Memory clock frequency		8		135	MHz*
T_R, T_F	Output clock rise/fall time	C_L=25pF, V_{OL} – V_{OH}		2		ns
T_{DC}	Output clock duty cycle	@V_{DD}/2, V_{DD}=5.0V, C_L=15pF	40	50	60	%

Note: * Output levels are guaranteed up to 90 MHz. Please consult Chrontel for suggested circuit implementations for frequencies higher than 90 MHz.



CH9294 APPLICATION SCHEMATIC

Note:
C1 should be placed in close proximity to the power pins

ORDERING INFORMATION	
Part Number	Package Type
CH9294x-N	300 mil PDIP
CH9294x-S	300 mil SOIC
Note: x = Frequency table version	

For the location of the sales office nearest you, contact:

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