Consumer Infrared Communications Controller

FEATURES

- Multi-Protocol Serial Communications Controller
- Full IrDA v1.0 Implementation: 2.4 kbps to 115.2 kbps
- Consumer Infrared Remote Control Interface
- SHARP Amplitude Shift Keyed Infrared (ASK IR) Interface
- Direct Rx/Tx Infrared Diode Control (Raw) and General Purpose Data Pins
- Programmable High-Speed Synchronous Communications Engine (SCE) with a 32-Byte FIFO and Programmable Threshold

- Programmable DMA Refresh Counter
- High-Speed NS16C550A-Compatible Universal Asynchronous Receiver/ Transmitter Interface (ACE UART) with 16-Byte Send and Receive FIFOs
- ISA Single-Byte and Burst-Mode DMA and Interrupt-Driven Programmed I/O with Zero Wait State and String Move Timing
- Automatic Transceiver Control
- Transmit Pulse Width Limiter
- SCE Transmit Delay Timer
- IR Media Busy Indicator

GENERAL DESCRIPTION

This document describes the Consumer Infrared Communications Controller (CIrCC) function, which is common to a number of SMSC products. The CIrCC consists of two main architectural blocks: the ACE 16C550A UART and a Synchronous Communications Engine (SCE) (Figure 2). Each Block is supported by its own unique register set.
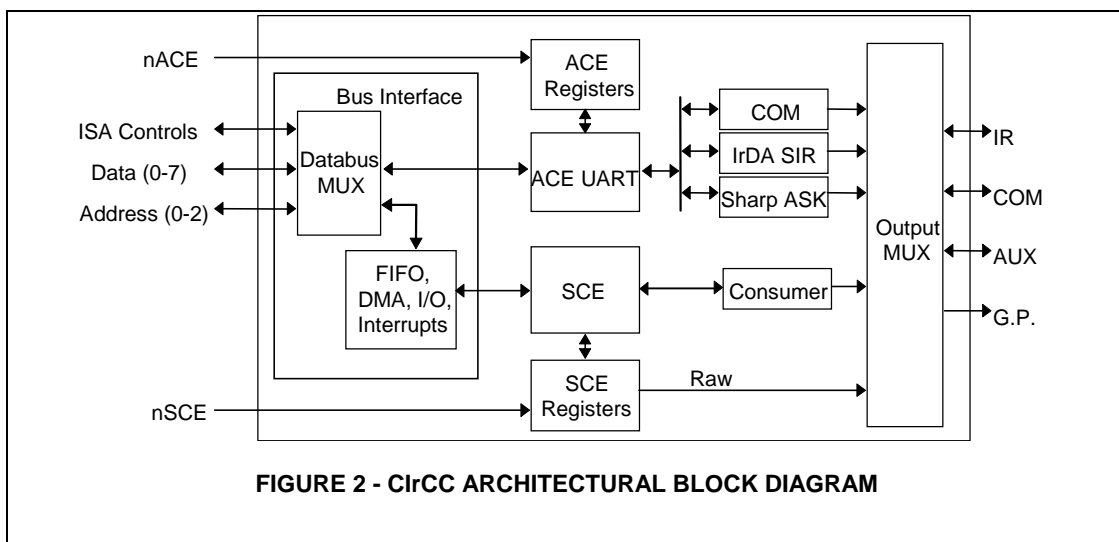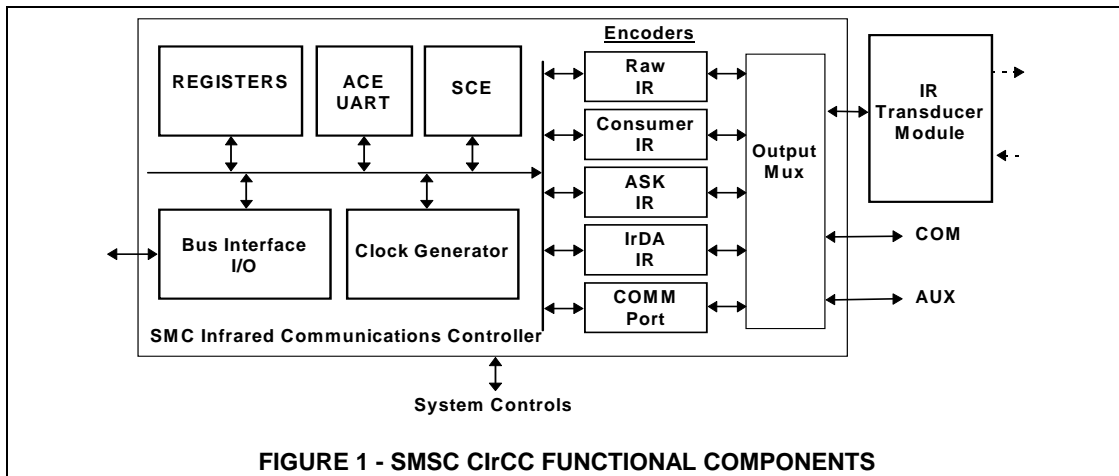
The CIrCC UART-driven IrDA SIR and SHARP ASK modes are backward-compatible with early SMSC Super I/O and Ultra I/O infrared implementations. The CIrCC SCE supports IrDA version 1.0 and consumer IR modes. All of the SCE modes use DMA. The CIrCC offers flexible signal routing and programmable output control through the Raw mode interface, General Purpose Data pins and Output Multiplexer. Hardware decoding of the NEC PPM Consumer IR Remote Control format is implemented in the CIrCC. The CIrCC provides a PME output signal that is used to indicate the occurrence of a valid CIR Wake-up event. Chip-level address decoding is required to access the CIrCC register sets.

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INTERFACE DESCRIPTION

The Interface Description lists the signals that are required to place the CIrCC in a larger chip-level context.

There are four groups of signals in this section: PORT signals, HOST BUS controls, SYSTEM controls, and CHIP-LEVEL CONFIGURATION controls.

Ports

The three Ports (IR, COM, and AUX) provide external access for serial data and controls. The active CIrCC encoder is routed through the Output Multiplexer to the IR, COM, or AUX port.

Table 1 - IR Port Signals

NAME	SIZE (BITS)	TYPE	DESCRIPTION
IRRx	1	Input	Infrared Receive Data
IRTx	1	Output	Infrared Transmit Data

Table 2 - COM Port Signals

NAME	SIZE (BITS)	TYPE	DESCRIPTION
CRx	1	Input	COM Receive Data
CTx	1	Output	COM Transmit Data
nRTS	1	Output	Request to Send
nDTR	1	Output	Data Terminal Ready
nCTS	1	Input	Clear To Send
nDSR	1	Input	Data Set Ready
nDCD	1	Input	Data Carrier Detect
nRI	1	Input	Ring Indicator

Table 3 - AUX Port Signals
(e.g., can be used for high-current drivers for Consumer IR)

NAME	SIZE (BITS)	TYPE	DESCRIPTION
ARx	1	Input	Aux. Receive Data
ATx	1	Output	Aux. Transmit Data

Table 4 - HOST Signals

NAME	SIZE (BITS)	TYPE	DESCRIPTION
D0-D7	8	Bi-directional	Host Data Bus
A0-A2	3	Input	CIrCC Register Address Bus
nIOR	1	Input	ISA I/O Read
nIOW	1	Input	ISA I/O Write
AEN	1	Input	ISA Address Enable
DRQ	1	Output	DMA Request
nDACK	1	Input	ISA DMA Acknowledge
TC	1	Input	ISA DMA Terminal Count
IRQ	1	Output	Interrupt Request
IOCHRDY	1	Output	ISA I/O Channel Ready
nSRDY	1	Output	ISA Synchronous Ready (Zero Wait State)

Table 5 - SYSTEM Signals

NAME	SIZE (BITS)	TYPE	DESCRIPTION
CLK	1	Input	System Clock
RESET	1	Input	CIrCC System Reset
CIR_PME	1	Output	CIR PME Wake Event
Power Down	1	Input	Low Power Control
DMAEN	1	Output	DRQ Tristate Control
IRQEN	1	Output	IRQ Tristate Control
nACE	1	Input	ACE 550 Register Bank Select
nSCE	1	Input	SCE Register Bank Select
VCC		Power	System Supply
GND		Power	System Ground

DMAEN

DMAEN is used by the chip-level interface to tristate the CIrCC DRQ output when the DMA Enable bit is inactive. The DMA Enable bit is located in SCE Configuration Register B, bit 0.

IRQEN

IRQEN is used by the chip-level interface to tristate the CIrCC IRQ output when the OUT2 bit is inactive. The OUT2 bit is located in 16C550A MODEM Control Register.

Power Down

The Power Down pin is used by the chip-level interface to put the SCE into low power mode. Note: Power Down only forces the SCE into low power mode. The ACE power down function is not a part of this specification.

CIR_PME

CIR_PME is used by a chip-level interface to indicate that a valid NEC control frame has been received and a PME Wake event can be issued. (See the PME WAKE bit in the Consumer IR Control Register in SCE Register Block Two).

CHIP-LEVEL CONFIGURATION CONTROLS

The following signals come from chip-level configuration registers. There are two types of Chip-Level Configuration Controls: CIrCC-Specific controls, and Legacy Controls. Both types have equivalent controls in either the CIrCC ACE or SCE Registers.

The CIrCC-Specific controls have been newly added primarily to support the CIrCC block. Provisions have been made in new chip-level configuration contexts to accommodate these signals.

The Legacy controls already exist in other contexts. Provisions have been made in legacy devices to accommodate these controls from either the Chip-Level Configuration Registers or the CIrCC Registers; i.e., the last updated value from either source determines the current control state and is visible in both registers.

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Table 6 - CIrCC-Specific Chip-Level Controls

NAME	SIZE (BITS)	TYPE	DESCRIPTION
DMA Channel	4	Input	ISA DMA Channel Number
IRQ Level	4	Input	ISA Interrupt Level
Software Select A	8	Input	Software Programmable Register A
Software Select B	8	Input	Software Programmable Register B

DMA Channel

4 bit bus from a chip-level configuration register, used to identify the current CIrCC DMA channel number. The value appears in the upper nibble of CIrCC Register Block Three, Address Four.

IRQ Level

4 bit bus from a chip-level configuration register, used to identify the current CIrCC IRQ level. The value appears in the lower nibble of CIrCC Register Block Three, Address Four.

Software Select A/B

The 8 bit Software Select A and Software Select B inputs come from software-only programmable chip-level configuration controls. The values on these buses appear in CIrCC Register Block Three, Addresses Five and Six.

Table 7 - Legacy Chip-Level Controls

NAME	SIZE (BITS)	TYPE	DESCRIPTION
Tx Polarity	1	Input	Output Mux. Transmit Polarity
Rx Polarity	1	Input	Output Mux. Receive Polarity
Half Duplex	1	Input	16C550A UART Half Duplex Control
IR Half Duplex Timeout	8	Input	IR Transceiver Turnaround Time
IR Mode	3	Input	IR Mode Register Bits
IR Location	2	Input	IR Option Register Location Bits

Tx Polarity

Typically part of a 16C550A Serial Port Option Register. The value also appears in CIrCC Register Block One, Address Zero.

Rx Polarity

Typically part of a 16C550A Serial Port Option Register. The value also appears in CIrCC Register Block One, Address Zero.

Half Duplex

Typically part of a 16C550A Serial Port Option Register. The value also appears in CIrCC Register Block One, Address Zero.

IR Half Duplex Timeout

Typically part of a 16C550A Serial Port 2 Configuration Register. The value also appears in CIrCC Register Block One, Address Zero.

IR Mode

Typically part of a 16C550A Serial Port Option Register. These values are also part of the CIrCC Block Control bits 3-5, Register Block One, Address Zero.

IR Location

Typically part of a 16C550A Serial Port IR Option Register. These values are the CIrCC Output Mux bits, Register Block One, Address One. Note: These legacy controls are uniformly updated in the CIrCC and the Top-Level Device Configuration Registers only when either set of registers is explicitly written using IOW or following a device-level POR. CIrCC software resets will not affect the legacy bits.

RAW IR

In Raw mode the state of the IR emitter and detector can be directly accessed through the host interface (Figure 3).

The IR emitter tracks the Raw Tx Control bit in SCE Line Control Register A. For example, depending on the state of the Tx Polarity control a logic '1' may turn the LED on and a logic '0' may turn the LED off. Care must be taken in software to ensure that the LED is not on continuously.

The Raw Rx Control bit in SCE Line Control Register A represents the state of the PIN diode. For example, depending on the state of the Rx Polarity control a logic '1' may mean no IR is detected, a logic '0' may mean IR is being detected. If an IR carrier is present, the Raw Rx Control bit will oscillate at the carrier frequency.

If enabled, a Raw Mode Interrupt will occur when the Raw Rx Control bit transitions to the active state, depending on the state of the Rx Polarity control. Raw Mode is enabled with the Block Control Bits in SCE Configuration Register A (see page 30).

FIGURE 3 - RAW IR BLOCK DIAGRAM
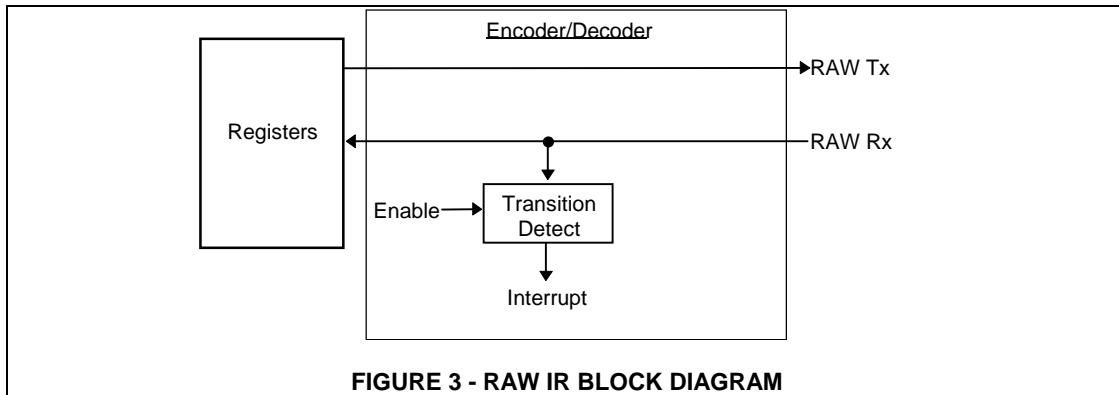
CONSUMER IR (REMOTE CONTROL)

INTRODUCTION

The CIrCC Consumer IR Remote Control block is a general-purpose programmable Synchronous Amplitude Shift Keyed serial communications interface that includes a Carrier Frequency Divider, a Programmable Receive Carrier Range Sensitivity Register, Receive and Transmit Modulators and an NEC PPM Frame Format Decoder.

The Consumer IR transmit block transfers data LSB first between the SCE and Output Multiplexer as a fixed bit-cell serial NRZ data stream. The components of this block can also modulate serial data at programmable data rates and carrier frequencies.

Variable length encoding and message framing is handled during transmit by system software. Receive message framing may be handled by either hardware or software. The high degree of control afforded to the system software allows for the support of many encoding methods; including PPM, PWM and RC-5 Remote Control formats.

Register controls for the Consumer IR hardware can be found in Register Block Two. They are the Consumer IR Control Register, the Consumer IR Carrier Rate Register, the Consumer IR Bit Rate Register, the Custom Code Register, the Custom Code' Register, and the Data Code Register.

NEC HARDWARE FRAME DECODING

General

The CIrCC implements hardware-level decoding for the NEC Consumer IR Remote Control format. The hardware decoder may be used to generate a wake-up event or to send parts of the received message frame to the FIFO. The No Care Custom Code (NCCC), No Care Data Code (NCDC), PME Wake and Frame bits of the Consumer IR Control register configure the hardware decoder.

NEC Consumer IR Format

The NEC Consumer IR Remote Control format specifies a 38kHz carrier, 13ms of sync framing, and 32 bits of pulse-position modulated (PPM) message data. The message data includes an 8 bit Custom Code field, an 8 bit Custom Code' field, an 8 bit Data Code field, and an 8 bit Data Code' field. A single frame of the NEC PPM Consumer Remote Control output is shown in Figure 5.

The Custom Code fields in this protocol uniquely address message frames for specific devices. The Custom Code fields can be used as a 16 bit address or as an 8 bit address followed by the bit-wise complement of the Custom Code field Custom Code'. The Data Code field is an 8 bit command code, Data Code' is the bit-wise complement of Data Code.

Note: The CIrCC hardware can decode NEC protocol framing (sync pulse, 32 bit PPM message data) at any carrier frequency or data rate, depending on the programmed Carrier Frequency Divider (CFD) and Bit Rate Divider (BRD).
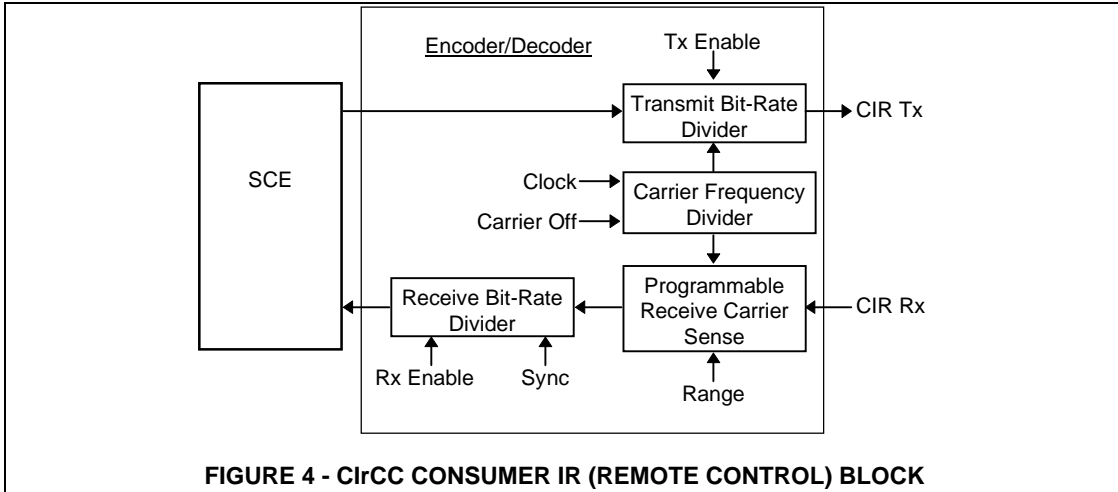
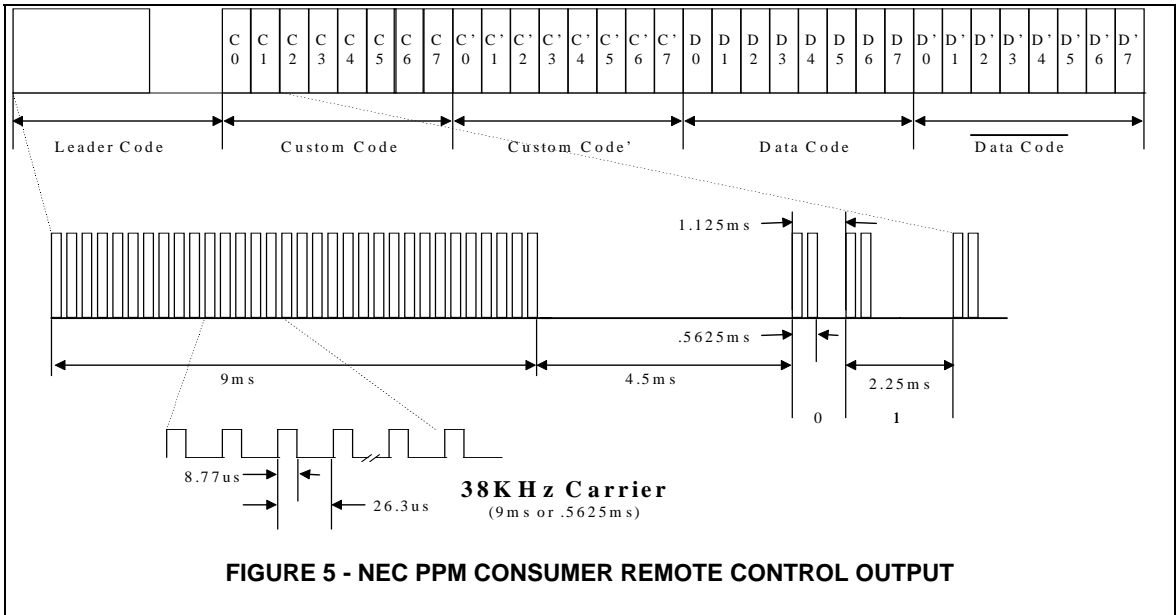**FIGURE 4 - ClrCC CONSUMER IR (REMOTE CONTROL) BLOCK**

FIGURE 5 - NEC PPM CONSUMER REMOTE CONTROL OUTPUT

Carrier Frequency Divider

The Carrier Frequency Divider register is used to program the ASK carrier frequency for the transmit modulator and receive detector (Figure 6). The divider is eight bits wide.

The input clock to the Carrier Frequency Divider is 1.6MHz (48MHz ÷ 30). The relationship between the divider value (CFD) and the carrier frequency (Fc) is as follows:

$$CFD = (1.6MHz/Fc) - 1$$

For example, program the Carrier Frequency Divider register with 41 ('29'Hex) for a 38kHz carrier like for the NEC remote control frame format: Fc = 38.095kHz. This is ~.25% accuracy. Table 8 contains representative CFD vs. Carrier Frequency relationships.

The Carrier Frequency range is 1.6MHz to 6.25kHz.

The carrier frequency encoder/decoder can be defeated using the Carrier Off bit. When Carrier Off is one, the transmitter outputs a non-modulated SCE serial NRZ data stream at the programmed bit rate; the receiver does not attempt to demodulate a carrier from the incoming serial data stream.

Table 8 - Representative Carrier Frequencies

CFD	Fc (kHz)	CFD	Fc (kHz)	CFD	Fc (kHz)	CFD	Fc (kHz)
001	800.000	065	24.242	129	12.308	193	8.247
005	266.667	069	22.857	133	11.940	197	8.081
009	160.000	073	21.622	137	11.594	201	7.921
013	114.286	077	20.513	141	11.268	205	7.767
017	88.889	081	19.512	145	10.959	209	7.619
021	72.727	085	18.605	149	10.667	213	7.477
025	61.538	089	17.778	153	10.390	217	7.339
029	53.333	093	17.021	157	10.127	221	7.207
033	47.059	097	16.327	161	9.877	225	7.080
037	42.105	101	15.686	165	9.639	229	6.957
041	38.095	105	15.094	169	9.412	233	6.838
045	34.783	109	14.545	173	9.195	237	6.723
049	32.000	113	14.035	177	8.989	241	6.612
053	29.630	117	13.559	181	8.791	245	6.504
057	27.586	121	13.115	185	8.602	249	6.400
061	25.806	125	12.698	189	8.421	253	6.299

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Bit Rate Divider

The Transmit and Receive Bit Rate Divider register is used to extract a serial NRZ data stream for the CIrCC SCE. The divider is eight bits wide.

The input clock to the Bit Rate Divider is 100kHz (Carrier Frequency Divider input clock ÷ 16). The relationship between the Bit Rate Divider (BRD) and the Bit Rate (Fb) is as follows:

$$BRD = (.1MHz/Fb) - 1$$

For example, program the Bit Rate Divider with 55 ('37'Hex) for a .562ms Remote Control bit cell like for the NEC remote control frame format: Fb = 1.786kHz. This is ~.5% accuracy. Table 9 contains representative BRD vs. Bit Rate relationships. The Bit Rate range is 100kHz to 390.625Hz.

It is important to note that the bit rate as determined by the SCE CIR Bit Rate Divider register is not necessarily the data signaling rate for any given consumer remote control modulation scheme. For example, to support the NEC PPM remote control message frame format in the CIrCC, the value programmed in the SCE CIR Bit Rate register must be one half of the signaling rate for an NEC PPM "0" (see Figure 5).

Table 9 - Representative Bit Rates

| BRD	Fb (kHz)	BRD	Fb (kHz)	BRD	Fb (kHz)	BRD	Fb (kHz)
003	25.000	067	1.471	131	0.758	195	0.510
007	12.500	071	1.389	135	0.735	199	0.500
011	8.333	075	1.316	139	0.714	203	0.490
015	6.250	079	1.250	143	0.694	207	0.481
019	5.000	083	1.190	147	0.676	211	0.472
023	4.167	087	1.136	151	0.658	215	0.463
027	3.571	091	1.087	155	0.641	219	0.455
031	3.125	095	1.042	159	0.625	223	0.446
035	2.778	099	1.000	163	0.610	227	0.439
039	2.500	103	0.962	167	0.595	231	0.431
043	2.273	107	0.926	171	0.581	235	0.424
047	2.083	111	0.893	175	0.568	239	0.417
051	1.923	115	0.862	179	0.556	243	0.410
055	1.786	119	0.833	183	0.543	247	0.403
059	1.667	123	0.806	187	0.532	251	0.397
063	1.563	127	0.781	191	0.521	255	0.391

Receive Carrier Sense

The Programmable Receive Carrier Sense register is used to program the Consumer IR decoder to detect the presence of IR energy in a wide-to-narrow range of carrier frequencies. The register is two bits wide.

The range values are shown in Table 10. Carriers that fall outside of the programmed range set the Frame Abort bit. If the "Carrier Off" bit is active, the Receive Carrier range sensitivity function is disabled.

Table 10 - Receive Carrier Sense Range

D1	D0	RANGE
0	0	±10%
0	1	±20%
1	0	±40%
1	1	Reserved

FIGURE 6 - REMOTE CONTROL ASK ENCODE/DECODE

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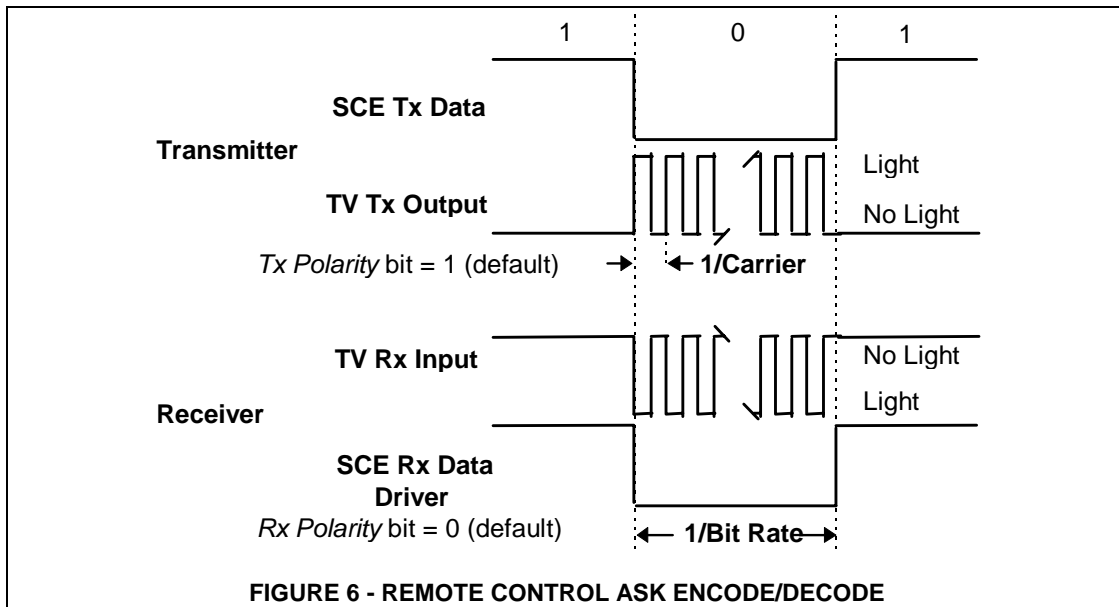
Receiver Bit Cell Synchronization

The Consumer IR Receiver demodulates incoming ASK waveforms into NRZ data for the SCE. The CIrCC uses the edges of the demodulated incoming infrared data to indicate changes in bit state.

For continuous periods of high or low data without transitions, the CIrCC samples the signal level in the center of each incoming bit period. Using the Receiver Bit Cell Synchronization mechanism, any transition resets the timer that is used in the sampling process to eliminate errors due to timing differences between the receive decoder and the incoming bit period (Figure 7).

Receiver synchronization can be disabled to allow direct sampling of the demodulated incoming infrared data stream at some preset receive bit rate. This is useful in situations where the speed of the receive data is not strictly known. In such cases, the receive bit rate is set as high as possible, the Receiver Bit Cell Synchronization is disabled, and the system software is used to measure the bit-cell period from the over sampled data. The learned parameters can then be used to switch to the synchronized, fixed bit-cell mode to reduce processing overhead in the host CPU for all future transactions.
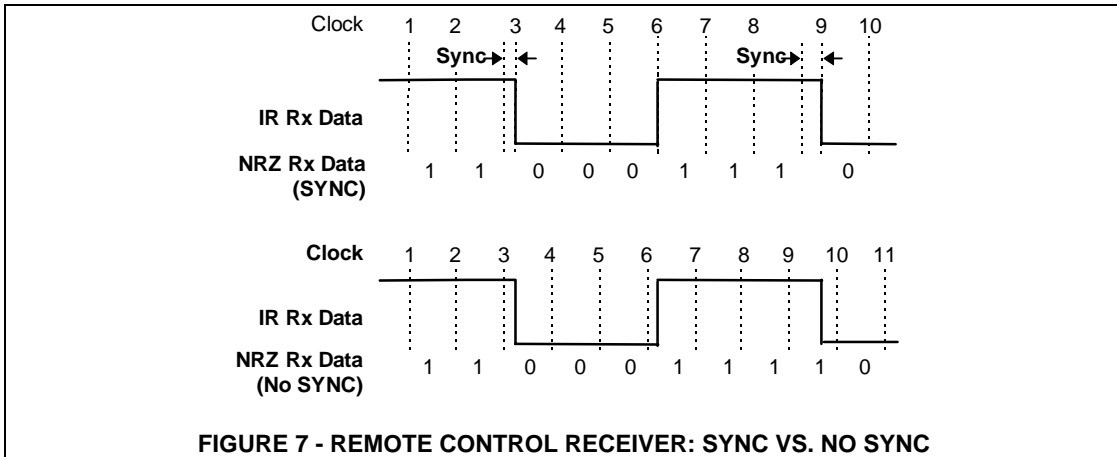

FIGURE 7 - REMOTE CONTROL RECEIVER: SYNC VS. NO SYNC

IrDA SIR AND SHARP ASK IR INTERFACE

This interface uses the ACE UART to provide a two-way wireless communications port using infrared as a transmission medium. Two distinct implementations have been provided in this block of the CIrCC, IrDA SIR and Sharp ASK IR.

IrDA SIR allows serial communication at baud rates up to 115K Baud. Each word is sent serially beginning with a zero value start bit. Sending a single infrared pulse at the beginning of the serial bit time signals a zero. A one is signaled by sending no infrared pulse during the bit time. Please refer to Figure 8-Figure 11 for the parameters of these pulses and the IrDA waveform.

The SHARP ASK interface allows asynchronous amplitude shift keyed serial communication at baud rates up to 19.2K Baud. Each word is sent serially beginning with a zero value start bit. A zero is signaled by sending a 500kHz waveform for the duration of the serial bit time.

A one is signaled by sending no transmission during the bit time. Please refer to the AC timing for the parameters of the ASKIR waveform.

If the Half Duplex option is chosen, there is a time-out when the direction of the transmission is changed. This time-out starts at the last bit transferred during a transmission and blocks the receiver input until the time-out expires. If the transmit buffer is loaded with more data before the time-out expires, the timer is restarted after the new byte is transmitted. If data is loaded into the transmit buffer while a character is being received, the transmission will not start until the time-out expires after the last receive bit has been received. If the start bit of another character is received during this time-out, the timer is restarted after the new character is received. The time-out is programmable up to a maximum of 10ms through the IR Half-Duplex Time-Out Configuration Register. Note: The IR Half Duplex Timeout is disabled in hardware when the CIR decoder is configured for wake-up.

FIGURE 8 - IrDA SIR RECEIVE TIMING
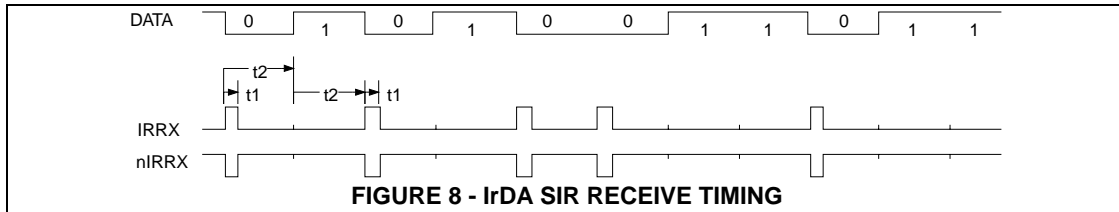
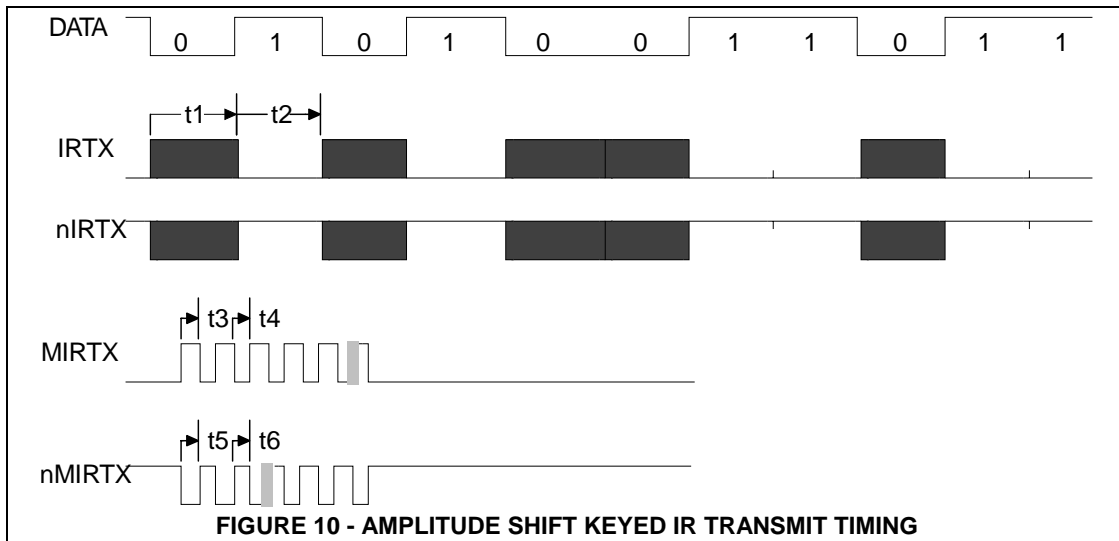|		PARAMETER	MIN	TYP	MAX	UNITS
t1		Pulse Width at 115kbaud	1.4	1.6	2.71	µs
t1		Pulse Width at 57.6kbaud	1.4	3.22	3.69	µs
t1		Pulse Width at 38.4kbaud	1.4	4.8	5.53	µs
t1		Pulse Width at 19.2kbaud	1.4	9.7	11.07	µs
t1		Pulse Width at 9.6kbaud	1.4	19.5	22.13	µs
t1		Pulse Width at 4.8kbaud	1.4	39	44.27	µs
t1		Pulse Width at 2.4kbaud	1.4	78	88.5	µs
t2		Bit Time at 115kbaud		8.68		µs
t2		Bit Time at 57.6kbaud		17.4		µs
t2		Bit Time at 38.4kbaud		26		µs
t2		Bit Time at 19.2kbaud		52		µs
t2		Bit Time at 9.6kbaud		104		µs
t2		Bit Time at 4.8kbaud		208		µs
t2		Bit Time at 2.4kbaud		416		µs

Notes:
1. IrDA @ 115k is HPSIR compatible. IrDA @ 2400 will allow compatibility with HP95LX and 48SX.
2. IRRX: Rx Polarity bit = 1
   nIRRX: Rx Polarity bit = 0 (default)

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FIGURE 9 - IrDA SIR TRANSMIT TIMING
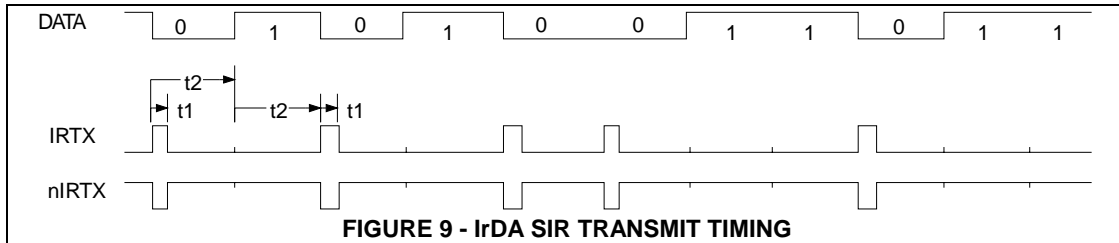
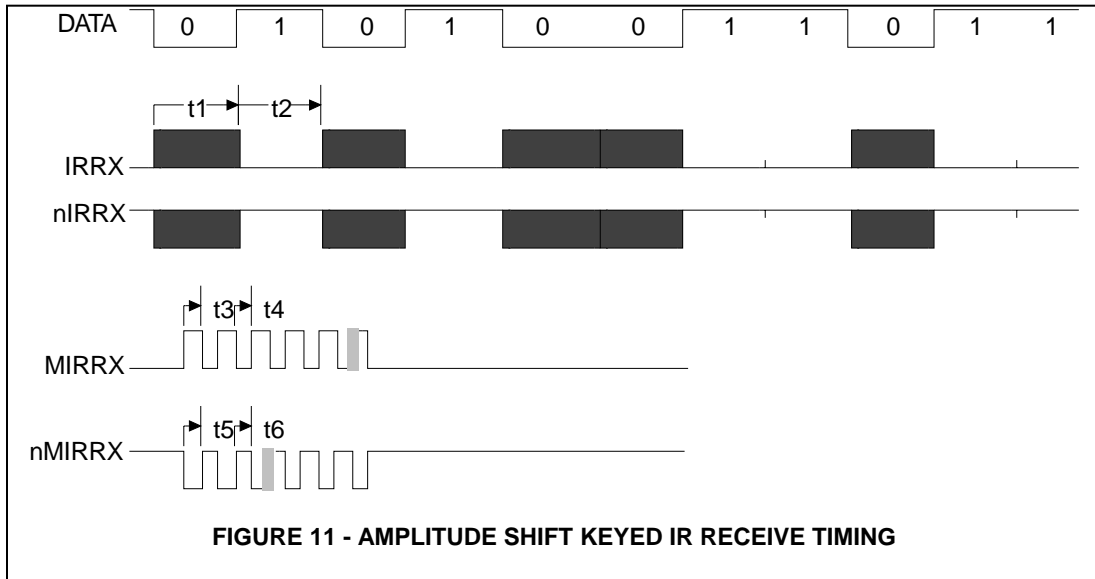|		PARAMETER	MIN	TYP	MAX	UNITS
t1		Pulse Width at 115kbaud	1.41	1.6	2.71	μs
t1		Pulse Width at 57.6kbaud	1.41	3.22	3.69	μs
t1		Pulse Width at 38.4kbaud	1.41	4.8	5.53	μs
t1		Pulse Width at 19.2kbaud	1.41	9.7	11.07	μs
t1		Pulse Width at 9.6kbaud	1.41	19.5	22.13	μs
t1		Pulse Width at 4.8kbaud	1.41	39	44.27	μs
t1		Pulse Width at 2.4kbaud	1.41	78	88.55	μs
t2		Bit Time at 115kbaud		8.68		μs
t2		Bit Time at 57.6kbaud		17.4		μs
t2		Bit Time at 38.4kbaud		26		μs
t2		Bit Time at 19.2kbaud		52		μs
t2		Bit Time at 9.6kbaud		104		μs
t2		Bit Time at 4.8kbaud		208		μs
t2		Bit Time at 2.4kbaud		416		μs

Notes:
1. Receive Pulse Detection Criteria: A received pulse is considered detected if the received pulse is a minimum of 1.41 μs
2. IRTX: Tx Polarity bit = 1 (default)
   nIRTX: Tx Polarity bit = 0

FIGURE 10 - AMPLITUDE SHIFT KEYED IR TRANSMIT TIMING

		PARAMETER	MIN	TYP	MAX	UNITS
	t1	Modulated Output Bit Time				µs
	t2	Off Bit Time				µs
	t3	Modulated Output "On"	0.8	1	1.2	µs
	t4	Modulated Output "Off"	0.8	1	1.2	µs
	t5	Modulated Output "On"	0.8	1	1.2	µs
	t6	Modulated Output "Off"	0.8	1	1.2	µs

Notes:
1. IRTX: Tx Polarity bit = 1 (default)
   nIRTX: Tx Polarity bit = 0
   MIRTX, nMIRTX are the modulated outputs.

FIGURE 11 - AMPLITUDE SHIFT KEYED IR RECEIVE TIMING

	PARAMETER	MIN	TYP	MAX	UNITS
t1	Modulated Output Bit Time				µs
t2	Off Bit Time				µs
t3	Modulated Output "On"	0.8	1	1.2	µs
t4	Modulated Output "Off"	0.8	1	1.2	µs
t5	Modulated Output "On"	0.8	1	1.2	µs
t6	Modulated Output "Off"	0.8	1	1.2	µs

Notes:
1. IRRX: Rx Polarity bit = 1
    nIRRX: Rx Polarity bit = 0 (default)
    MIRRX, nMIRRX are the modulated outputs.

REGISTERS

The CIrCC is partially enabled through binary controls found in two 8-byte register banks. The banks, the ACE550 UART Controls and the SCE Controls, are selected with the nACE and nSCE register-bank selector inputs found in the Interface Description.

If nACE is zero, the three least significant bits of the Host Address Bus decode the 16C550A UART control registers. If nSCE is zero, the SCE control bank is addressed. All of the CIrCC registers are 8 bits wide.

ACE UART CONTROLS

The table below (Table 12) lists the ACE UART Control Registers. See the current SMSC 16C550A implementation for a complete description.

Table 12 - 16C550A UART Addressing

DLAB	A2	A1	A0	DIRECTION	REGISTER NAME
0	0	0	0	Read	Receive Buffer
0	0	0	0	Write	Transmit Buffer
0	0	0	1	Read/Write	Interrupt Enable
X	0	1	0	Read	Interrupt Identification
X	0	1	0	Write	FIFO Control
X	0	1	1	Read/Write	Line Control
X	1	0	0	Read/Write	Modem Control
X	1	0	1	Read/Write	Line Status
X	1	1	0	Read/Write	Modem Status
X	1	1	1	Read/Write	Scratchpad
1	0	0	0	Read/Write	Divisor (LSB)
1	0	0	1	Read/Write	Divisor (MSB)

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SCE CONTROLS

The CIrCC SCE Registers are arranged in 7-byte blocks. Of the eight possible register blocks, four are used in this implementation.

The Master Block Control Register controls access to the register blocks. Table 13 lists all of the SCE registers in all blocks.

Table 13 - SCE Register Addressing

BLOCK	ADDRESS	DIRECTION	REGISTER NAME	
X	7	R/W	Master Block Control	
0	0	R/W	Data Register	
0	1	RO	Interrupt Identification	
0	2	R/W	Interrupt Enable	
0	3	RO	Line Status (read)	
0	3	WO	Line Status Address (write)	
0	4	R/W	Line Control A	
0	5	R/W	Line Control B	
0	6	R/W	Bus Status	
1	0	R/W	SCE Configuration A	
1	1	R/W	SCE Configuration B	
1	2	R/W	FIFO Threshold	
1	3	RO	FIFO COUNT	
1	6	R/W	SCE Configuration C	
2	0	R/W	Consumer IR Control	
2	1	R/W	Consumer IR Carrier Rate	
2	2	R/W	Consumer IR Bit Rate	
2	3	R/W	Custom Code	
2	4	R/W	Custom Code	
2	5	R/W	Data Code	
3	0	RO	SMSC ID (high)	
3	1	RO	SMSC ID (low)	
3	2	RO	CHIP ID	
3	3	RO	VERSION Number	
3	4	RO	IRQ Level	DMA Channel
3	5	RO	Software Select A	
3	6	RO	Software Select B	

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MASTER BLOCK CONTROL REGISTER

The Master Block Control Register contains the CIrCC Power Down bit, two reset bits, the Master Interrupt Enable bit, and the Register Block Select lines (Table 14).

Address 7 is solely reserved for the Master Block Control register. If the nSCE input is 0, the MBC is always visible, regardless of the state of the Register Block Select lines.

Table 14 - SCE Master Block Control Register

Address			Direction	Description								Default
A2	A1	A0		D7	D6	D5	D4	D3	D2	D1	D0	
1	1	1	R/W	Master Block Control Register								'00'hex
				power down	master reset	master int en.	error reset		register block select			

Register Block Select, bits 0-2
The Register Block Select bits enable access to each of the eight possible register blocks. To access a register block other than the default (0), write a 3 bit register block number to the least significant bits of the Master Block Control Register. All subsequent reads and writes to addresses 0 through 6 will access the registers in the new block. To return to register block 0, rewrite zeros to the register block select bits.

Error Reset, bit 4
Writing a one to the Error Reset bit will return all of the SCE Line Status Register bits (Register Block Zero) to their inactive states and reset the Message Count bits, the Memory Count bits, and the Message Byte Count registers to zero.

Master Interrupt Enable, bit 5
Setting the Master Interrupt Enable to one enable the SCE interrupts onto the Interrupt Request bus (IRQ) only if their individual enables are active. Setting this bit to a zero disables all SCE interrupts regardless of the state of their individual enables.

Master Reset, bit 6
Setting the Master Reset bit to one forces data in the SCE registers and SCE logical blocks into the Power-On-Reset state. The Master Reset bit is reset to zero following the reset operation. Note: The Legacy bits (Register Block One, Address Zero, Bits D0-D6) and the IR Half Duplex Timeout are unaffected by Master Reset.

Power Down, bit 7
Setting this bit to a one causes only the SCE to enter the low-power state. Power down mode does not preclude access to the Master Block Control register so that this mode can be maintained entirely under software control. The SCE can also be powered-down by the Power Down input described in the Interface Description.

REGISTER BLOCK ZERO

Register Block Zero contains the SCE Data Register, the Interrupt Control/Status registers, the Line Control/Status registers, and the Bus Status register (Table 15). Typically, the controls in Register Block Zero are used during Consumer IR message transactions. Bits and registers marked "reserved" in the table below cannot be written and return 0s when read. Programmers must set reserved bits to 0 when writing to registers that contain reserved bits.

Table 15 - Register Block Zero

Address			Direction	Description								Default
A2	A1	A0		D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	R/W	Data Register								
0	0	1	RO	Interrupt Identification Register								'00'hex
				active frame	eom	raw mode	fifo	IR busy	reserved			
0	1	0	R/W	Interrupt Enable Register								'00'hex
				active frame	eom	raw mode	fifo	IR busy	reserved			
0	1	1	RO	Line Status Register (read)								'00'hex
				under-run	over-run	frame error	reserved		frame abort	reserved		
0	1	1	WO	Line Status Address Register (write)								
				reserved					status register address			
1	0	0	R/W	Line Control Register A								'00'hex
				fifo reset	reserved		raw tx	raw rx	reserved			
1	0	1	R/W	Line Control Register B								'00'hex
				sce modes bits	reserved		message count					
1	1	0	RO	Bus Status Register								'00'hex
				not empty	fifo full	time-out	reserved				valid frame	

Data Register (Address 0)

The Data Register is the FIFO access port. Typically, the user will only write to the FIFO when transmitting and read from the FIFO when receiving. The host always has read access to the FIFO regardless of the state of the SCE Modes bits or the Loopback bit. Host read access to the FIFO is blocked when the FIFO is empty. The host has write access to the FIFO only when the Loopback bit is inactive and the SCE Modes bits are zero or Transmit mode is enabled. Host write access to the FIFO is blocked when the FIFO is full.

Interrupt Identification Register (Address 1)

When an interrupt is active the associated interrupt identifier bit in the IID register is also active regardless of the state of its individual interrupt enable or the Master Interrupt Enable, except for the FIFO Interrupt. The Master Interrupt Enable and the individual Interrupt Enables serve only to enable the IID register interrupts onto the Interrupt Request bus IRQ shown in the Interface Description.

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Active Frame Interrupt, bit 7

When this bit is one, an Active Frame has occurred (see the Active Frame Indicator section on page 54). The Active Frame typically indicates that the SCE receiver has detected a valid infrared carrier. Reading the Interrupt Identification register resets the Active Frame Interrupt bit.

EOM Interrupt, bit 6

When this bit is one, an End of Message has occurred. The EOM bit indicates the end of an Abort, FIFO underruns/overruns and DMA Terminal Counts. Reading the Interrupt Identification register resets the EOM bit.

Raw Mode Interrupt, bit 5

When this bit is one, a Raw Mode interrupt has occurred. The Raw Mode Interrupt indicates that the Raw Rx Control bit has gone active. Reading the Interrupt Identification register resets the Raw Mode Interrupt bit.

FIFO Interrupt, bit 4

When this bit is one, a FIFO Interrupt has occurred. The FIFO Interrupt indicates that the FIFO Interrupt Enable is active and either a TxServReq or a RxServReq has occurred. The FIFO Interrupt bit is cleared when the interrupt is disabled; i.e., reading the Interrupt Identification register does not reset the FIFO Interrupt bit (see the FIFO Interrupt section on page 57).

IR Busy, bit 3

The IR Media Busy hardware sets the IR Busy bit in the IID high if an infrared pulse that is greater than T_{PW_MIN} has occurred at the receiver input, except during message transmit or during the IR Half Duplex Timeout following message transmit.

T_{PW_MIN} can be defined as $20ns \# T_{PW\_MIN} \# 30ns$

The IR Media Busy hardware operates independently of the IR Rx Pulse Rejection filters, the programmed receive data rate, or the state of the ACE or SCE Rx Enables (see Figure 36). Reading the IID register will reset the IR Busy bit. The IR Busy bit is also reset following Master Reset and POR. If the IR Busy Enable bit is high, the IR Busy Interrupt is enabled onto the Interrupt Request bus IRQ if the master Interrupt Enable is also active. The IR Busy Enable bit does not affect the IR Busy bit in the IID.

PROGRAMMER'S NOTE: The IR Busy bit may be unintentionally activated during IR Mode changes.

Interrupt Enable Register (Address 2)

Setting any of the bits in this register to one enables the associated interrupt (see the Interrupt Identification Register). Interrupts will only occur if both the interrupt enable bit and the Master Interrupt Enable bit (see the Master Block Control Register) are active.

The interrupt enables do not affect the state of the interrupts, except for the FIFO Interrupt. For example, a Raw Mode interrupt that occurs while the Raw Mode Interrupt Enable is inactive will be visible in the IID register but will not affect IRQ.

Line Status Register(s) (Address 3)

Error Indicators (read-only)

There are eight Line Status Registers at address 3. Each register is read-only and is accessed using the three Status Register Address bits, also located at this address. The FIFO Underrun, FIFO Overrun, Frame Error, and Frame Abort Error flags indicate the status of any one of eight message frames. The Error Indicators, in all registers, are reset following a Master Reset, Power-On-Reset, and Error Reset (see the Master Block Control Register). The error indicators for the current status register only (see the Message Count bits) are reset following a valid start of frame sequence.

FIFO Underrun, bit 7

The FIFO Underrun bit gets set to one when the transmitter runs out of FIFO data.

FIFO Overrun, bit 6

The FIFO Overrun bit gets set to one when the receiver tries to write data to the FIFO when the FIFO Full flag is active.

Frame Error, bit 5

The Frame Error bit is set to one when bit-wide violations are detected during the payload, i.e. non-leader code, portion of NEC PPM remote control message frames.

Frame Abort, bit 2

The Frame Abort bit is set to one following a FIFO underrun during transmit, a FIFO Overrun during receive, and when detected carriers are out of range.

Status Register Address, bits 0 - 2 (write-only)

Three Status Register Address bits control software access to, and reside at the same address as, the Line Status Registers. The Status Register Address bits are write-only and occupy bits D0 to D2. To access any one of the eight Line Status Registers first write the address of the appropriate register (0 - 7), then read the register contents.

Line Control Register A (Address 4)

FIFO Reset, bit 7

When set to one, the FIFO Reset bit clears the FIFO Full and Not Empty flags in the 32-byte SCE FIFO. The FIFO Reset bit is automatically set to zero following the re-initialization.

Raw Tx, bit 4

The Raw Tx bit controls the state of the infrared emitter in Raw IR mode. The bit is read/write.

Raw Rx, bit 3

The Raw Rx bit represents the state of the infrared detector in Raw IR mode. The bit is read-only.

Line Control Register B (Address 5)

SCE Modes, bits 6 - 7
The SCE Modes bits enable the SCE transmitter and receiver (Table 16). These bits are R/W and must be manually reset by the host following CIR message transactions when the FRAME bit is one. The SCE Modes bits are automatically reset by the hardware following FIFO Overruns or Underruns. Note: The SCE Modes bits must be zero for loopback tests.

Table 16 - SCE Modes

D7	D6	MODE DESCRIPTION
0	0	Receive/Transmit Disabled (default)
0	1	Transmit Mode
1	0	Receive Mode
1	1	Undefined

Transmit Mode
Transmit mode enables the SCE Consumer IR transmitter whenever TC goes active, or the FIFO THRESHOLD has been exceeded (see the Transmit Timing section on page 54). In Transmit mode, the SCE FIFO input is connected to the Host System Data Bus and the FIFO output is connected to the SCE transmitter input. The Consumer IR encoder will reset Transmit mode in hardware following the rising edge of nActive Frame following a FIFO underrun.

Receive Mode
Receive mode enables the SCE Consumer IR receiver (see the Receive Timing section on page 54). In Receive mode, the SCE FIFO output is connected to the Host System Data Bus, the FIFO input is connected to the SCE receiver output. The Consumer IR encoder will reset Receive mode in hardware following the rising edge of nActive Frame following a FIFO underrun or TC.

Message Count, bits 0 - 3
The four Message Count bits control (internal*)* hardware access to the Line Status Registers and are unaffected by the Status Register Address. The Message Count bits also indicate the system message-state. For example, if the Message Count bits are zero, i.e. the power-up default, Line Status Register zero is active, although undefined because no messages have been sent or received. The Message Count bits

are incremented after every active frame. At point A in Figure 18, for example, the rising edge of nActive Frame increments Message Count by one indicating that the first message has been received. This means that Line Status Register #1 (status register address 0) is valid, and Line Status Register #2 is currently active, although undefined. Hardware prevents the Message Count register from exceeding eight ('1000'Binary).
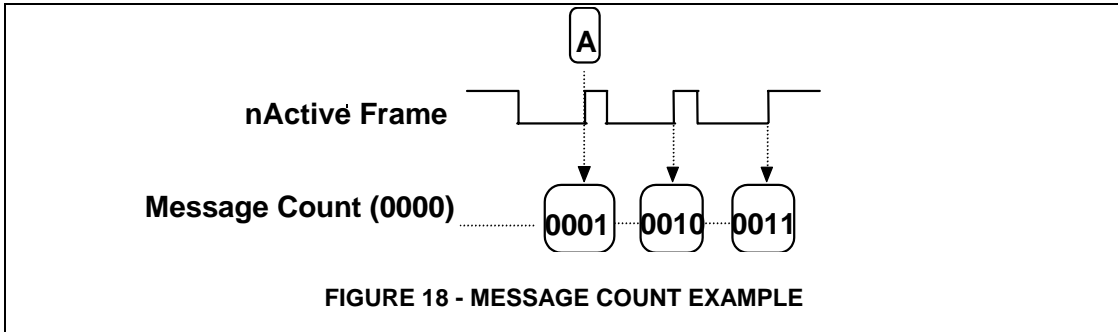
FIGURE 18 - MESSAGE COUNT EXAMPLE

Bus Status Register (Address 6)

FIFO Indicators (read-only)
The FIFO Indicators reflect the current status of the SCE FIFO.

FIFO Not Empty, bit 7
The FIFO Not Empty bit when set to one indicates that there is data in the SCE FIFO.

FIFO Full, bit 6
The FIFO Full bit when set to one indicates that there is no room for data in the SCE FIFO.

Time-Out, bit 5
The Time-Out bit is the IOCHRDY time-out error bit. The Time-Out bit when set to one indicates that an IOCHRDY time-out error has occurred (see the IOCHRDY Time-Out section on page 63). Time-Out is reset by the CIrCC System Reset, following a read of the Bus Status register, and following a Master Reset.

Valid Frame, bit 0
The Valid Frame bit reflects the state of the internal state variable nActive Frame. When nActive Frame=0 (active) Valid Frame=1 (active). When nActive Frame=1 (inactive) Valid Frame=0 (inactive). Valid Frame is only defined for the SCE Encoder/Decoders during Transmit and Receive.

REGISTER BLOCK ONE

Register Block One contains the SCE control registers (Table 17). Typically, the controls in Register Block One are needed to configure the SCE before message transactions can occur. Bits and registers marked "reserved" in the table below cannot be written and return 0s when read. Programmers must set reserved bits to 0 (zero) when writing to registers that contain reserved bits.

Table 17 - Register Block One

Address			Direction	Description								Default
A2	A1	A0		D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	R/W	SCE Configuration Register A								'02'hex
				aux ir	block control bits				half duplx	tx po-larity	rx po-larity	
0	0	1	R/W	SCE Configuration Register B								'00'hex
				output mux bits		loop-back		no wait	string move	dma burst	dma enable	
0	1	0	R/W	FIFO Threshold Register								'00'hex
0	1	1	RO	FIFO COUNT								'00'hex
				FC7	FC6	FC5	FC4	FC3	FC3	FC1	FC0	
1	0	0		Reserved								
1	0	1		Reserved								
1	1	0	R/W	SCE Configuration Register C								'03'hex
				rsvd	tx pw limit	reserved				DMA Refresh Count		

SCE Configuration Register A (Address 0)

Auxiliary IR, bit 7
When the Auxiliary IR bit is one and the active device is routed through the Output Multiplexer to the IR Port or the COM Port, the transmit signal also appears at the Auxiliary Port.

Block Control, bits 3 – 6
The Block Control bits select one of the six IrCC 2.0 operational modes (Table 18). The three low-order Block Control bits are

equivalent to the IR Mode bits in the chip-level configuration space of earlier devices; e.g., the FDC37C93x IR Option Register, Serial Port 2, Logical Device 5, Register 0xF1. Provisions have been made in legacy devices to accommodate IR Mode selection through either the chip-level configuration registers or the IrCC 2.0 Block Control bits; i.e., the last write from either source determines the current mode selection and is visible in both registers.

TABLE 18 - IRCC LOGICAL BLOCK CONTROLS

D6	D5	D4	D3	MODE	DESCRIPTION
0	0	0	0	COM	16550 UART COM Port (default)
0	0	0	1	IrDA SIR - A	Up to 115.2 kbps, Variable 3/16 Pulse
0	0	1	0	ASK IR	Amplitude Shift Keyed Ir Interface
0	0	1	1	IrDA SIR - B	Up to 115.2 kbps, Fixed 1.6μs Pulse
0	1	0	0	-	Reserved
0	1	0	1	-	Reserved
0	1	1	0	CONSUMER	Remote Control
0	1	1	1	RAW IR	Direct IR Diode Control
1	X	X	X	-	Reserved

Half Duplex, bit 2

When Half Duplex is zero (default), the 16C550A is in full duplex mode. The Half Duplex bit only supports the 16C550A UART; i.e., this bit has no effect on the CIrCC SCE. The Half Duplex bit is analogous to the chip-level configuration register Half Duplex bit and has the same effect on the UART. Provisions have been made in legacy devices to accommodate Half Duplex selection through either the chip-level configuration registers or the CIrCC Half Duplex bit; i.e., the last write from either source determines the current mode selection and is visible in both registers.

Tx/Rx Polarity Bits, 0 - 1

The Tx and Rx Polarity bits define the active states for signals entering and exiting the Output Multiplexer ports. Internal CIrCC Active states are typically decoded as zero. The Tx Polarity bit default is one; the Rx Polarity bit default is zero.

For backward compatibility, the Tx and Rx Polarity bits do not apply to COM mode; i.e., when the Block Control bits are zero. The relationship between the Output Multiplexer port signals and the Polarity bits is an exclusive-or (Table 19). For example, if the IRRx pin in the Output Multiplexer is one and the Rx Polarity bit is zero, the signal is inactive and therefore decoded as a one. The CIrCC Tx Polarity bit (bit 1) is equivalent to the Transmit Polarity bit in the chip-level configuration space of earlier devices; e.g., the FDC37C93x IR Option Register, Serial Port 2, Logical Device 5, Register 0xF1. The Rx Polarity bit (bit 0) is equivalent to the Receive Polarity bit in the same register. Provisions have been made in legacy devices to accommodate Polarity bit selection through either the chip-level configuration registers or the SCE registers; i.e., the last write from either source determines the current Polarity bit value and is visible in both registers.

Table 19 - Tx/Rx Polarity Bit Effects

SIGNAL	POLARITY BIT	DECODED SIGNAL
0	0	0
0	1	1
1	0	1
1	1	0

SCE Configuration Register B (Address 1)

Output Mux, bits 7 - 6
The Output Mux bits select the Output Multiplexer port for the active encoder/decoder (Table 20). When D[7:6]=1,1 in Table 20 inactive outputs depend on the state of the Tx Polarity bit, otherwise inactive outputs are zero. The Output Mux bits are equivalent to the FDC37C93x IR Option Register bits 6-7. The IR Location Mux, bit 6, in the FDC37C93x IR Option Register is equivalent to Output Mux bit, D6; bit 7 (Reserved) in the FDC37C93x IR Option Register is equivalent to Output Mux bit, D7. Provisions have been made in legacy devices to accommodate Output Multiplexer port selection through either the chip-level configuration registers or the Output Mux bits; i.e., the last write from either source determines the current port selection and is visible in both registers.

Table 20 - ClrCC Output Multiplexer

D7	D6	MUX. MODE
0	0	Active Device to COM Port (default)
0	1	Active Device to IR Port
1	0	Active Device to AUX Port
1	1	Outputs Inactive

Loopback, bit 5
The Loopback bit configures the FIFO and enables the transmitter/receiver for loopback testing. The SCE MODES bits must be set to zero before activating the Loopback bit. When the Loopback bit is one, the SCE enters a full-duplex mode with internal loopback capability for testing. The 32-byte FIFO input is connected to the SCE receiver output, the FIFO output is connected to the SCE transmit input. Consumer IR loopback tests reset the Loopback bit automatically when the Rx Data Size register reaches zero. Provisions must be made following loopback tests in all modes to verify the Rx message data in the FIFO.

No Wait, bit 3
When the No Wait bit is one, the ISA Bus nSRDY signal goes active following the trailing edge of the ISA I/O command and inactive following the rising edge (see the Zero Wait State Support section on page 65).

String Move, Bit 2
When the String Move bit is one, the programmed I/O host interface is qualified by IOCHRDY (Table 21). See the IOCHRDY Time-Out section on page 63.

DMA Burst Mode, bit 1

When the DMA Burst Mode bit is one, DMA Burst (Demand) mode is enabled. When the DMA Burst Mode bit is zero, Single Byte DMA mode is enabled (Table 21). See the DMA section on page 58.

DMA Enable, bit 0
DMA Enable is connected to a signal in the Interface Description called DMAEN that is used by the chip-level interface to tristate the CIrCC DMA controls when the DMA interface is inactive. When the DMA Enable bit is one, the DMA host interface is active (Table 21). See the DMA section on page 58. When the DMA Enable bit is zero (default), the nDACK and TC inputs are disabled and DRQ output is gated off.

Table 21 - I/O Interface Modes

STRING MOVE	DMA BURST	DMA ENABLE	FUNCTION
0	X	0	Programmed I/O, no IOCHRDY
1	X	0	Programmed I/O, uses IOCHRDY
X	0	1	Single Byte DMA Mode
X	1	1	Demand Mode DMA

FIFO Threshold Register (Address 2)

The FIFO Threshold register contains the programmable FIFO threshold count. The FIFO threshold is programmable from 0 to 31. Bits 6 and 7 in the FIFO Threshold register are read-only and will always return zero. FIFO Threshold values typically reflect the overall I/O performance characteristics of the host; the lower the value, the longer the interval between service requests and the faster the host must be to successfully service them. The same threshold value can be used for both I/O read and I/O write cases.

FIFO COUNT Register (Address 3)

The FIFO COUNT register represents the remaining number of data bytes in the 128-byte SCE FIFO. When the FIFO COUNT is 0x00 the FIFO is empty. When the FIFO is full the FIFO COUNT is 0x80. The FIFO COUNT is independent of the data flow direction. For example, if the FIFO COUNT is 0x0A during transmit there are ten bytes to send; if the FIFO COUNT is 0x0A during receive there are ten bytes to read.

Tx PW Limit, bit 6
The Tx PW Limit bit enables hardware designed to restrict the IR transmit pulse width (see the Transmit Pulse Width Limit section on page 67). If Tx PW Limit = 0, The TRANSMIT PULSE WIDTH LIMIT hardware is defeated and no transmit pulse width restrictions are made. If Tx PW Limit = 1, The TRANSMIT PULSE WIDTH LIMIT hardware will prevent pulses larger than 100Fs with a 25% duty cycle from appearing at the IRCC TX output ports.

DMA Refresh Count, bits 0 - 1

The DMA Refresh Count bits are used to program the DMA Refresh Counter. See the DMA Refresh Counter section on page 59 for more details. The DMA Refresh Counter can be preloaded with count values of 4, 8, 16, or 32 as determined by the DMA Refresh Count bits[1:0] as shown in Table 22.

Table 22 - DMA Refresh Count Bit Encoding

DMA REFRESH COUNT BITS		DMA COUNTER
D1	D0	PRELOAD VALUE
0	0	4
0	1	8
1	0	16
1	1	32 (default)

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REGISTER BLOCK TWO

Register Block Two contains the Consumer IR

(Remote Control) encoder/decoder configuration registers (Table 23).

Table 23 - Register Block Two

ADDRESS			DIR	DESCRIPTION								DEFAULT
A2	A1	A0		D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	R/W	Consumer IR Remote Control Register								'00'hex
				sync bit	frame	pme wake	nccc	ncdc	carrier off	carrier range bits		
0	0	1	R/W	Consumer IR Carrier Rate Register								'29'hex
0	1	0	R/W	Consumer IR Bit Rate Register								'37'hex
0	1	1	R/W	Custom Code								'00'hex
1	0	0	R/W	Custom Code'								'00'hex
1	0	1	R/W	Data Code								'00'hex
1	1	0		Reserved								

Consumer IR Control Register (Address 0)

Sync Bit, bit 7
The Sync Bit enables the receiver bit-rate clock synchronization mechanism. When the Sync bit is one, receiver edge synchronization is enabled (see the Receiver Bit Cell Synchronization section on page 16).

Frame Bit, bit 6
The Frame bit determines the compatibility mode of the CIR decoder (Table 24). If the Frame bit is one, the CIR hardware decodes NEC PPM remote control frames. If the Frame bit is zero (default), frame decoding must be performed in software.

PME Wake, bit 5
The PME Wake bit is used to configure the CIR decoder for a PME wake-up event and to clear the PME output (Table 24). When the PME Wake bit is one, the CIR decoder qualifies incoming message frames depending upon the state of the 16 bit Custom Code register, the 8 bit Data Code register, the NCCC bit and the NCDC bit and activates the CIrCC PME output when appropriate. When the PME Wake bit is one, the data received from NEC CIR remote frames is not sent to the FIFO. When the PME Wake bit is zero (default), the CIrCC PME output is cleared, the CIR decoder qualifies incoming message frames depending on the state of the 16 bit

Custom Code register and the NCCC bit, and sends valid data to the FIFO.

NCCC, bit 4
The No Care Custom Code (NCCC) bit determines the behavior of the CIR decoder when the Frame bit is active (one) (Table 24). When the NCCC bit is one and the PME Wake bit is one, a PME event will be generated upon receipt of a valid NEC CIR frame if the data code field of the NEC frame matches the value of the Data Code register, regardless of the custom code field of the incoming frame. When the NCCC bit is zero (default) and the PME Wake bit is active (one), a PME event may be generated if the custom code of the incoming NEC CIR frame matches the value programmed into the 16 bit Custom Code register, depending upon NCDC qualification. When the NCCC bit is one and the PME Wake bit is inactive (zero), the 8 bit data code and the 16 bit custom code field of any valid NEC CIR frame that is received will be sent to the FIFO. When the NCCC bit is zero (default) and the PME Wake bit is zero, the data code field of an incoming NEC CIR frame will be written to the FIFO if the custom code field matches the value programmed into the 16 bit Custom Code register. Non-qualifying frames are ignored by the hardware.

NCDC, bit 3

The No Care Data Code (NCDC) bit determines the behavior of the CIR decoder when both the Frame and the PME Wake bits are active (one) (Table 24). When the NCDC bit is one, a PME event may be generated regardless of the data programmed in the 8 bit Data Code register, pending NCCC qualification. This enables a wake-up event on any key press. When the NCDC bit is zero (default), a PME event can only be generated if the data code field in the received NEC CIR frame matches the value programmed in the 8 bit Data Code register; NCCC qualification may also apply. This enables a wake-up event for a particular key-press. Note: The NCDC bit has no effect if either the Frame bit or the PME Wake bit is inactive (zero).

TABLE 24 - NCCC AND NCDC FUNCTIONALITY

FRAME	NCCC	NCDC	PME WAKE	FUNCTION
0	X	X	X	No CIR Hardware Framing or Wake-up Events.
1	0	X	0	The data code field of incoming frame is written to the FIFO if the custom code field of incoming NEC CIR frame matches the value of the 16 bit Custom Code register.
1	0	0	1	PME signal is asserted if the custom code and the data code fields of incoming NEC CIR frame match the values programmed in the 16 bit Custom Code and 8 bit Data Code registers.
1	0	1	1	PME signal is asserted if the custom code field of incoming NEC CIR frame matches the value programmed in the 16 bit Custom Code register, regardless of the data that is programmed in the 8-bit Data Code register.
1	1	X	0	The custom code and the data code fields of any valid NEC CIR frame are written to the FIFO.
1	1	0	1	PME signal is asserted if the data code field of an incoming NEC CIR frame matches the value of the 8 bit Data Code register.
1	1	1	1	PME asserted upon receipt of any valid NEC CIR frame.

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Carrier Off, bit 2

The Carrier Off bit bypasses the Consumer IR Carrier generator/receiver (see the Carrier Frequency Divider section on page 12). When the Carrier Off bit is one, the transmitter outputs a non-modulated SCE NRZ serial data stream at the programmed bit rate. Also, when the Carrier Off bit is one, the receiver does not attempt to demodulate a carrier from the incoming data stream and samples the state of the PIN diode at the programmed bit rate.

Carrier Range, bits 0 - 1

The Consumer IR Carrier Range Bits set the carrier detect sensitivity of the receiver. The effects of this register are shown in Table 10.

Consumer IR Carrier Rate Register (Address 1)

The Consumer IR Carrier Rate Register programs the ASK carrier frequency divider. The effects of this register are shown in Table 8.

Consumer IR Bit Rate Register (Address 2)

The Consumer IR Bit Rate Register programs the transmit and receive bit-rate divider. The effects of this register are shown in Table 9.

REGISTER BLOCK THREE

Register Block Three contains the CIrCC Block Identifier Registers. These read-only registers classify the hardware Manufacturer, the Device ID, the Version number, and Host interface parameters. Bits and registers marked "reserved" in the table below cannot be written and return 0 when read. Programmers must set reserved bits to 0 when writing to registers that contain reserved bits.

Table 25 - Register Block Three

ADDRESS			DIRECTION	DESCRIPTION								DEFAULT
A2	A1	A0		D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	RO	SMSC ID (high-byte)								'10'hex
0	0	1	RO	SMSC ID (low-byte)								'B8'hex
0	1	0	RO	CHIP ID								'FA'hex
0	1	1	RO	VERSION Number								'00'hex
1	0	0	RO	IRQ Level				DMA Channel				Note 1
1	0	1	RO	Software Select A								Note 1
1	1	0	RO	Software Select B								Note 1

NOTE 1: The default values for these registers assume the values that have been programmed in chip-level configuration registers.

SMSC ID (Addresses 0 - 1)

The SMSC ID registers contain a 16 bit manufacturer identification code. Address zero contains the high byte of this code, address one contains the low byte.

Chip ID (Address 2)

The Chip ID register specifically identifies this SMSC product.

Version Number (Address 3)

The Version Number register identifies the revision-level of the product referenced by the Chip ID register.

IRQ Level/ DMA Channel (Address 4)

IRQ Level, bits 4 - 7
The IRQ Level bits identify the current active IRQ number for this device. The value comes from the 4 bit IRQ Level Bus found in the Interface Description.

DMA Channel, bits 0 – 3

The DMA Channel bits identify the current active DMA Channel number for this device. The value comes from the 4 bit DMA Channel Bus found in the Interface Description.

Software Select A (Address 5)

The Software Select A register is software-only controlled from a chip-level configuration register (see the CIrCC-Specific Chip-Level Controls section on page 8).

Software Select B (Address 6)

The Software Select B register is software-only controlled from a chip-level configuration register (see the CIrCC-Specific Chip-Level Controls section on page 8).

ACE UART

The SMSC CIrCC incorporates one full function UART compatible with the NS16450, the 16450 ACE registers and the NS16C550A. The UART performs serial-to-parallel conversion on received characters and parallel-to-serial conversion on transmit characters. The data rates are independently programmable from 115.2K baud down to 50 baud. The character options are programmable for 1 start; 1, 1.5 or 2 stop bits; even, odd, sticky or no parity; and prioritized interrupts. The UART contains a programmable baud rate generator that is capable of dividing the input clock or crystal by a number from 1 to 65535. The UART is also capable of supporting the MIDI data rate. Refer to the Configuration Register section of the device data sheet for the information on disabling, power down and changing the base address of the UART. The interrupt from the UART is enabled by programming OUT2 of the UART to a logic "1". OUT2 being a logic "0" disables the UART's interrupt.

REGISTER DESCRIPTION

Addressing of the accessible registers of the Serial Port is shown below. The configuration registers define the base addresses of the serial ports. The Serial Port registers are located at sequentially increasing addresses above these base addresses. The SMSC CIrCC UART register set is described below.

Table 26 - Addressing The Serial Port

DLAB*	A2	A1	A0	REGISTER NAME
0	0	0	0	Receive Buffer (read)
0	0	0	0	Transmit Buffer (write)
0	0	0	1	Interrupt Enable (read/write)
X	0	1	0	Interrupt Identification (read)
X	0	1	0	FIFO Control (write)
X	0	1	1	Line Control (read/write)
X	1	0	0	Modem Control (read/write)
X	1	0	1	Line Status (read/write)
X	1	1	0	Modem Status (read/write)
X	1	1	1	Scratchpad (read/write)
1	0	0	0	Divisor LSB (read/write)
1	0	0	1	Divisor MSB (read/write)

*NOTE: DLAB is Bit 7 of the Line Control Register

The following section describes the operation of the registers.

RECEIVE BUFFER REGISTER (RB)
Address Offset = 0H, DLAB = 0, READ ONLY

This register holds the received incoming data byte. Bit 0 is the least significant bit, which is transmitted and received first. Received data is double buffered; this uses an additional shift register to receive the serial data stream and convert it to a parallel 8 bit word which is transferred to the Receive Buffer register. The shift register is not accessible.

TRANSMIT BUFFER REGISTER (TB)
Address Offset = 0H, DLAB = 0, WRITE ONLY

This register contains the data byte to be transmitted. The transmit buffer is double buffered, utilizing an additional shift register (not accessible) to convert the 8 bit data word to a serial format. This shift register is loaded from the Transmit Buffer when the transmission of the previous byte is complete.

INTERRUPT ENABLE REGISTER (IER)
Address Offset = 1H, DLAB = 0, READ/WRITE

The lower four bits of this register control the enables of the five interrupt sources of the Serial Port interrupt. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of this register. Similarly, setting the appropriate bits of this register to a high, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and disables any Serial Port interrupt out of the SMSC CIrCC. All other system functions operate in their normal manner, including the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are described below.

Bit 0
This bit enables the Received Data Available Interrupt (and timeout interrupts in the FIFO mode) when set to logic "1".

Bit 1
This bit enables the Transmitter Holding Register Empty Interrupt when set to logic "1".

Bit 2
This bit enables the Received Line Status Interrupt when set to logic "1". The error sources causing the interrupt are Overrun, Parity, Framing and Break. The Line Status Register must be read to determine the source.

Bit 3
This bit enables the MODEM Status Interrupt when set to logic "1". This is caused when one of the Modem Status Register bits changes state.

Bits 4 through 7
These bits are always logic "0".

FIFO CONTROL REGISTER (FCR)
Address Offset = 2H, DLAB = X, WRITE

This is a write only register at the same location as the IIR. This register is used to enable and clear the FIFOs, set the RCVR FIFO trigger level. Note: DMA is not supported.

Bit 0
Setting this bit to a logic "1" enables both the XMIT and RCVR FIFOs. Clearing this bit to a logic "0" disables both the XMIT and RCVR FIFOs and clears all bytes from both FIFOs. When changing from FIFO Mode to non-FIFO (16450) mode, data is automatically cleared from the FIFOs. This bit must be a 1 when other bits in this register are written to or they will not be properly programmed.

Bit 1
Setting this bit to a logic "1" clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. This bit is self-clearing.

Bit 2

Setting this bit to a logic "1" clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. This bit is self-clearing.

Bit 3

Writing to this bit has no effect on the operation of the UART. The RXRDY and TXRDY pins are not available on this chip.

Bit 4,5

Reserved

BIT 7	BIT 6	RCVR FIFO TRIGGER LEVEL
0	0	1
0	1	4
1	0	8
1	1	14

Bit 6,7

These bits are used to set the trigger level for the RCVR FIFO interrupt.

INTERRUPT IDENTIFICATION REGISTER (IIR)
Address Offset = 2H, DLAB = X, READ

By accessing this register, the host CPU can determine the highest priority interrupt and its source. Four levels of priority interrupt exist. They are in descending order of priority:

1. Receiver Line Status (highest priority)
2. Received Data Ready

3. Transmitter Holding Register Empty
4. MODEM Status (lowest priority)

Information indicating that a prioritized interrupt is pending and the source of that interrupt is stored in the Interrupt Identification Register (refer to Table 27 - Interrupt Control Table). When the CPU accesses the IIR, the Serial Port freezes all interrupts and indicates the highest priority pending interrupt to the CPU. During this CPU access, even if the Serial Port records new interrupts, the current indication does not change until access is completed. The contents of the IIR are described below.

Bit 0

This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic "0", an interrupt is pending and the contents of the IIR may be used as a pointer to the appropriate internal service routine. When bit 0 is logic "1", no interrupt is pending.

Bits 1 and 2

These two bits of the IIR are used to identify the highest priority interrupt pending as indicated by the Interrupt Control Table.

Bit 3

In non-FIFO mode, this bit is a logic "0". In FIFO mode this bit is set along with bit 2 when a timeout interrupt is pending.

Bits 4 and 5

These bits of the IIR are always logic "0".

Bits 6 and 7

These two bits are set when the FIFO CONTROL Register bit 0 equals 1.

Table 27 - Interrupt Control

| FIFO MODE ONLY | INTERRUPT IDENTIFICATION REGISTER | | | INTERRUPT SET AND RESET FUNCTIONS | | | |
BIT 3	BIT 2	BIT 1	BIT 0	PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET CONTROL
0	0	0	1	-	None	None	-
0	1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available	Read Receiver Buffer or the FIFO drops below the trigger level.
1	1	0	0	Second	Character Timeout Indication	No Characters Have Been Removed From or Input to the RCVR FIFO during the last 4 Char times and there is at least 1 char in it during this time	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if Source of Interrupt) or Writing the Transmitter Holding Register
0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

LINE CONTROL REGISTER (LCR)
Address Offset = 3H, DLAB = 0, READ/WRITE

This register contains the format information of the serial line. The bit definitions are:

Bits 0 and 1
These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

BIT 1	BIT 0	WORD LENGTH
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

The Start, Stop and Parity bits are not included in the word length.

Bit 2
This bit specifies the number of stop bits in each transmitted or received serial character. The following table summarizes the information.

BIT 2	WORD LENGTH	NUMBER OF STOP BITS
0	--	1
1	5 bits	1.5
1	6 bits	2
1	7 bits	2
1	8 bits	2

NOTE: The receiver will ignore all stop bits beyond the first, regardless of the number used in transmitting.

Bit 3
Parity Enable bit. When bit 3 is a logic "1", a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and the first stop bit of the serial data. (The parity bit is used to generate an even or odd number of 1s when the data word bits and the parity bit are summed).

Bit 4
Even Parity Select bit. When bit 3 is a logic "1" and bit 4 is a logic "0", an odd number of logic "1"'s is transmitted or checked in the data word bits and the parity bit. When bit 3 is a logic "1" and bit 4 is a logic "1" an even number of bits is transmitted and checked.

Bit 5
Stick Parity bit. When bit 3 is a logic "1" and bit 5 is a logic "1", the parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

Bit 6
Set Break Control bit. When bit 6 is a logic "1", the transmit data output (TXD) is forced to the Spacing or logic "0" state and remains there (until reset by a low level bit 6) regardless of other transmitter activity. This feature enables the Serial Port to alert a terminal in a communications system.

Bit 7
Divisor Latch Access bit (DLAB). It must be set high (logic "1") to access the Divisor Latches of the Baud Rate Generator during read or write operations. It must be set low (logic "0") to access the Receiver Buffer Register, the Transmitter Holding Register, or the Interrupt Enable Register.

MODEM CONTROL REGISTER (MCR)
Address Offset = 4H, DLAB = X, READ/WRITE

This 8 bit register controls the interface with the MODEM or data set (or device emulating a MODEM). The contents of the MODEM control register are described below.

Bit 0

This bit controls the Data Terminal Ready (nDTR) output. When bit 0 is set to a logic "1", the nDTR output is forced to a logic "0". When bit 0 is a logic "0", the nDTR output is forced to a logic "1".

Bit 1

This bit controls the Request To Send (nRTS) output. Bit 1 affects the nRTS output in a manner identical to that described above for bit 0.

Bit 2

This bit controls the Output 1 (OUT1) bit. This bit does not have an output pin and can only be read or written by the CPU.

Bit 3

Output 2 (OUT2). This bit is used to enable an UART interrupt. When OUT2 is a logic "0", the serial port interrupt output is forced to a high impedance state - disabled. When OUT2 is a logic "1", the serial port interrupt outputs are enabled.

Bit 4

This bit provides the loopback feature for diagnostic testing of the Serial Port. When bit 4 is set to logic "1", the following occur:

1. The TXD is set to the Marking State(logic "1").
2. The receiver Serial Input (RXD) is disconnected.
3. The output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input.
4. All MODEM Control inputs (nCTS, nDSR, nRI and nDCD) are disconnected.
5. The four MODEM Control outputs (nDTR, nRTS, and OUT2) are internally connected to the four MODEM Control inputs.
6. The Modem Control output pins are forced inactive high.
7. Data that is transmitted is immediately received.

This feature allows the processor to verify the transmit and receive data paths of the Serial Port.

In the diagnostic mode, the receiver and the transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

Bits 5 through 7

These bits are permanently set to logic zero.

LINE STATUS REGISTER (LSR)
Address Offset = 5H, DLAB = X, READ/ WRITE

Bit 0

Data Ready (DR). It is set to a logic "1" whenever a complete incoming character has been received and transferred into the Receiver Buffer Register or the FIFO. Bit 0 is reset to a logic "0" by reading all of the data in the Receive Buffer Register or the FIFO.

Bit 1

Overrun Error (OE). Bit 1 indicates that data in the Receiver Buffer Register was not read before the next character was transferred into the register, thereby destroying the previous character. In FIFO mode, an overrun error will occur only when the FIFO is full and the next character has been completely received in the shift register, the character in the shift register is overwritten but not transferred to the FIFO. The OE indicator is set to a logic "1" immediately upon detection of an overrun condition, and reset whenever the Line Status Register is read.

Bit 2

Parity Error (PE). Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even parity select bit. The PE is set to a logic "1" upon detection of a parity error and is reset to a logic "0" whenever the Line Status Register is read. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO.

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Bit 3

Framing Error (FE). Bit 3 indicates that the received character did not have a valid stop bit. Bit 3 is set to a logic "1" whenever the stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level). The FE is reset to a logic "0" whenever the Line Status Register is read. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. The Serial Port will try to resynchronize after a framing error. To do this, it assumes that the framing error was due to the next start bit, so it samples this 'start' bit twice and then takes in the 'data'.

Bit 4

Break Interrupt (BI). Bit 4 is set to a logic "1" whenever the received data input is held in the Spacing state (logic "0") for longer than a full word transmission time (that is, the total time of the start bit + data bits + parity bits + stop bits). The BI is reset after the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. When break occurs only one zero character is loaded into the FIFO. Restarting after a break is received, requires the serial data (RXD) to be logic "1" for at least 1/2 bit time.

NOTE: Bits 1 through 4 are the error conditions that produce a Receiver Line Status Interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

Bit 5

Transmitter Holding Register Empty (THRE). Bit 5 indicates that the Serial Port is ready to accept a new character for transmission. In addition, this bit causes the Serial Port to issue an interrupt when the Transmitter Holding Register interrupt enable is set high. The THRE bit is set to a logic "1" when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic "0" whenever the CPU loads the Transmitter Holding Register. In the FIFO mode this bit is set when the XMIT FIFO is empty, it is cleared when at least 1 byte is written to the XMIT FIFO. Bit 5 is a read only bit.

Bit 6

Transmitter Empty (TEMT). Bit 6 is set to a logic "1" whenever the Transmitter Holding Register (THR) and Transmitter Shift Register (TSR) are both empty. It is reset to logic "0" whenever either the THR or TSR contains a data character. Bit 6 is a read only bit. In the FIFO mode this bit is set whenever the THR and TSR are both empty,

Bit 7

This bit is permanently set to logic "0" in the 450 mode. In the FIFO mode, this bit is set to a logic "1" when there is at least one parity error, framing error or break indication in the FIFO. This bit is cleared when the LSR is read if there are no subsequent errors in the FIFO.

MODEM STATUS REGISTER (MSR)
Address Offset = 6H, DLAB = X, READ/
WRITE

This 8 bit register provides the current state of the control lines from the MODEM (or peripheral device). In addition to this current state information, four bits of the MODEM Status Register (MSR) provide change information.

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These bits are set to logic "1" whenever a control input from the MODEM changes state. They are reset to logic "0" whenever the MODEM Status Register is read.

Bit 0
Delta Clear To Send (DCTS). Bit 0 indicates that the nCTS input to the chip has changed state since the last time the MSR was read.

Bit 1
Delta Data Set Ready (DDSR). Bit 1 indicates that the nDSR input has changed state since the last time the MSR was read.

Bit 2
Trailing Edge of Ring Indicator (TERI). Bit 2 indicates that the nRI input has changed from logic "0" to logic "1".

Bit 3
Delta Data Carrier Detect (DDCD). Bit 3 indicates that the nDCD input to the chip has changed state.

NOTE: Whenever bit 0, 1, 2, or 3 is set to a logic "1", a MODEM Status Interrupt is generated.

Bit 4
This bit is the complement of the Clear To Send (nCTS) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to nRTS in the MCR.

Bit 5
This bit is the complement of the Data Set Ready (nDSR) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to DTR in the MCR.

Bit 6
This bit is the complement of the Ring Indicator (nRI) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to OUT1 in the MCR.

Bit 7
This bit is the complement of the Data Carrier Detect (nDCD) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to OUT2 in the MCR.

SCRATCHPAD REGISTER (SCR)
Address Offset =7H, DLAB =X, READ/WRITE

This 8 bit read/write register has no effect on the operation of the Serial Port. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

PROGRAMMABLE BAUD RATE GENERATOR (AND DIVISOR LATCHES DLH, DLL)

The Serial Port contains a programmable Baud Rate Generator that is capable of taking any clock input (DC to 3 MHz) and dividing it by any divisor from 1 to 65535. This output frequency of the Baud Rate Generator is 16x the Baud rate. Two 8 bit latches store the divisor in 16 bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16 bit Baud counter is immediately loaded. This prevents long counts on initial load. If a 0 is loaded into the BRG registers the output divides the clock by the number 3. If a 1 is loaded the output is the inverse of the input oscillator. If a two is loaded the output is a divide by 2 signal with a 50% duty cycle. If a 3 or greater is loaded the output is low for 2 bits and high for the remainder of the count. The input clock to the BRG is the 24 MHz crystal divided by 13, giving a 1.8462 MHz clock.

Table 28 shows the baud rates possible with a 1.8462 MHz crystal.

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Effect of the Reset on Register File

The Reset Function Table (TABLE 29) details the effect of the Reset input on each of the registers of the Serial Port.

FIFO INTERRUPT MODE OPERATION

When the RCVR FIFO and receiver interrupts are enabled (FCR bit 0 = "1", IER bit 0 = "1"), RCVR interrupts occur as follows:

A. The receive data available interrupt will be issued when the FIFO has reached its programmed trigger level; it is cleared as soon as the FIFO drops below its programmed trigger level.

B. The IIR receive data available indication also occurs when the FIFO trigger level is reached. It is cleared when the FIFO drops below the trigger level.

C. The receiver line status interrupt (IIR=06H), has higher priority than the received data available (IIR=04H) interrupt.

D. The data ready bit (LSR bit 0)is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts occur as follows:

A. A FIFO timeout interrupt occurs if all the following conditions exist:
   – at least one character is in the FIFO
   – The most recent serial character received was longer than 4 continuous character times ago. (If 2 stop bits are programmed, the second one is included in this time delay.)
   – The most recent CPU read of the FIFO was longer than 4 continuous character times ago.
   – This will cause a maximum character received to interrupt issued delay of 160

msec at 300 BAUD with a 12 bit character.

A. Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baudrate).

B. When a timeout interrupt has occurred it is cleared and the timer reset when the CPU reads one character from the RCVR FIFO.

C. When a timeout interrupt has not occurred the timeout timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

When the XMIT FIFO and transmitter interrupts are enabled (FCR bit 0 = "1", IER bit 1 = "1"), XMIT interrupts occur as follows:

A. The transmitter holding register interrupt (02H) occurs when the XMIT FIFO is empty; it is cleared as soon as the transmitter holding register is written to (1 of 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.

B. The transmitter FIFO empty indications will be delayed 1 character time minus the last stop bit time whenever the following occurs: THRE=1 and there have not been at least two bytes at the same time in the transmitter FIFO since the last THRE=1. The transmitter interrupt after changing FCR0 will be immediate, if it is enabled.

Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

FIFO POLLED MODE OPERATION

With FCR bit 0 = "1" resetting IER bits 0, 1, 2 or 3 or all to zero puts the UART in the FIFO Polled Mode of operation. Since the RCVR and are controlled separately, either one or both can be in the polled mode of operation.

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In this mode, the user's program will check RCVR and XMITTER status via the LSR. LSR definitions for the FIFO Polled Mode are as follows:

- Bit 0=1 as long as there is one byte in the RCVR FIFO.
- Bits 1 to 4 specify which error(s) have occurred. Character error status is handled the same way as when in the interrupt mode, the IIR is not affected since EIR bit 2=0.

- Bit 5 indicates when the XMIT FIFO is empty.
- Bit 6 indicates that both the XMIT FIFO and shift register is empty.
- Bit 7 indicates whether there are any errors in the RCVR FIFO.

There is no trigger level reached or timeout condition indicated in the FIFO Polled Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

Table 28 - Baud Rates Using 1.8462 MHz Clock (24 MHz/13)

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL[1]	UART HIGH SPEED BIT[2]
50	2304	0.001	X
75	1536	-	X
110	1047	-	X
134.5	857	0.004	X
150	768	-	X
300	384	-	X
600	192	-	X
1200	96	-	X
1800	64	-	X
2000	58	0.005	X
2400	48	-	X
3600	32	-	X
4800	24	-	X
7200	16	-	X
9600	12	-	X
19200	6	-	X
38400	3	0.030	X
57600	2	0.16	X
115200	1	0.16	X
230400	32770	0.16	1
460800	32769	0.16	1

Note[1]: The percentage error for all baud rates, except where indicated otherwise, is 0.2%.
Note[2]: The UART High Speed bit is located in the device configuration space.

Table 29 - Reset Function Table

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	RESET	All bits low
Interrupt Identification Reg.	RESET	Bit 0 is high; Bits 1 - 7 low
FIFO Control	RESET	All bits low
Line Control Reg.	RESET	All bits low
MODEM Control Reg.	RESET	All bits low
Line Status Reg.	RESET	All bits low except 5, 6 high
MODEM Status Reg.	RESET	Bits 0 - 3 low; Bits 4 - 7 input
TXD1, TXD2	RESET	High
INTRPT (RCVR errs)	RESET/Read LSR	Low
INTRPT (RCVR Data Ready)	RESET/Read RBR	Low
INTRPT (THRE)	RESET/ReadIIR/Write THR	Low
OUT2B	RESET	High
RTSB	RESET	High
DTRB	RESET	High
OUT1B	RESET	High
RCVR FIFO	RESET/FCR1*FCR0/_FCR0	All Bits Low
XMIT FIFO	RESET/FCR1*FCR0/_FCR0	All Bits Low

Table 30 - Register Summary For An Individual UART Channel

REGISTER ADDRESS*	REGISTER NAME	REGISTER SYMBOL	BIT 0	BIT 1
ADDR = 0 DLAB = 0	Receive Buffer Register (Read Only)	RBR	Data Bit 0 (Note 1)	Data Bit 1
ADDR = 0 DLAB = 0	Transmitter Holding Register (Write Only)	THR	Data Bit 0	Data Bit 1
ADDR = 1 DLAB = 0	Interrupt Enable Register	IER	Enable Received Data Available Interrupt (ERDAI)	Enable Transmitter Holding Register Empty Interrupt (ETHREI)
ADDR = 2	Interrupt Ident. Register (Read Only)	IIR	"0" if Interrupt Pending	Interrupt ID Bit
ADDR = 2	FIFO Control Register (Write Only)	FCR	FIFO Enable	RCVR FIFO Reset
ADDR = 3	Line Control Register	LCR	Word Length Select Bit 0 (WLS0)	Word Length Select Bit 1 (WLS1)
ADDR = 4	MODEM Control Register	MCR	Data Terminal Ready (DTR)	Request to Send (RTS)
ADDR = 5	Line Status Register	LSR	Data Ready (DR)	Overrun Error (OE)
ADDR = 6	MODEM Status Register	MSR	Delta Clear to Send (DCTS)	Delta Data Set Ready (DDSR)
ADDR = 7	Scratch Register (Note 4)	SCR	Bit 0	Bit 1
ADDR = 0 DLAB = 1	Divisor Latch (LS)	DDL	Bit 0	Bit 1
ADDR = 1 DLAB = 1	Divisor Latch (MS)	DLM	Bit 8	Bit 9

*DLAB is Bit 7 of the Line Control Register (ADDR = 3).

Note 1: Bit 0 is the least significant bit. It is the first bit serially transmitted or received.
Note 2: When operating in the XT mode, this bit will be set any time that the transmitter shift register is empty.

Table 30 - Register Summary For An Individual UART Channel (continued)

BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
Data Bit 2	Data Bit 3	Data Bit 4	Data Bit 5	Data Bit 6	Data Bit 7
Data Bit 2	Data Bit 3	Data Bit 4	Data Bit 5	Data Bit 6	Data Bit 7
Enable Receiver Line Status Interrupt (ELSI)	Enable MODEM Status Interrupt (EMSI)	0	0	0	0
Interrupt ID Bit	Interrupt ID Bit (Note 5)	0	0	FIFOs Enabled (Note 5)	FIFOs Enabled (Note 5)
XMIT FIFO Reset	DMA Mode Select (Note 6)	Reserved	Reserved	RCVR Trigger LSB	RCVR Trigger MSB
Number of Stop Bits (STB)	Parity Enable (PEN)	Even Parity Select (EPS)	Stick Parity	Set Break	Divisor Latch Access Bit (DLAB)
OUT1 (Note 3)	OUT2 (Note 3)	Loop	0	0	0
Parity Error (PE)	Framing Error (FE)	Break Interrupt (BI)	Transmitter Holding Register (THRE)	Transmitter Empty (TEMT) (Note 2)	Error in RCVR FIFO (Note 5)
Trailing Edge Ring Indicator (TERI)	Delta Data Carrier Detect (DDCD)	Clear to Send (CTS)	Data Set Ready (DSR)	Ring Indicator (RI)	Data Carrier Detect (DCD)
Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

Note 3: This bit no longer has a pin associated with it.
Note 4: When operating in the XT mode, this register is not available.
Note 5: These bits are always zero in the non-FIFO mode.
Note 6: Writing a one to this bit has no effect. DMA modes are not supported in this chip.

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NOTES ON SERIAL PORT OPERATION

FIFO MODE OPERATION:

GENERAL

The RCVR FIFO will hold up to 16 bytes regardless of which trigger level is selected.

TX AND RX FIFO OPERATION

The Tx portion of the UART transmits data through TXD as soon as the CPU loads a byte into the Tx FIFO. **The UART will prevent loads to the Tx FIFO if it currently holds 16 characters.** Loading to the Tx FIFO will again be enabled as soon as the next character is transferred to the Tx shift register. These capabilities account for the largely autonomous operation of the Tx.

The UART starts the above operations typically with a Tx interrupt. The chip issues a Tx interrupt whenever the Tx FIFO is empty and the Tx interrupt is enabled, except in the following instance. Assume that the Tx FIFO is empty and the CPU starts to load it. When the first byte enters the FIFO the Tx FIFO empty interrupt will transition from active too inactive. Depending on the execution speed of the service routine software, the UART may be able to transfer this byte from the FIFO to the shift register before the CPU loads another byte. If this happens, the Tx FIFO will be empty again and typically the UART's interrupt line would transition to the active state. This could cause a system with an interrupt control unit to record a Tx FIFO empty condition, even though the CPU is currently servicing that interrupt. **Therefore, after the first byte has been loaded into the FIFO the UART will wait one serial character transmission time before issuing a new Tx FIFO empty interrupt.**

This one character Tx interrupt delay will remain active until at least two bytes have been loaded into the FIFO, concurrently. When the Tx FIFO empties after this condition, the Tx interrupt will be activated without a one character delay.

Rx support functions and operation are quite different from those described for the transmitter. The Rx FIFO receives data until the number of bytes in the FIFO equals the selected interrupt trigger level. At that time if Rx interrupts are enabled, the UART will issue an interrupt to the CPU. The Rx FIFO will continue to store bytes until it holds 16 of them. It will not accept any more data when it is full. Any more data entering the Rx shift register will set the Overrun Error flag. Normally, the FIFO depth and the programmable trigger levels will give the CPU ample time to empty the Rx FIFO before an overrun occurs.

One side effect of having an Rx FIFO is that the selected interrupt trigger level may be above the data level in the FIFO. This could occur when data at the end of the block contains fewer bytes than the trigger level. No interrupt would be issued to the CPU and the data would remain in the UART. **To prevent the software from having to check for this situation the chip incorporates a timeout interrupt.**

The timeout interrupt is activated when there is a least one byte in the Rx FIFO, and neither the CPU nor the Rx shift register has accessed the Rx FIFO within 4 character times of the last byte. The timeout interrupt is cleared or reset when the CPU reads the Rx FIFO or another character enters it.

These FIFO related features allow optimization of CPU/UART transactions and are especially useful given the higher baud rate capability (256 kbaud).

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FIGURE 19 - SERIAL PORT TIMING

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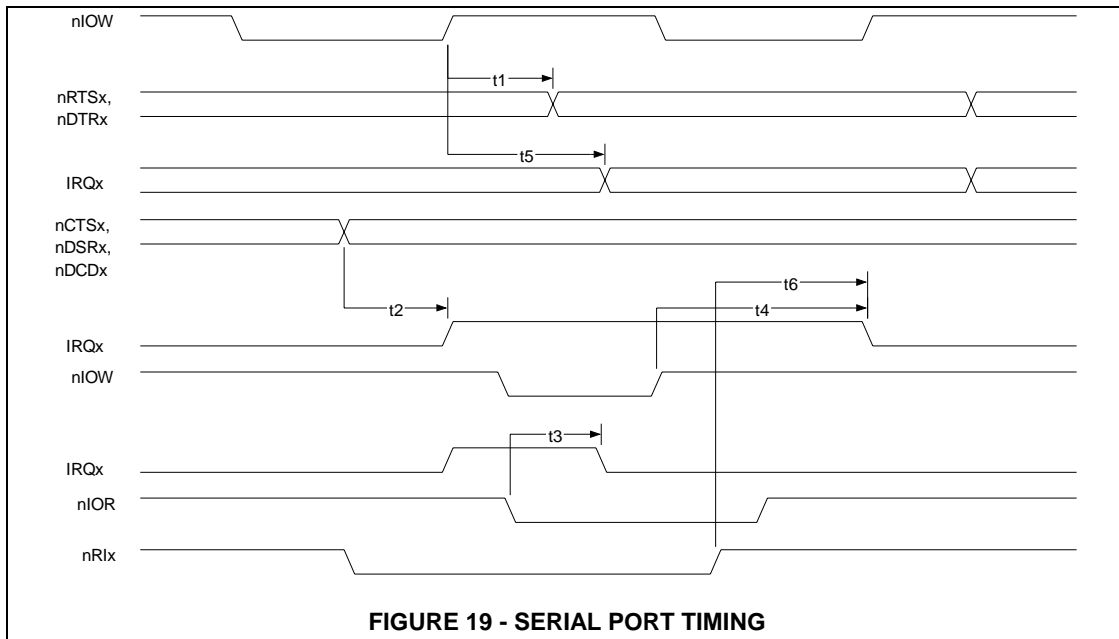
The SCE is a half-duplex synchronous serial communications controller that directs data flow between the Bus Interface I/O block and the Consumer IR (Remote Control) Encoder (Figure 20). The SCE also includes partial full-duplex loopback functionality for diagnostic testing. Bit rates from .4kbps to 100kbps are supported. All of the SCE register controls are located in the nSCE-addressable 8-bit register blocks.

FIGURE 20 - SCE BLOCK DIAGRAM
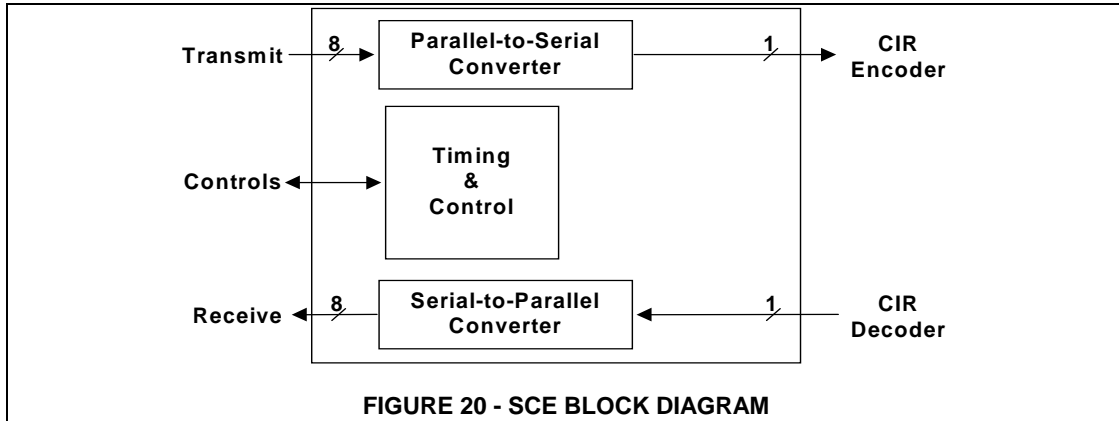
FRAMING

The SCE operates with and without framing, depending on the state of the FRAME bit in the Consumer IR Remote Control register in SCE Register Block Two. With framing implies that the SCE works with the NEC Consumer IR decoder so that the required portions of the frame message can be extracted and placed in the 32 byte FIFO. Without framing implies that the SCE operates simply as a serial-to-parallel converter for the Consumer IR (Remote Control) encoder/decoder.

ACTIVE FRAME INDICATOR

The SCE signal nActiveFrame is a PLA state variable that is synchronized to Consumer IR message frames. nActiveFrame is primarily used to trigger active frame interrupts.

Transmit
nActiveFrame goes active as soon as the Consumer IR transmitter starts modulating the SCE data stream. nActiveFrame becomes inactive as soon as the transmit register is empty.

Receive
When the FRAME bit is zero, nActiveFrame goes active as soon as the Consumer IR receiver detects the first active bit-time of infrared energy. nActiveFrame becomes inactive whenever the Consumer IR receiver is manually disabled, a DMA Terminal Count has occurred, or following a FIFO Overrun.

When the FRAME bit is one, nActive Frame goes active as soon as the NEC PPM frame format decoder detects valid data following the leader code. nActive Frame becomes inactive as soon as the receiver updates the line status register and signals an End-Of-Message following a FIFO overrun.

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FRAME ERRORS

A framing error is any bit-wide violation that occurs during the payload portion of NEC consumer remote control message frames. Payload data in this protocol always follows the leader code and includes the custom code and data code fields as shown in Figure 5.

The Frame Error bit in the SCE Line Status Register is set to "1" when a framing error occurs. The Frame Error bit will not be set if framing errors occur when the FRAME bit in the SCE Consumer IR Remote Control Register is inactive ("0").

The bit-wide violations that produce framing errors are defined as the continuous presence of carrier for more than two or more bit cells, or the continuous absence of carrier for four or more bit cells. Note: bit cells are determined by the SCE CIR Bit Rate Divider register. For example; if the Bit Rate Divider is programmed for the NEC format shown in Figure 5 when the FRAME bit is "1", then the Frame Error bit will be set if carrier is detected for 1.125ms or greater, or if no carrier is detected for 2.25ms or greater.

Note: It is possible for the FIFO to be empty with the Frame Error bit set at the end of an invalid NEC remote control message frame because the payload data in messages with framing errors will either be ignored or passed to the FIFO depending on the data pattern and the frequency of violations.

BUS INTERFACE I/O

The Bus Interface I/O block contains a 32-byte FIFO, DMA/Interrupt logic, and multiplexers to control access to the FIFO and the ISA Bus (Figure 21).

The Databus Multiplexer provides exclusive ISA Bus access to either the 16C550A UART or the CIrCC SCE depending on the state of Block Control bits. Disabled blocks are disconnected from the ISA Bus.

Loopback	Transmit	Function
0	0	FIFO In to SCE Rx
		FIFO Out to Host Bus
0	1	FIFO In to Host Bus
		FIFO Out to SCE Tx
1	X	FIFO In to SCE Rx
		FIFO Out to SCE Tx
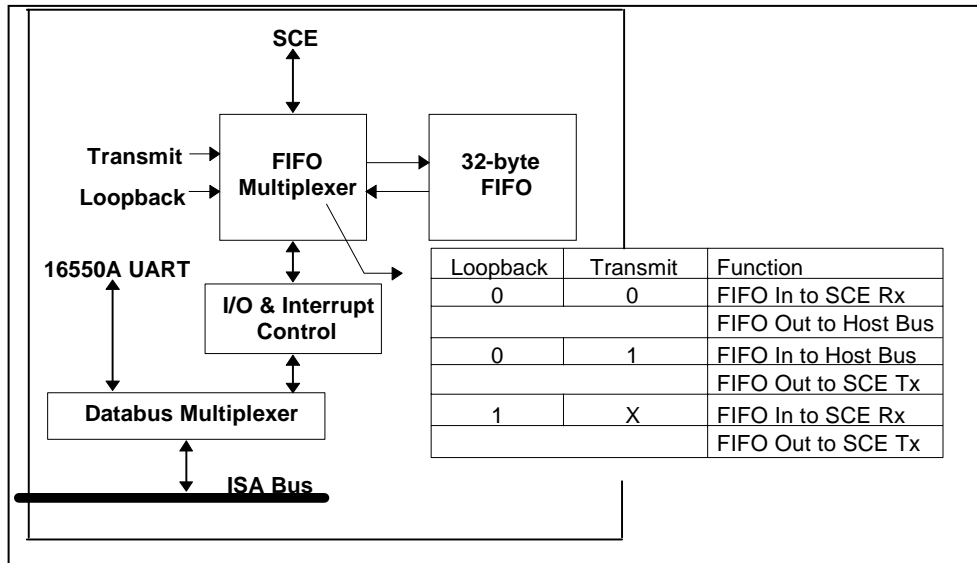
FIGURE 21 - BUS INTERFACE I/O BLOCK

FIFO MULTIPLEXER

SCE FIFO Access

The FIFO Multiplexer controls the configuration of the SCE FIFO in the Bus Interface I/O Block. This configuration can be inferred from the state of the SCE Modes bits in Line Control Register B. When the transmit/receive modes are disabled, or the transmit mode is enabled, the FIFO is configured for transmit, otherwise, the FIFO is configured for receive. The signal Transmit in Figure 21, above, can be satisfied by the inverse of the SCE Modes msb; e.g., nD7.

HOST FIFO Access

The host always has read access to the FIFO, regardless of the state of the SCE Modes bits, or the Loopback bit. The host has write access to the FIFO when the Loopback bit is inactive and the transmit/receive modes are disabled or the Transmit mode is enabled.

32-BYTE SCE FIFO

FIFO Timing & Controls

The FIFO requires interleaved access timing to allow simultaneous FIFO data reads and data

writes. This is required both for normal operation with asynchronous host/SCE access timing, and during loopback tests with synchronous SCE-only access timing where the FIFO is simultaneously used for transmit and receive. FIFO controls include, separate read/ write lines, FIFO Full and FIFO Not Empty flags, Reset, FIFO Threshold, and Interrupt.

FIFO Threshold

The SCE FIFO Threshold generates programmed I/O service requests to accommodate systems with widely varying I/O response times. FIFO Threshold values typically reflect the overall I/O response characteristics of a system. The same threshold value can be used for both I/O read and I/O write cases. During DMA operations, the FIFO Threshold is only used to trigger the SCE transmitter. **NOTE:** the DMA controller will fill the FIFO until the FIFO Threshold has been exceeded before the transmitter is enabled.

The FIFO Threshold value is programmable from 0 to 31. The FIFO Threshold Register, located in Register Block One, Address Two, contains the FIFO Threshold value. Low threshold values result in longer periods of time between service requests because more of the FIFO is utilized before the request is issued. Systems that program low threshold values must typically provide fast response times to these requests; i.e., high performance systems that move I/O data quickly.

High threshold values are used in "sluggish" systems with long service request latencies. Low performance systems typically take longer to move I/O data and require more frequent I/O service. For systems that program high FIFO threshold values, much less of the FIFO is utilized before service requests are issued.

Receive Threshold

Once the FIFO Interrupt is enabled, Receive Service Requests (RxServReq), i.e. data transfers from the FIFO to the host, are generated whenever there are 32 minus the FIFO Threshold value or more data bytes in the FIFO, given by:

$$RxServReq \geq 32 - \text{FIFO Threshold}$$

For example, if the FIFO threshold value is 12, RxServReq will be active whenever there are 20 to 32 data bytes in the FIFO. If the FIFO Threshold is 0, RxServReq will be active whenever the FIFO is full. If the FIFO Threshold is 31, RxServReq will be active whenever the FIFO is not empty.

Transmit Threshold

Once the FIFO Interrupt is enabled, Transmit Service Requests (TxServReq), i.e. data transfers from the host to the FIFO, are generated whenever there are FIFO Threshold value or fewer data bytes in the FIFO, given by:

$$TxServReq \leq \text{FIFO Threshold}$$

For example, if the FIFO Threshold value is 12, TxServReq will be active whenever there are 12 or less data bytes in the FIFO. If the FIFO Threshold is 0, TxServReq will be active whenever the FIFO is empty. If the FIFO Threshold is 31, TxServReq will be active whenever the FIFO is not full.

FIFO Interrupt

The FIFO Interrupt becomes active whenever the FIFO Interrupt Enable is active and either TxServReq or RxServReq is active. When FIFO Interrupt Enable becomes inactive, the FIFO Interrupt goes inactive.

For example, the FIFO Interrupt will become active during a transmit operation if the FIFO Threshold is fifty, the FIFO Interrupt Enable is active, and there are from one to fifty data bytes in the FIFO (Figure 22).

In Figure 22, notice that five bytes are written to the FIFO every time a service request is answered. The third request occurs as soon as the FIFO Interrupt Enable is activated because the five bytes written to the FIFO following the

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second service request was not enough data to exceed the FIFO Threshold given the long interrupt latency.

FIGURE 22 - FIFO INTERRUPT EXAMPLE
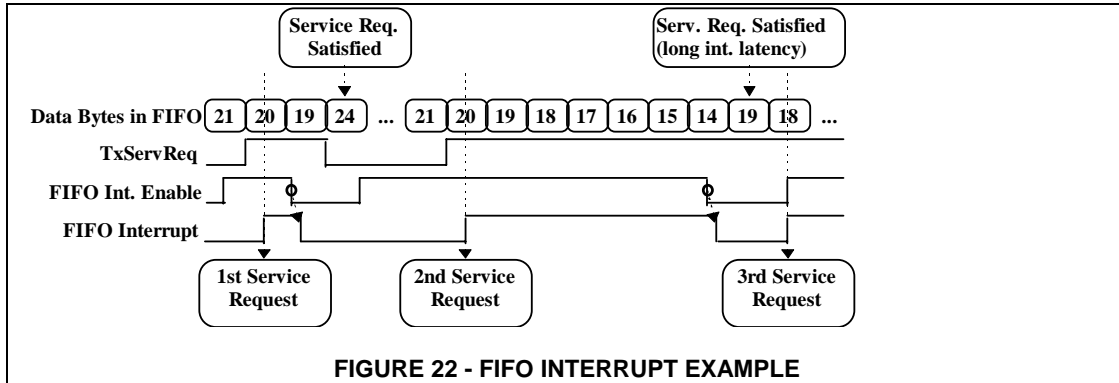
DMA

The DMA channel works in Single-Byte and Burst (Demand) Mode. AEN is high during DMA transfers. The DMA controls are located in SCE Configuration Register B. When the DMA Enable bit (D0) is one, DMA is enabled. The DMA Burst Mode bit (D1) controls the DMA mode. DRQ is further gated by the SCE Modes bits; e.g., DRQ can only be enabled if either Transmit or Receive mode has been enabled. During transmit DRQ remains active as long as the FIFO is not full until TC. During receive DRQ remains active as long as the FIFO is not empty until TC.

Single-Byte Mode

Single-Byte mode is enabled by resetting the DMA Burst bit in SCE Configuration Register B. Single-Byte DMA transfers one data byte for each DRQ (Figure 23). Terminal Count occurs only once, during the last byte of data block.

FIGURE 23 - DMA SINGLE-BYTE MODE TIMING
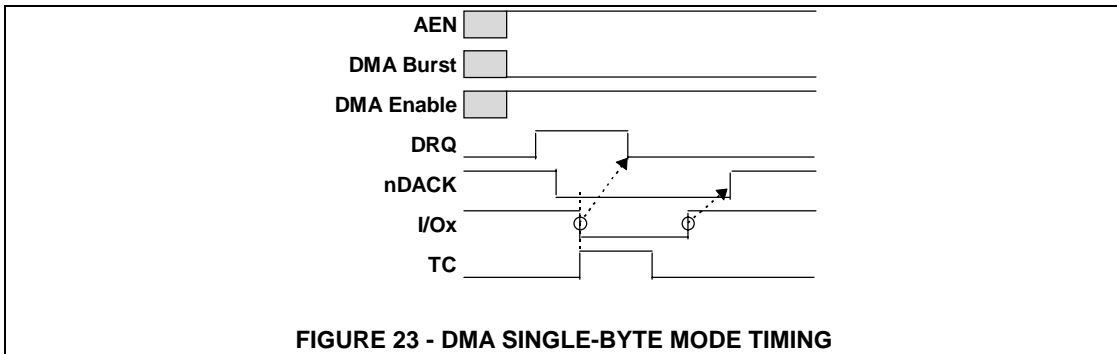
Burst (Demand) Mode

DMA Burst mode is enabled by setting the DMA Burst bit in SCE Configuration Register B. Demand Mode DMA transfers up to 32 data bytes for each DRQ (Figure 24). The CIrCC guarantees that DRQ relinquishes the ISA bus after thirty-two DMA I/O read or write cycles to allow for memory refresh.
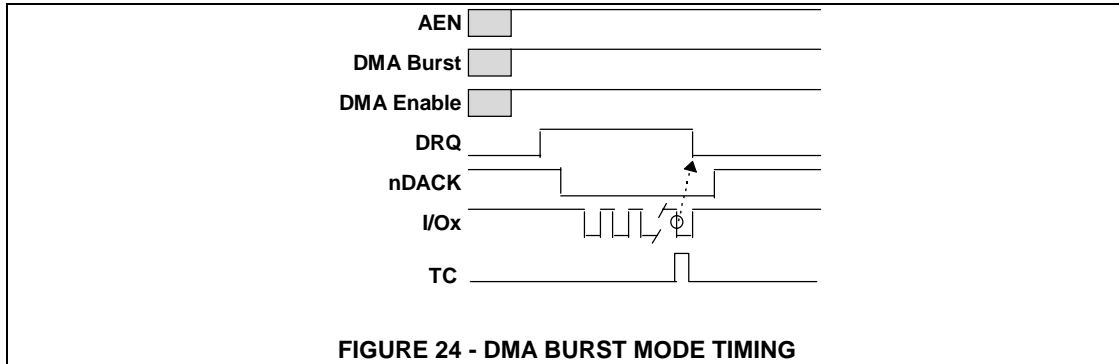
FIGURE 24 - DMA BURST MODE TIMING

DMA Refresh Counter

The DMA Refresh Counter is used to prevent DRQ from staying active for more than 4, 8, 16, or 32 I/O cycles at a time (see DMA Refresh Count, bits 0-1, on page 34).

The counter is stopped and preloaded whenever DRQ is not active. Once DRQ becomes active, the counter decrements until zero-count or DRQ is deactivated.

In Demand Mode, the count-zero condition always clears DRQ and triggers a Refresh Interval. The Refresh Interval remains active for 350ns following an inactive nDACK (Figure 25). If there is more data to transfer, DRQ goes active again and the cycle repeats.

Single Byte Mode DMA does not use the DMA Refresh Counter. Table 22 illustrates the DMA Refresh Count bit encoding; e.g., if D[1:0] = 0,0, the DMA Refresh Counter will prevent DRQ from staying active for more than four I/O read/write cycles at a time.
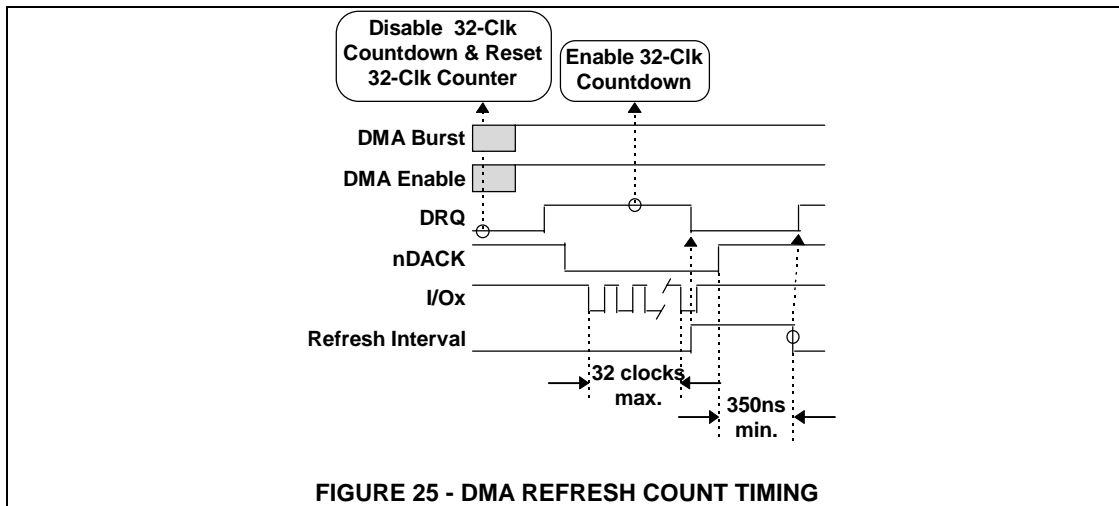
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FIGURE 25 - DMA REFRESH COUNT TIMING

DRQ Control

In DMA Burst Mode, DRQ remains active until the entire DMA data block has been transferred, as indicated by DMA Terminal Count (TC). The internal FIFO Full signal can temporarily deactivate DRQ if the DMA block has not been completely transferred but there is no room left in the FIFO for more data. As soon as the FIFO Full becomes inactive, DRQ is reasserted. The internal Refresh Interval signal can also temporarily deactivate DRQ (see the DMA Refresh Counter on page 59).

FIGURE 26 - DMA BURST MODE TRANSMIT TIMING
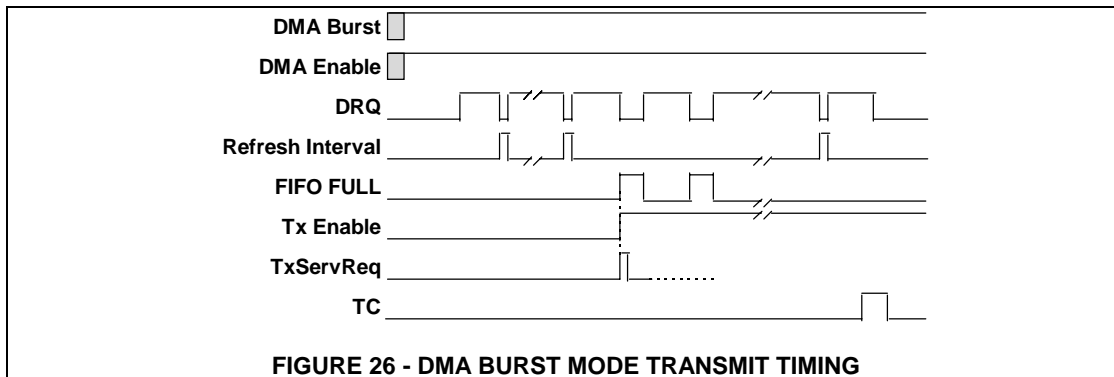
Burst Mode Receive

DRQ Control

In DMA Burst Mode, DRQ remains active until the entire DMA data block has been transferred, as indicated by DMA Terminal Count (TC). Since the FIFO Threshold is not used for DMA transfer cycles, DRQ is asserted as soon as FIFO Not Empty is true. FIFO Not Empty can temporarily deactivate DRQ if the DMA block has not been completely transferred but there is no data left in the FIFO to transfer. As soon as FIFO Not Empty becomes true, DRQ is reasserted. The internal refresh counter can also temporarily deactivate DRQ (see the DMA Refresh Counter on page 59).

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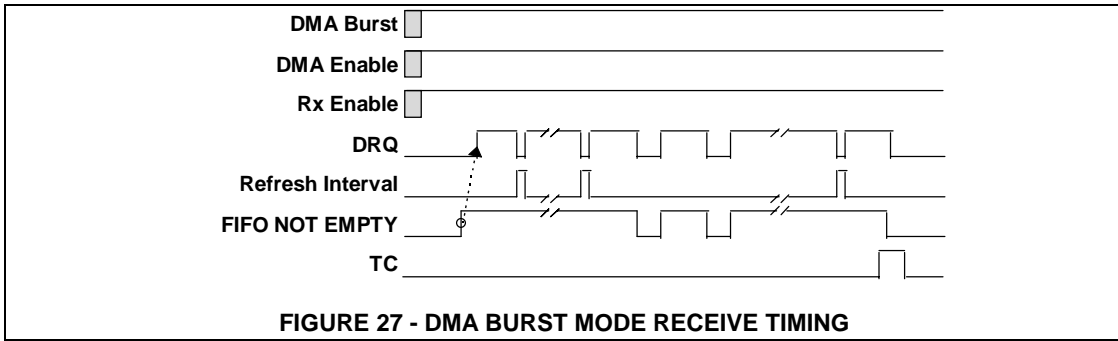
FIGURE 27 - DMA BURST MODE RECEIVE TIMING

PROGRAMMED I/O

Programmed I/O mode is selected when the DMA Enable bit in SCE Configuration Register B is zero. The CIrCC also supports String Move timing which is a block-mode programmed I/O operation that utilizes IOCHRDY to control the transfer (Figure 28). String Move mode is selected when the String Move bit in SCE Configuration Register B is one.
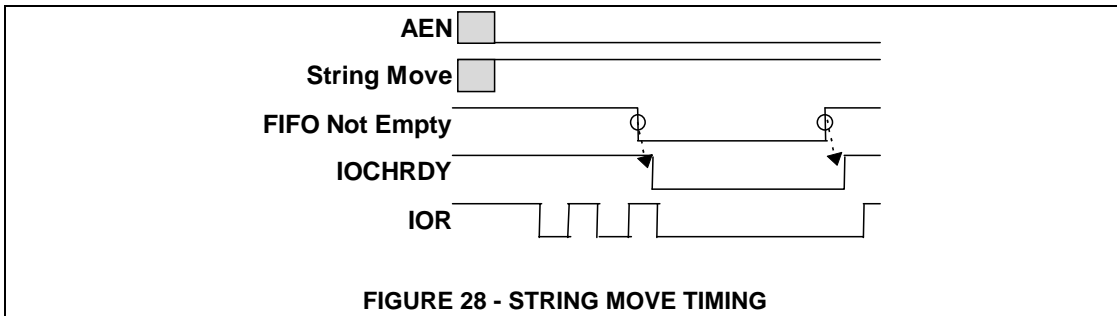
FIGURE 28 - STRING MOVE TIMING

Polling Interface

Programmed I/O without IOCHRDY requires polling the FIFO status flags before reading or writing FIFO data. The Receiver interface depends upon the FIFO Not Empty flag. If FIFO Not Empty is true, there is read data available in the FIFO (Figure 29). The Transmitter interface depends upon the FIFO Full flag. If FIFO Full is false, there is room for write data in the FIFO (Figure 30).

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FIGURE 29 - PROGRAMMED I/O READ TIMING

FIGURE 30 - PROGRAMMED I/O WRITE TIMING
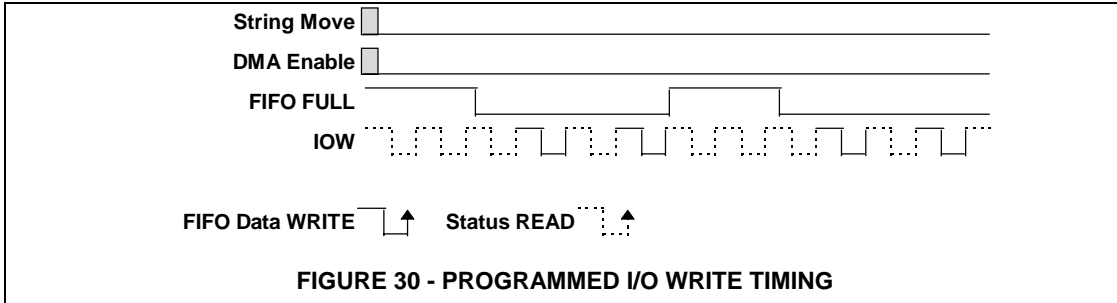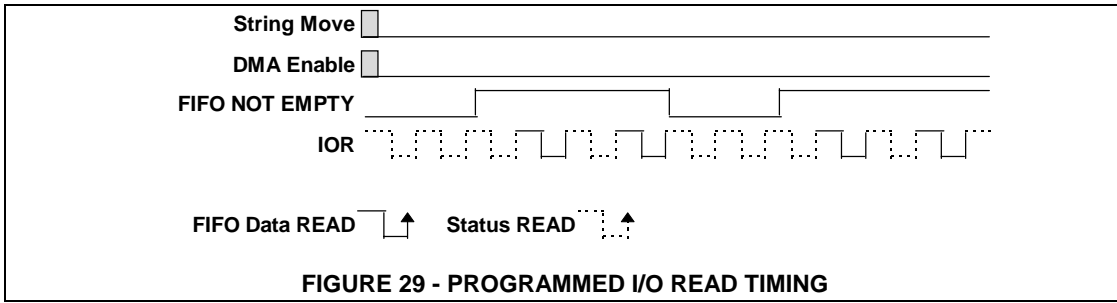
FIFO Interrupt Interface

Transmit

Transmitting messages with Programmed I/O using FIFO Interrupt requires writing a fixed number of data bytes, usually related to the threshold, whenever the FIFO Interrupt becomes active. An appropriate FIFO Threshold value allows the host to efficiently satsify the FIFO service requests until the message transmission is complete. For slow systems, the FIFO can be manually filled with transmit data before the transmitter is enabled. **NOTE:** The FIFO will automatically request service before the transmitter is activated if the FIFO Threshold is greater than zero.

String Move
DMA Enable **String Move**
Tx Enable **DMA Enable**
IOW
Rx Enable
TxServReq **IOR**
FIFO Int. Enable **RxServReq**
FIFO Interrupt **FIFO Int. Enable**
Data Done **FIFO Interrupt**
EOM Interrupt **EOM Interrupt**

FIGURE 31 INTERRUPT DRIVEN PROGRAMMED I/O TRANSMIT TIMING
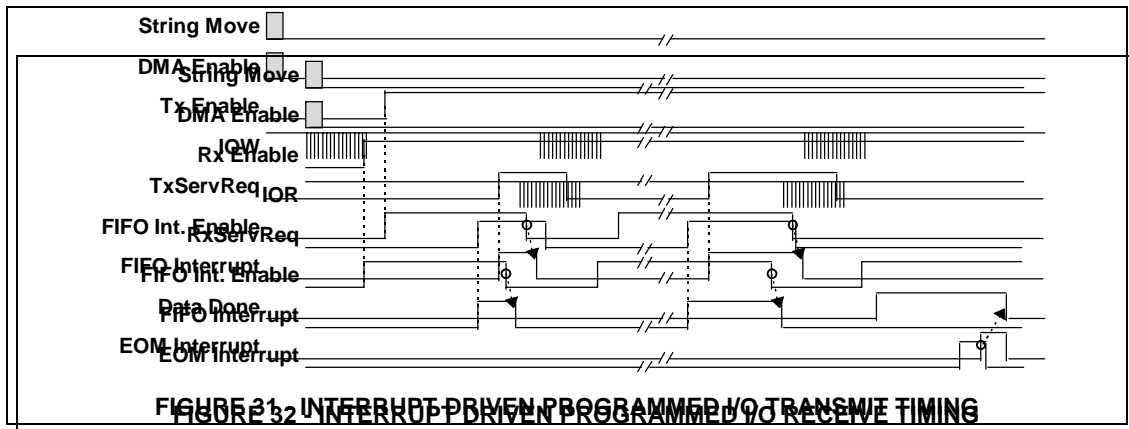
FIGURE 32 INTERRUP T DRIVEN PROGRAMMED I/O RECEIVE TIMING

Receive

Receiving messages with Programmed I/O using FIFO Interrupt requires reading a fixed number of data bytes, usually related to the threshold, whenever the FIFO Interrupt becomes active. An appropriate FIFO Threshold value allows the host to efficiently satsify the FIFO service requests until the message reception is complete.

IOCHRDY Time-out

In programmed I/O mode when AEN = low and String Move = active, IOCHRDY can be used to slightly extend the access cycle if the FIFO is temporarily unable to fulfill the transfer request (Figure 33). If IOCHRDY remains inactive for more than 10Fs, a time-out error occurs and subsequent IOCHRDY cycles are prevented until the string move bit is specifically reactivated. Because of the 10Fs IOCHRDY time-out, it is recommended that string move timing only be used for 1.152 Mbps transfers and above.

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FIGURE 33 - VALID I/O READ READY CYCLE
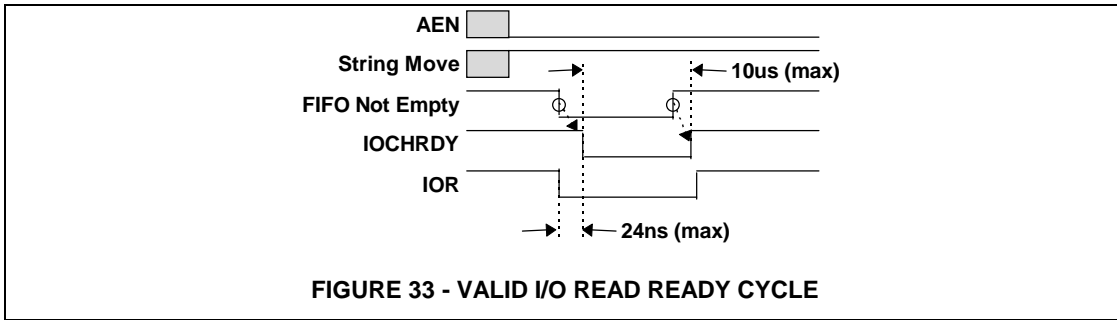
IOCHRDY Timer

The 10Fs IOCHRDY Timer is initialized when IOCHRDY is active. The timer count sequence is activated when IOCHRDY goes inactive. If IOCHRDY becomes active before the 10Fs time-out has elapsed, the timer is stopped and the count is re-initialized. If IOCHRDY is still inactive when the 10Fs time-out occurs, the timer stops, the time-out error bit is set, IOCHRDY is re-asserted, and the string move bit is reset (Figure 34).

FIGURE 34 - IOCHRDY 10FS TIME-OUT
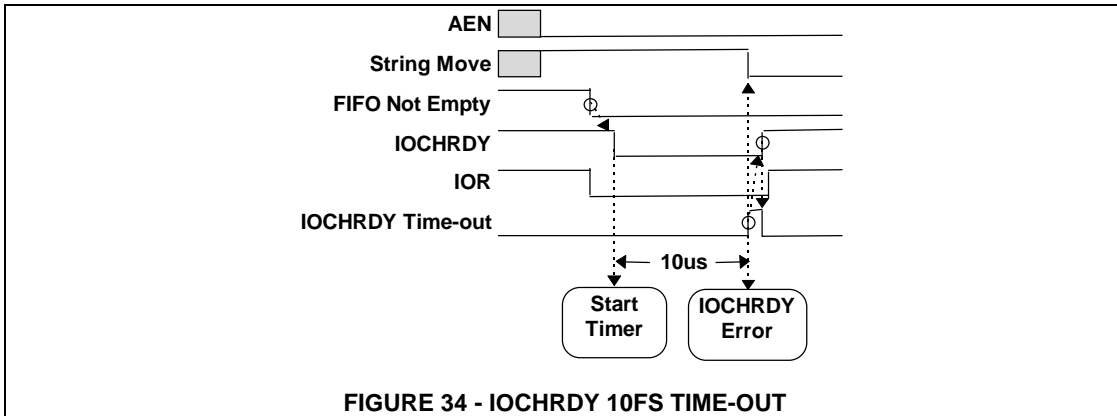
Zero Wait State Support

nSRDY

nSRDY can be driven by the CIrCC to indicate that an access cycle shorter than the standard I/O cycle can be executed. **NOTE**: the names nSRDY & nNOWS can be used interchangeably. nSRDY is enabled by the No Wait bit in SCE Configuration Register B. When No Wait is one, nSRDY goes active following the trailing edge of the ISA I/O command and inactive following the rising edge (Figure 35). nSRDY is suppressed during DMA & refresh cycles, i.e. when AEN is active, or when IOCHRDY is inactive. Zero Wait State support is only available when the SCE is enabled.

FIGURE 35 - nSRDY TIMING
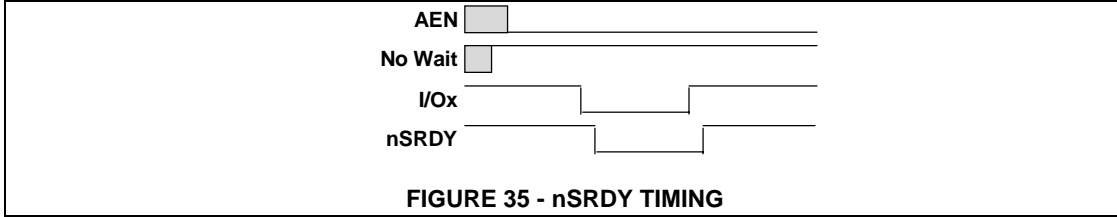
The Interaction of nSRDY and IOCHRDY determine the three types of ISA access cycles: no-wait-state cycle, standard cycle, ready cycle (Table 31). **NOTE:** An inactive IOCHRDY suppresses nSRDY.

Table 31 - nSRDY and IOCHRDY Interaction

nSRDY	IOCHRDY	DESCRIPTION
active	active	No-wait-state Cycle (shortest length)
inactive	active	Standard Cycle (mean length)
x	inactive	Ready Cycle (longest length)

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OUTPUT MULTIPLEXER

The Output Multiplexer routes the active encoder/decoder to one of three CIrCC serial communications ports. There are no restrictions on any of these connections other than Rx/Tx source pairs go to the same destination (Figure 36). Descriptions of the Block Control, Output Mux, and Aux IR signals can be found in the SCE Configuration Registers in Register Block One.

The Rx and Tx Polarity controls determine the active states for the IR port signals, see SCE Configuration Register A. The state of inactive IR outputs depends upon the Tx Polarity bit; e.g., if Tx Polarity is one (default), inactive outputs will be 0. Routing for the COM Port flow-control signals is fixed. When the COM Port is inactive, the flow-control signals behave according to the current SMSC 16C550A serial port specification. **NOTE:** The Tx/Rx Polarity bits do not apply when COM mode is selected.
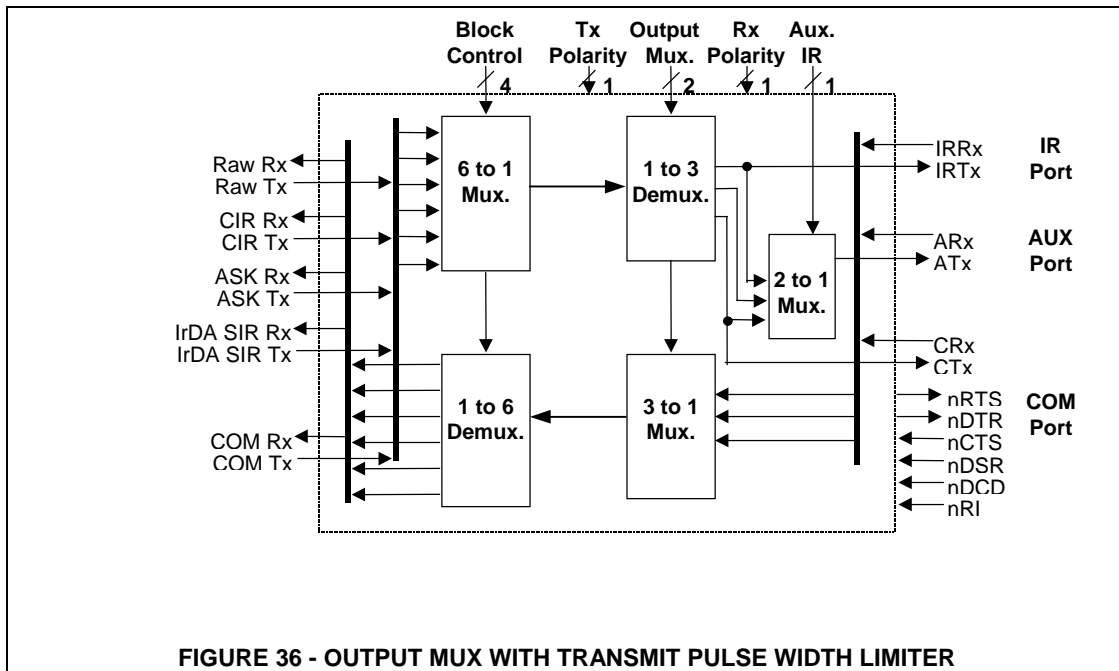
FIGURE 36 - OUTPUT MUX WITH TRANSMIT PULSE WIDTH LIMITER

NOTE: This figure is for illustration purposes only and is not intended to suggest specific implementation details.

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TRANSMIT PULSE WIDTH LIMIT

The Transmit Pulse Width Limit reduces the risk of thermal damage to the transmit LED during message transactions or from the unpredictable affects that can occur during a power-on-reset. The Transmit Pulse Width Limit hardware is controlled by the TX PW LIMIT bit (see Tx PW Limit, bit 6, on page 33). The Transmit Pulse Width Limit hardware must apply to all encoders, particularly the Consumer IR Encoder and the RAW Mode encoder (Figure 36).

When the TX PW LIMIT bit is high, active Tx levels trigger the Transmit Pulse Width Limit hardware. If an active Tx pulse goes inactive before 100Fs, the Transmit Pulse Width Limit hardware is deactivated until the next active Tx level. If the transmit pulse exceeds 100Fs, the hardware deactivates Tx for 300Fs and cannot re-activate it until the input to the Transmit Pulse Width Limit hardware has gone inactive and active again (Figure 37). When the TX PW LIMIT bit is low, the Transmit Pulse Width Limit hardware is disabled.

APPLICATION NOTE: The Transmit Pulse Width Limit can seriously distort low frequency Consumer IR carriers ($\leq$ 5kHz) or unmodulated low frequency Consumer IR bit rates.

TX PW LIMIT IN

TX PW LIMIT OUT

← 100us → ← 300us →

FIGURE 37 - TRANSMIT PULSE WIDTH LIMIT EXAMPLE

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CHIP-LEVEL ClrCC ADDRESSING SUPPORT

ClrCC Register addressing is controlled at the chip level. Both the ACE bank select, nACE, and the SCE bank select, nSCE, are decoded at the chip level from the host address bus to access data in the ClrCC register banks (Figure 38). Figure 38 illustrates a chip-level ClrCC address decoder using a base address of '400'hex.
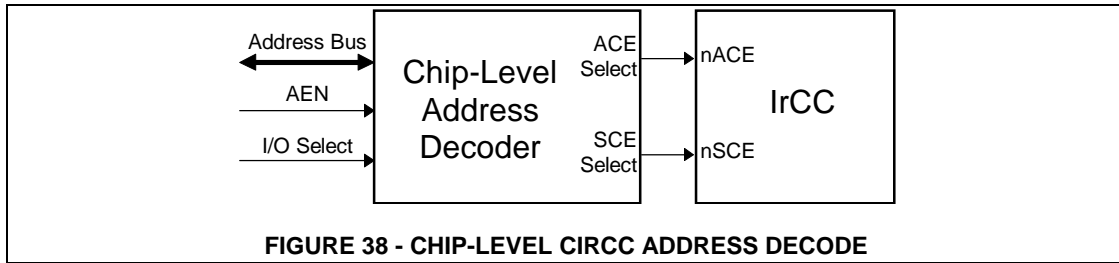
FIGURE 38 - CHIP-LEVEL CIRCC ADDRESS DECODE

Table 32 - ClrCC Address Decode at '400'hex

HEX ADDRESS	nACE	nSCE	DESCRIPTION
000 - 3FF	1	1	ClrCC registers not accessible
400 - 407	0	1	ACE UART registers enabled
408 - 40F	1	0	SCE registers enabled
410 - 4FF	1	1	ClrCC registers not accessible

AC TIMING

IR Rx Pulse Rejection

Table 33 - IR Rx Pulse Rejection

ENCODER	PULSE REJECTION
IrDA SIR	≤500ns
Consumer IR	≤166ns

RX PULSE JITTER TOLERANCE

Table 34 - RX Pulse Jitter Tolerance

	MAX JITTER
115.2 kbps	400ns
9.6 kbps	5Fs

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

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