150mA/1.2V CMOS LDO Regulator with Power Good

Features

- LDO regulator with Power Good
- No capacitor required on the LDO output
- Power Good (PG) control signal
- Regulated 1.2V output
- 150mA output current
- Low quiescent operating current (90µA typical)
- "Zero" disable mode current
- Foldback current limiting protection
- Thermal shutdown protection
- SOT23-5 package
- Micrel MIC5258, MIC5268 compatible pinout
- Lead-free version available

Applications

- Pentium® 4 Motherboards
- PC Cards
- Peripheral Adapter Cards

Product Description

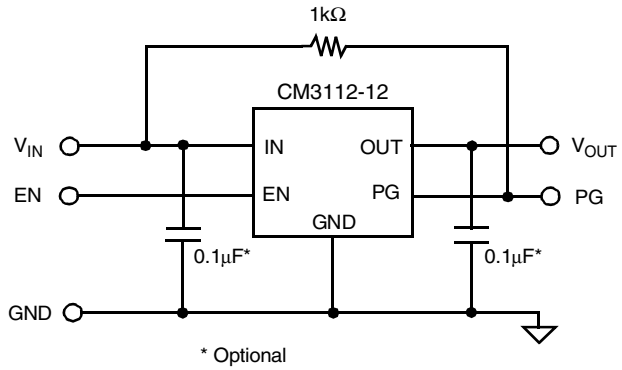
The CM3112-12 is a low quiescent current (90uA) regulator that delivers up to 150mA of load current at a fixed 1.2V output. All the necessary circuitry has been included to deliver a 50Ω power good signal (open drain) which remains for 5ms after the output has exceeded 90% (typ) of its nominal level.

A dedicated control input (EN, Active High) has been included for power-up sequencing flexibility. When this input is taken low, the regulator is disabled. In this state, the supply current will drop to near zero. An internal discharge MOSFET (500Ω) resistance will force the output to ground whenever the device has been shutdown.

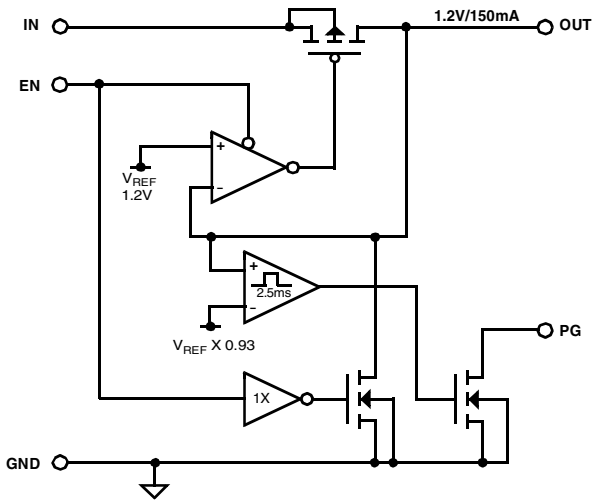
The CM3112-12 is fully protected, offering both overload current limiting and high temperature thermal shutdown.

Housed in a tiny SOT23 package, the device is ideal for space critical applications and is also available with optional lead-free finishing.

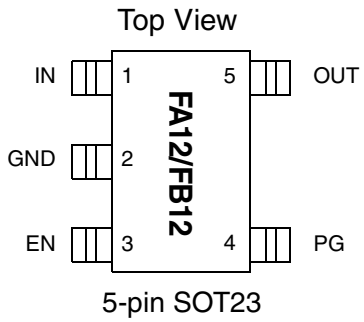
Typical Application Circuit



Simplified Electrical Schematic



PACKAGE / PINOUT DIAGRAM



Note: This drawing is not to scale.

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	IN	Positive input voltage for the regulator. The internal loading on this input is typically 300µA whenever the regulator is enabled, and less than 10µA when the regulator is disabled. If the IN pin is within a few inches of the main input filter, a capacitor may not be necessary. Otherwise an input filter capacitor (C_{IN}) of 0.1uF to 1uF will ensure adequate filtering.
2	GND	The negative reference for all voltages.
3	EN	Enable/shutdown input. When EN is asserted high ($V_{EN} \geq 1.6V$), the regulator is enabled. When EN is asserted low ($V_{EN} \leq 0.4V$), the regulator's series pass transistor is forced into a high impedance mode and an internal discharge resistance (500Ω) is applied to the output to quickly reduce the output voltage to 0 volts.
4	PG	Power Good output. This is an open drain output and functions as a supply voltage supervisor for the output voltage. It is asserted low when the output falls below 84% of its nominal value. This output becomes inactive when (EN > 1.5V), (2.5V < V_{IN} < 5.5V) and (V_{OUT} > 97% of V_{OUTNOM}), all of which are valid for more than 1-10ms.
5	OUT	The regulated voltage output. Although an output capacitor is not necessary for stable regulator operation, a optional 0.1uF capacitor can be used to provide an added measure of output stability.

Ordering Information

PART NUMBERING INFORMATION

			Standard Finish		Lead-free Finish	
Regulator	Pins	Package	Ordering Part Number[1]	Part Marking	Ordering Part Number[1]	Part Marking
CM3112-12	5	SOT23-5	CM3112-12ST	FA12	CM3112-12SO	FB12

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	**RATING**	**UNITS**
ESD Protection (HBM)	±2000	V
Pin Voltages V_{IN} V_{OUT} V_{EN}	 [GND - 0.6] to +6.0 [GND - 0.6] to [V_{IN}+0.6] [GND - 0.6] to [V_{IN}+0.6]	 V V V
Storage Temperature Range	-40 to +150	°C
Operating Temperature Range Ambient Junction	 0 to +70 0 to +150	 °C °C
Power Dissipation (See note 1)	Internally Limited	W

Note 1: The power rating is based on a printed circuit board heat spreading capability equivalent to 2 square inches of copper connected to the GND pins. Typical multi-layer boards using power plane construction will provide this heat spreading ability without the need for additional dedicated copper area. Please consult with factory for thermal evaluation assistance.

STANDARD OPERATING CONDITIONS		
PARAMETER	**VALUE**	**UNITS**
V_{IN}	2.5 to 5.5	V
Ambient Operating Temperature Range	0 to +70	°C
Load Current	0 to 150	mA
C_{OUT}	0 to 10	µF

ELECTRICAL OPERATING CHARACTERISTICS (SEE NOTE 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OUT}	Output Voltage Accuracy	I_{LOAD} = 5mA, V_{IN} = 3.3V	-2 **-3**		2 **3**	% **%**
V_{OUT}	Output Voltage	5mA ≤ I_{LOAD} ≤ 150mA, 3.135V ≤ V_{IN} ≤ 5.5V	-4 **-5**		4 **5**	% **%**
$V_{R\ LOAD}$	Load Regulation	5mA ≤ I_{LOAD} ≤ 100mA			0.5 **0.7**	% **%**
$V_{R\ LINE}$	Line Regulation	I_{LOAD} = 5mA; 2.5V ≤ V_{IN} ≤ 5.5V			0.1 **0.15**	%/V **%/V**
R_{DROP}	Dropout Resistance	V_{IN} = 2.7V			10	Ω
I_{LIM}	Overload Current Limit		**160**	400		mA
I_{SC}	Short Circuit Current Limit	V_{OUT} < 0.5V		150		mA
R_{DISCH}	Discharge Resistance	EN tied to GND		500		Ω
I_{GND}	Ground Current	Regulator Enabled (EN=V_{IN}); I_{LOAD}= 0mA Regulator Enabled (EN=V_{IN}); I_{LOAD}= 150mA Regulator Disabled (EN=GND); (Disable Mode)		90 100 0.01	150 200 10	µA µA µA
V_{EN}	EN Input Logic High Threshold	Regulator Enabled, V_{IN} = 5.5V	1.6			V
V_{DIS}	EN Input Logic Low Threshold	Regulator Disabled, V_{IN} = 5.5V			0.4	V
I_{EN}	Enable Input Current			0.01	10	µA
V_{PGL}	Power Good Low Threshold	% of V_{OUT} (PG ON)	84			%
V_{PGH}	Power Good High Threshold	% of V_{OUT} (PG OFF)			97	%
V_{OL}	Power Good Logic "0" Voltage	I_L= 2mA; Fault Condition		0.05	**0.1**	V
I_{PG}	Power Good Leakage Current	Power Good Off; V_{PG} = 5.5V		0.01	**50**	µA
D_{PGD} D_{PGA}	Power Good Delay Time To de-assert PG To assert PG	2.5V ≤ V_{IN} ≤ 5.5V (applies to D_{PGD} only)	1		**10** **1**	**mS** **mS**

Note 1: B**old values indicate 0 °C < T_J <125 °C.**

Timing Diagram

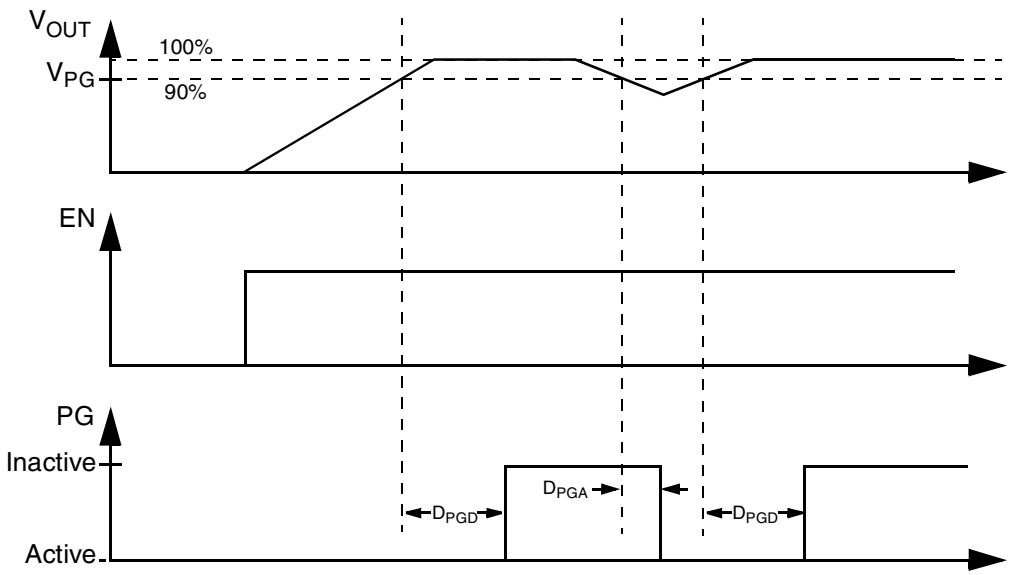


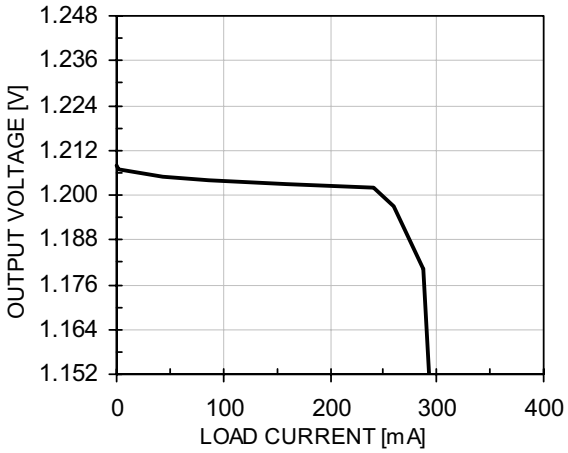
Figure 1. Power Good Delay Timing

Performance Information

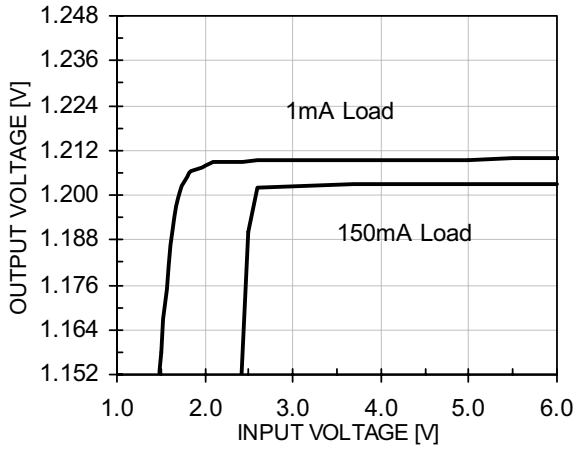
CM3112 Typical DC Characteristics (nominal conditions unless specified otherwise)

Nominal Conditions: V_{IN} = 3.3V, I_{LOAD}=1mA, no C_{OUT}

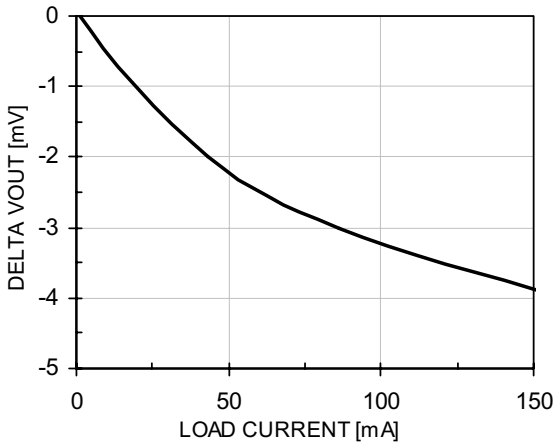
Load Regulation



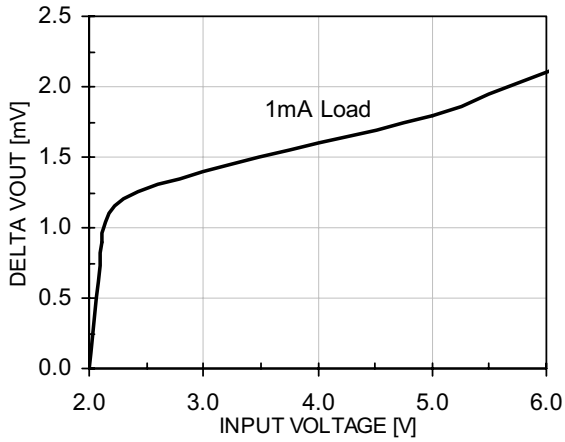
Line Regulation (1% and 100% rated load)



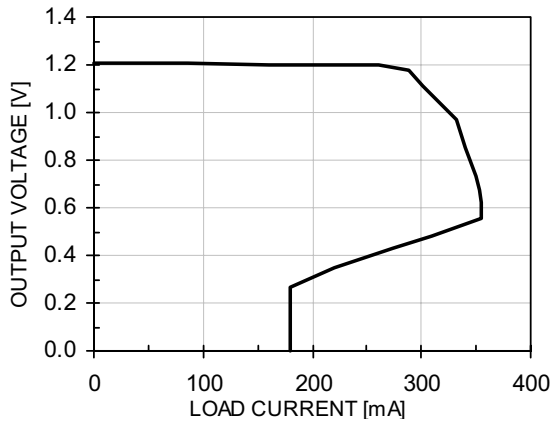
Load Regulation (Close-up)



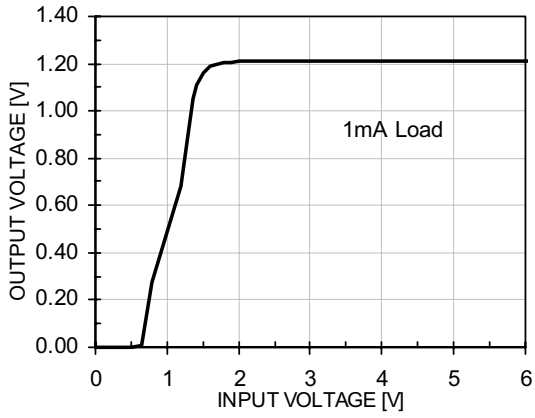
Line Regulation (Close-up)



Foldback Current Limiting



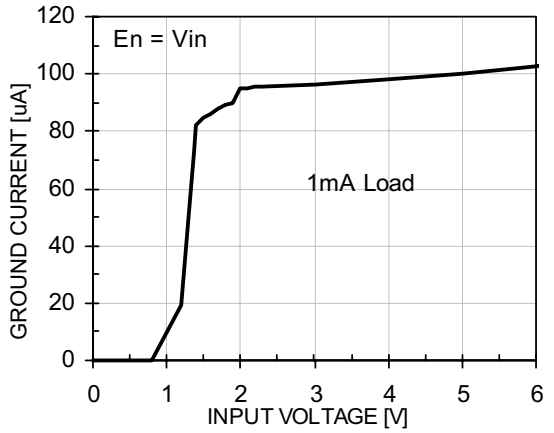
Line Regulation



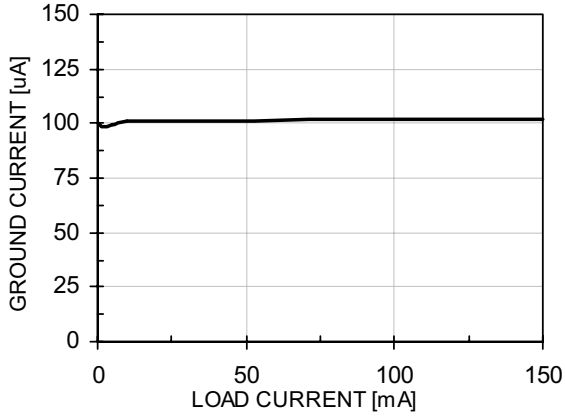
Performance Information (cont'd)

CM3112 Typical DC Characteristics (cont'd, nominal conditions unless specified otherwise)

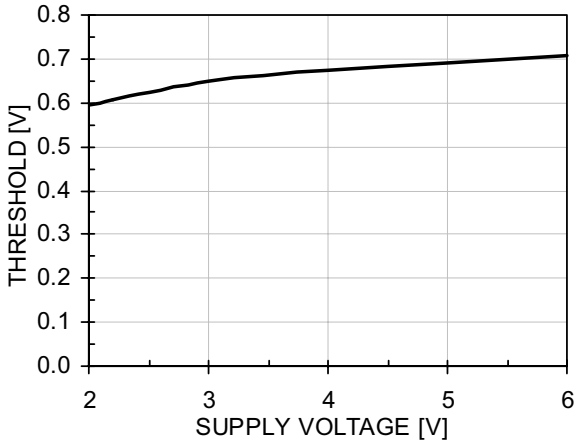
Ground Current Vs. Supply Voltage



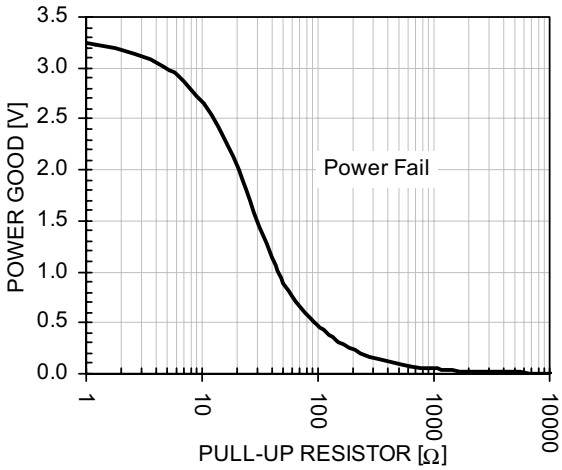
Ground Current Vs. Load Current



Enable Threshold Vs. Supply Voltage



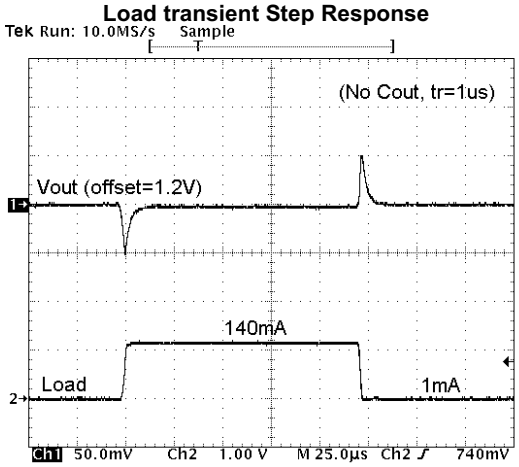
Power Good Voltage Vs. Pull-Up Resistor



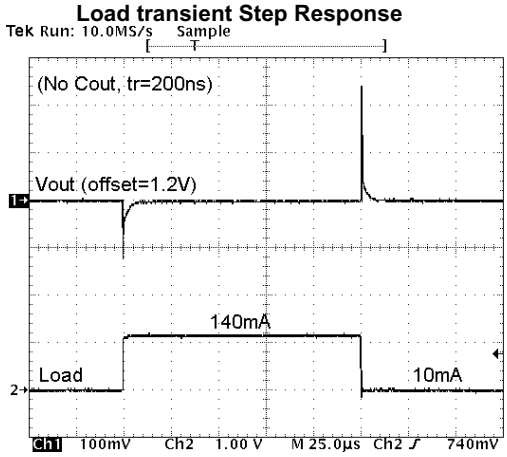
Performance Information (cont'd)

CM3112 Transient Characteristics (nominal conditions unless specified otherwise)

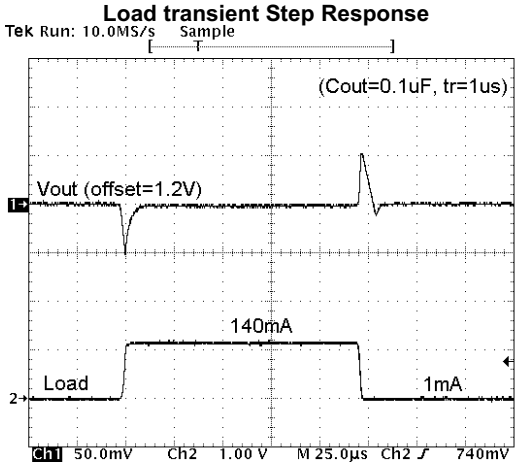
Load transient Step Response



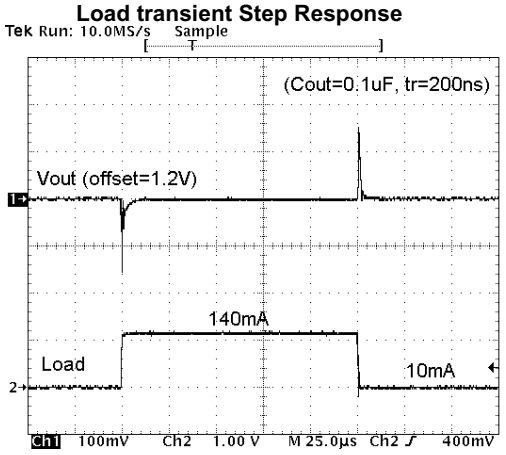
Load transient Step Response



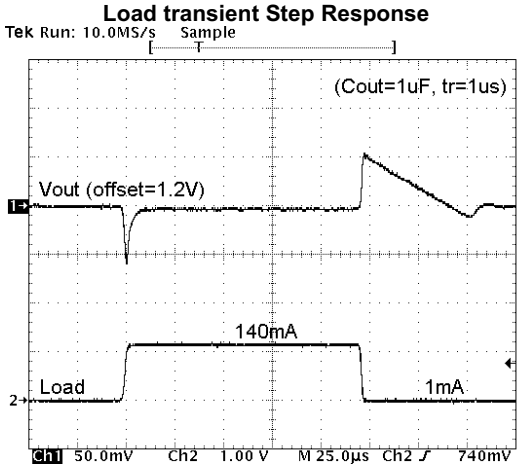
Load transient Step Response



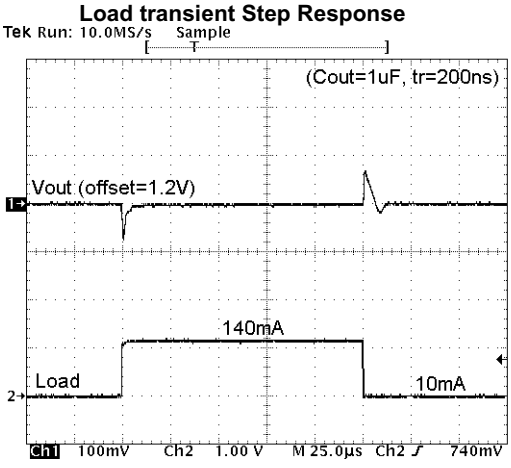
Load transient Step Response



Load transient Step Response



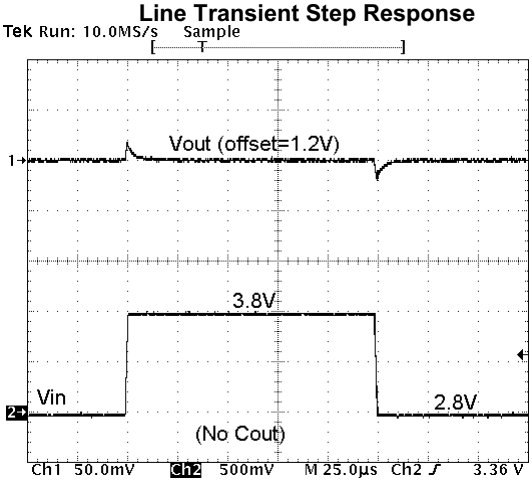
Load transient Step Response



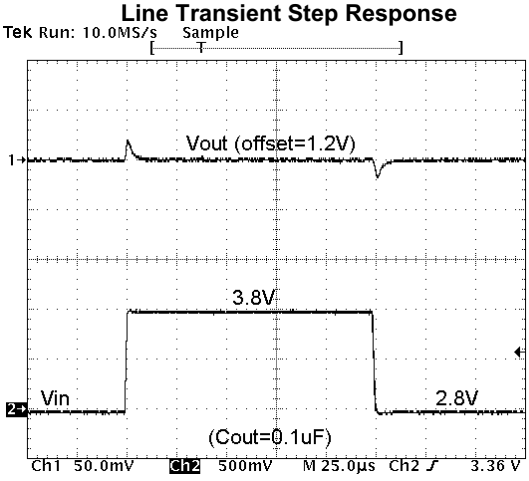
Performance Information (cont'd)

CM3112 Transient Characteristics (nominal conditions unless specified otherwise)

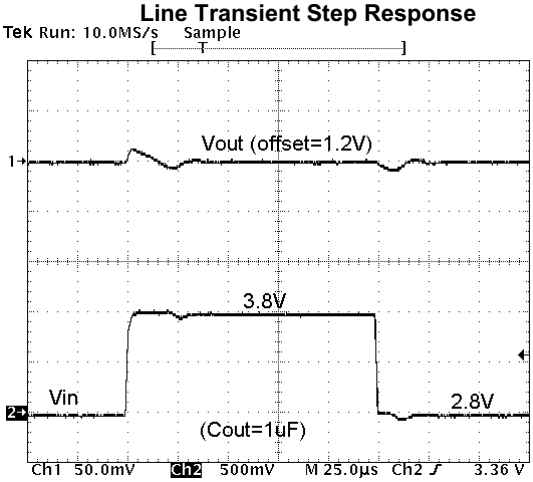
Line Transient Step Response



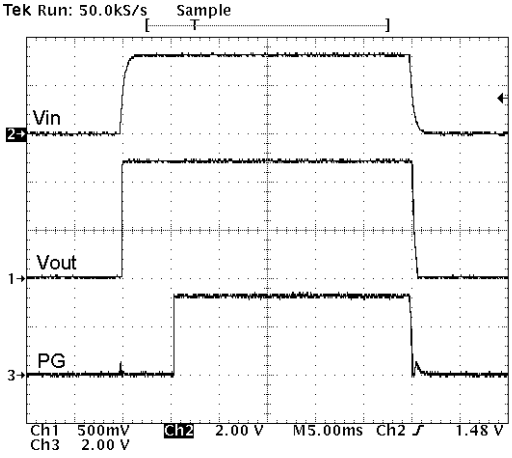
Line Transient Step Response



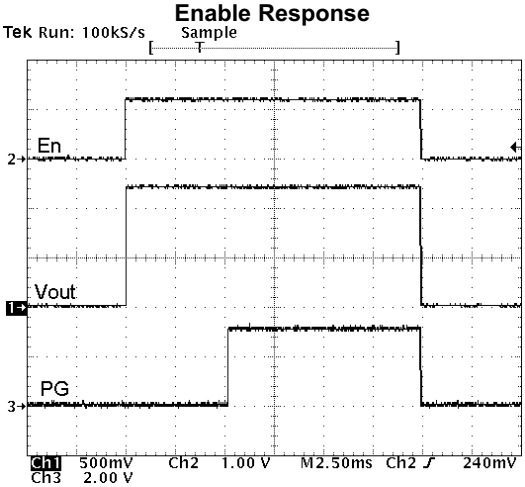
Line Transient Step Response



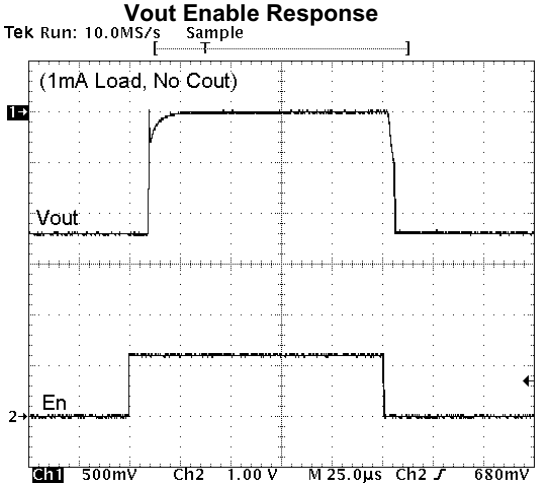
Cold Start & Power Down



Enable Response



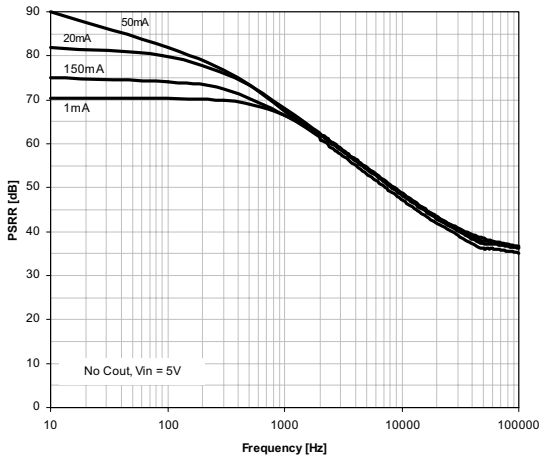
Vout Enable Response



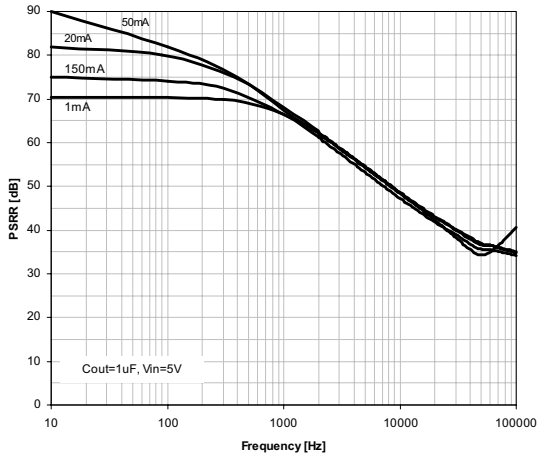
Performance Information (cont'd)

CM3112 Typical AC Characteristics (nominal conditions unless specified otherwise)

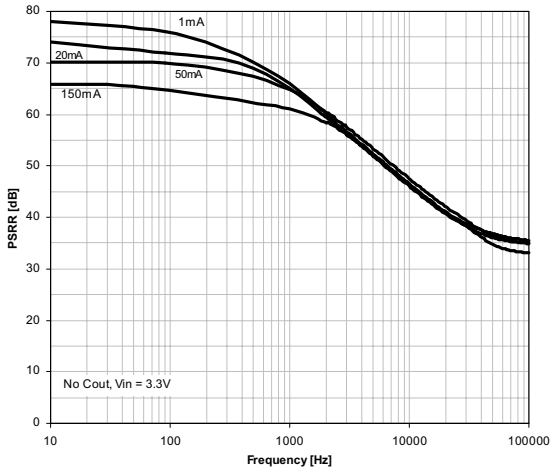
Power Supply Ripple Rejection
(No Cout, Vin=5V)



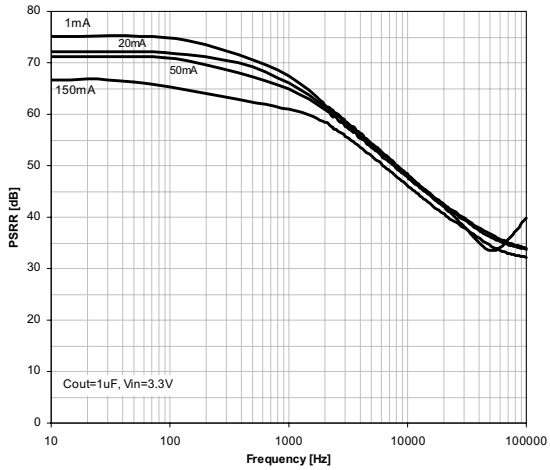
Power Supply Ripple Rejection
(Cout=1uF, Vin=5V)



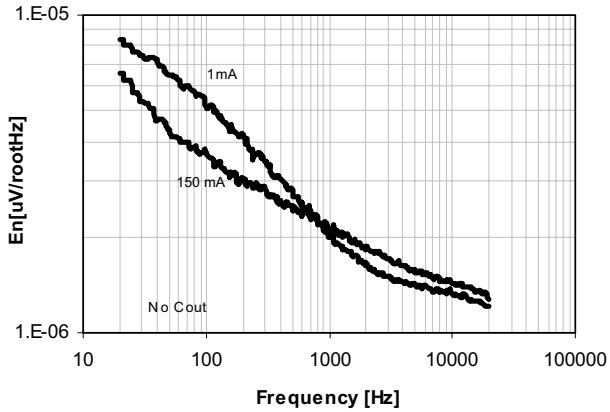
Power Supply Ripple Rejection
(No Cout, Vin=3.3V)



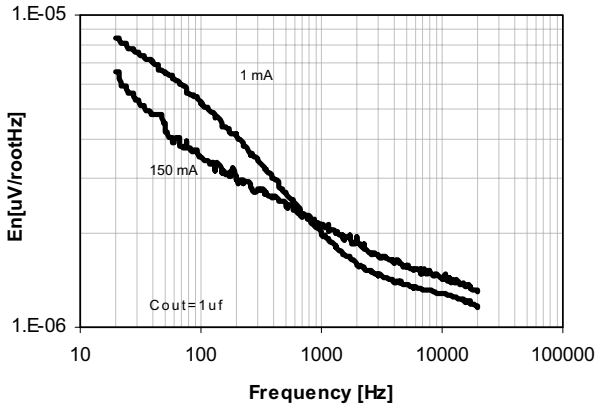
Power Supply Ripple Rejection
(Cout=1uF, Vin=3.3V)



Output Noise (No Cout)



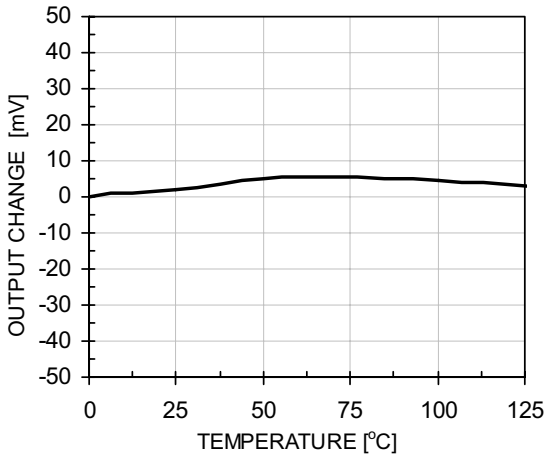
Output Noise (1uF Cout)



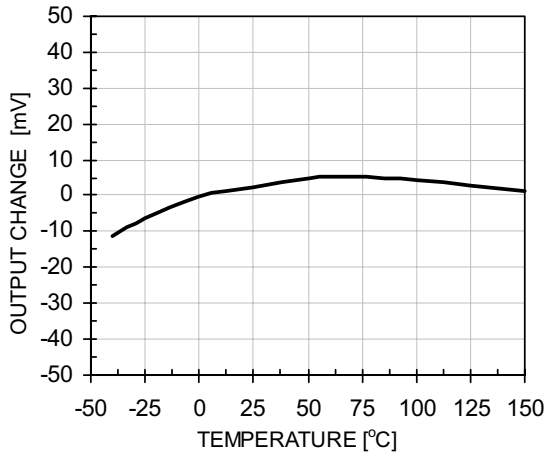
Performance Information (cont'd)

CM3112 Typical Thermal Characteristics

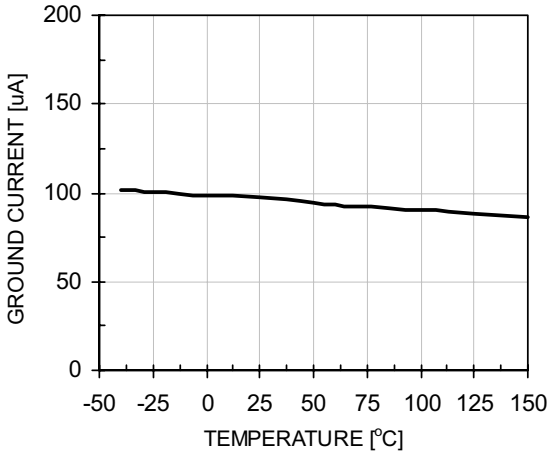
VOUT Over Temperature



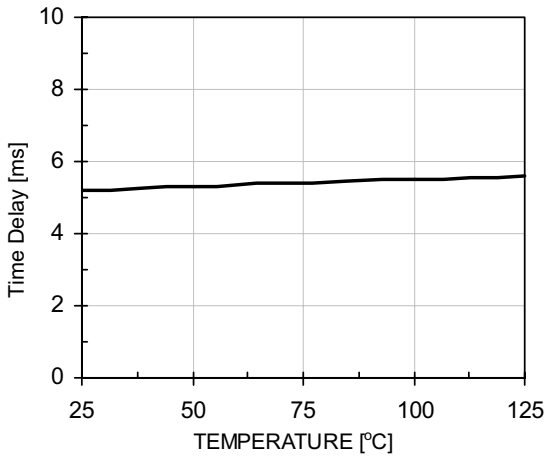
VOUT Over Temperature



Ground Current Over Temperature



Time Delay Over Temperature



Application Information

Output Capacitor

Unlike other LDO regulators the CM3112 does not require an output capacitor for stability. It is stable with any capacitor from 0 to 10uF.

Adding output capacitance will improve the very high frequency transient response of the part. Figures 1-7 demonstrate the effect of output capacitance on a 10mA to 140mA transient load step.

In first 3 figures the load step is applied with a rise time of approximately 1us. Adding capacitance does not improve the response.

The last three figures show the load step with a rise time of about 200ns. While the 0.1uF capacitor does not improve the response the 1uF capacitor decreases the overall magnitude of the transient spike.

Figure: 2

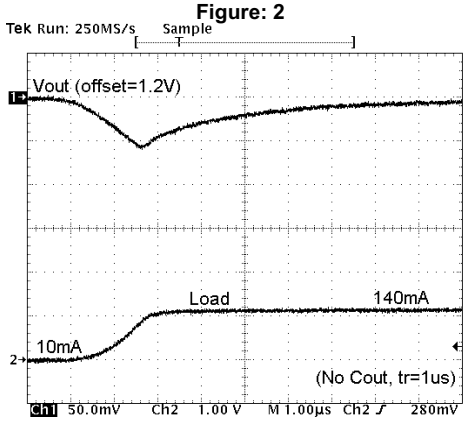


Figure: 3

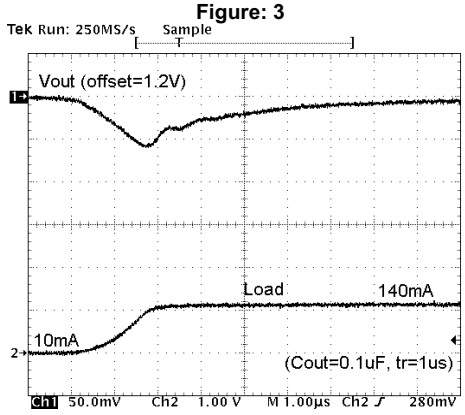


Figure: 4

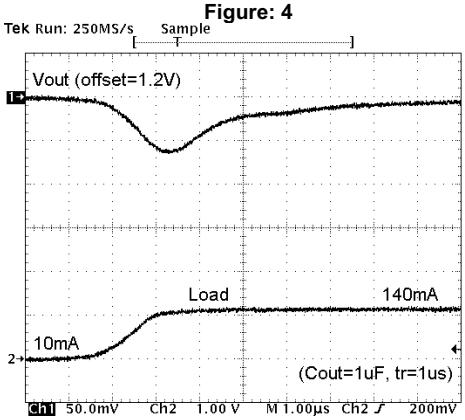


Figure: 5

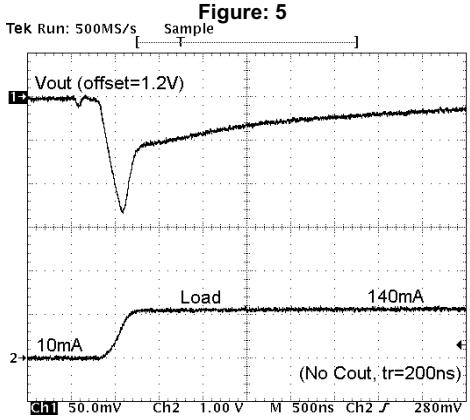


Figure: 6

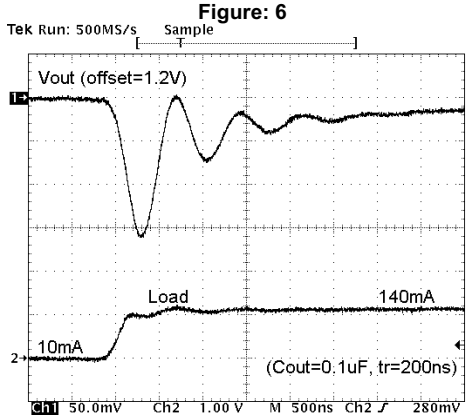
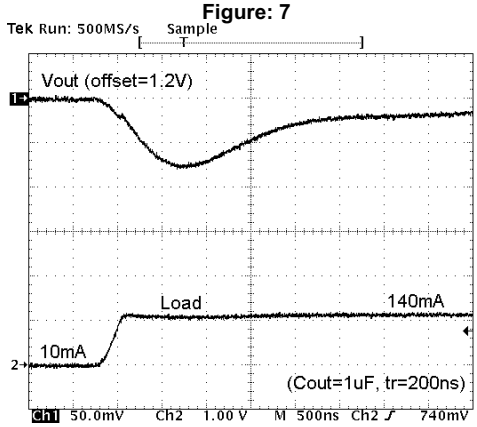


Figure: 7



Application Information (cont'd)

Power Dissipation/Handling

The overall junction to ambient thermal resistance (θ_{JA}) for device power dissipation (P_D) consists primarily of two paths in series. The first path is the junction to the case (θ_{JC}) which is defined by the package style, and the second path is case to ambient (θ_{CA}) thermal resistance which is dependent on board layout. The final operating junction temperature for any set of conditions can be estimated by the following thermal equation:

$$T_{JUNC} = T_{AMB} + P_D (\theta_{JC}) + P_D (\theta_{CA})$$
$$= T_{AMB} + P_D (\theta_{JA})$$

The CM3112-12 uses a SOT23-5 package. When this package is mounted on a double sided printed circuit board with two square inches of copper allocated for "heat spreading", the resulting θ_{JA} is 175°C/W.

Based on a maximum power dissipation of 315mW (2.1Vx150mA), with an ambient of 70°C the resulting junction temperature will be:

$$T_{JUNC} = T_{AMB} + P_D (\theta_{JA})$$
$$= 70°C + 315mW (175°C/W)$$
$$= 70°C + 55°C = 125°C$$

Thermal characteristics were measured using a double sided board with two square inches of copper area connected to the GND pins for "heat spreading".

Measurements showing performance up to junction temperature of 125°C were performed under light load conditions (1mA). This allows the ambient temperature to be representative of the internal junction temperature.

Note: The use of multi-layer board construction with separate ground and power planes will further enhance the overall thermal performance. In the event of no copper area being dedicated for heat spreading, a multi-layer board construction, using only the minimum size pad layout, will provide the CM3112-12 with an overall θ_{JA} of 175°C/W which allows up to 450mW to be safely dissipated.

Input Capacitor

If the VIN pin is within a few inches of the main input filter, a capacitor may not be necessary. Otherwise an input filter capacitor (C_{IN}) of 0.1uF to 1uF will ensure adequate filtering.

Enable/Disable

Whenever this input is taken low, the regulator pass transistor is forced into a high impedance mode and an internal discharge resistance (500Ω) will be applied from the output to ground.

Power Good

This is an open drain output signal. It works as a supply voltage supervisor for the output voltage.

It is asserted when the output falls below 84% (when 2.5V<Vin<5.5V) of its nominal value. The signal becomes inactive when the three following conditions are met (valid) for more than 1-10ms:

a) EN > 1.5V

b) 2.5V < V_{IN} < 5.5V

c) V_{OUT} > 97% of V_{OUTNOM}

Mechanical Details

SOT23-5 Mechanical Specifications

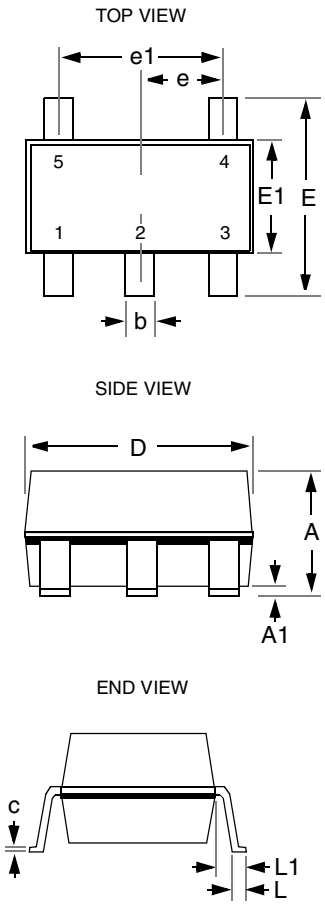
Dimensions for CM3112-12 device packaged in 5-pin SOT23 package are presented below.

For complete information on the SOT23-5 package, see the California Micro Devices SOT23 Package Information document.

PACKAGE DIMENSIONS

Package	SOT23-5 (JEDEC name is MO-178)			
Pins	5			
Dimensions	Millimeters		Inches	
	Min	Max	Min	Max
A	--	1.45	--	0.0571
A1	0.00	0.15	0.0000	0.0059
b	0.30	0.50	0.0118	0.0197
c	0.08	0.22	0.0031	0.0087
D	2.75	3.05	0.1083	0.1201
E	2.60	3.00	0.1024	0.1181
E1	1.45	1.75	0.0571	0.0689
e	0.95 BSC		0.0374 BSC	
e1	1.90 BSC		0.0748 BSC	
L	0.30	0.60	0.0118	0.0236
L1	0.60 REF		0.0236 REF	
# per tape and reel	3000 pieces			

Mechanical Package Diagrams



Package Dimensions for SOT23-5.