

## Triple Linear Voltage Regulator for DDR-I Memory and CPU

### Features

- Fully integrated power solution for a CPU/SOC core and DDR-I memory ICs
- Lowest system cost and smallest footprint with just three external output capacitors
- Three linear regulators for  $V_{CORE}$  (1.5A),  $V_{DDQ}$  (1.5A), and  $V_{TT}$  (0.5A, source-sink)
- $V_{DDQ} = 2.5V$ ,  $V_{TT} = V_{DDQ}/2 \pm 25mV$
- $V_{CORE}$  is adjustable, with a default output of 1.5V
- Over-temperature and reverse current protection
- Overcurrent protection for all regulators
- PSOP-8 package with integrated heat spreader
- Lead-free version available

### Applications

- Core CPU and DDR-I memory power for:
  - Set Top Boxes, DVD Players, Games
  - Digital TVs, Flat Panel Displays
  - Printers, Digital Projectors
  - Embedded systems
  - Communications systems

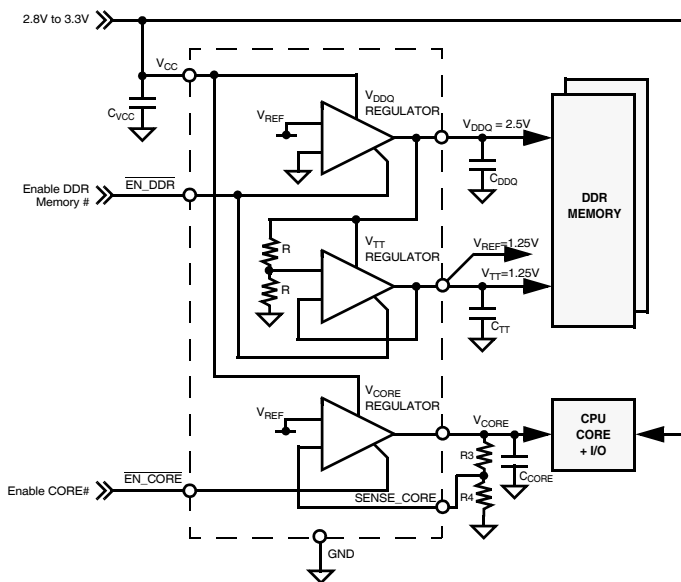
### Product Description

The CM3132 provides an integrated power solution for a CPU core and DDR-I memory for consumer and other embedded applications. It features three independent linear regulators for  $V_{CORE}$ ,  $V_{DDQ}$  and  $V_{TT}$  supply regulation. The default voltage for  $V_{CORE}$  is 1.5V. The SENSE\_CORE pin can be tied to GND for the default voltage, or through a resistor divider for setting the CPU core in the range 1.2V to 1.8V.  $V_{DDQ}$  is internally set to 2.50V and the  $V_{TT}$  voltage is always half the  $V_{DDQ}$  voltage. A capacitor should be connected to each of the three outputs.

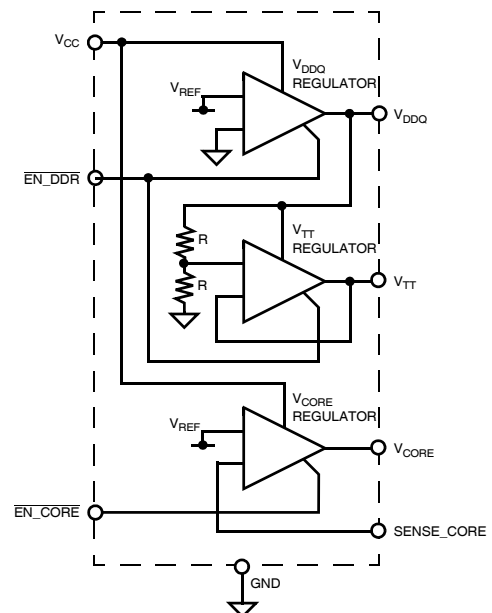
There are two enable pins,  $\overline{EN\_CORE}$  and  $\overline{EN\_DDR}$ . When  $\overline{EN\_CORE}$  is set high, the CORE regulator is disabled. When  $\overline{EN\_DDR}$  is set high, the two DDR regulators are disabled to minimize overall system power dissipation when memory is in standby mode. These two enable pins allow power sequencing of the DDR and CORE regulator blocks independently.

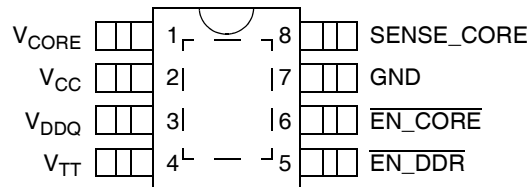
The CM3132 is available in a PSOP-8 package that has excellent thermal dissipation. It is available with optional lead-free finishing.

### Typical Application Circuit



### Circuit Schematic



**PACKAGE / PINOUT DIAGRAM**
**TOP VIEW**

**8-Lead PSOP**

Note: This drawing is not to scale.

**PIN DESCRIPTIONS**

PSOP-8		
LEAD	NAME	DESCRIPTION
1	V <sub>CORE</sub>	V <sub>CORE</sub> output.
2	V <sub>CC</sub>	Input supply.
3	V <sub>DDQ</sub>	V <sub>DDQ</sub> output.
4	V <sub>TT</sub>	V <sub>TT</sub> output for termination resistors or V <sub>REF</sub>
5	$\overline{\text{EN\_DDR}}$	Enable DDR power. Active low input.
6	$\overline{\text{EN\_CORE}}$	Enable V <sub>CORE</sub> . Active low input.
7	GND	Ground reference.
8	SENSE <sub>CORE</sub>	Sense input. Adjusts V <sub>CORE</sub> output voltage using external resistor divider. When tied to GND, V <sub>CORE</sub> = 1.5V.
PAD	GND	Tied to ground reference.

**Ordering Information**
**PART NUMBERING INFORMATION**

Leads	Package	Standard Finish		Lead-free Finish	
		Ordering Part Number <sup>1</sup>	Part Marking	Ordering Part Number <sup>1</sup>	Part Marking
8	PSOP-8	CM3132-02SB	CM3132 02SB	CM3132-02SH	CM3132 02SH

Note 1: Parts are shipped in Tape &amp; Reel form unless otherwise specified.

## Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	RATING	UNITS
ESD (Human Body Model)	$\pm 2000$	V
Pin Voltages $V_{CC}$ $\overline{EN\_CORE}$ , $\overline{EN\_DDR}$ , $\overline{SENSE\_CORE}$ $V_{DDQ}$ , $V_{TT}$	[GND - 0.6] to [+6.5] [GND - 0.6] to [ $V_{CC} + 0.6$ ] [GND - 0.6] to [ $V_{CC} + 0.6$ ]	V V V
Storage Temperature Range	-40 to +150	$^{\circ}\text{C}$
Operating Temperature Range Ambient Junction	0 to +85 0 to +125	$^{\circ}\text{C}$ $^{\circ}\text{C}$

STANDARD OPERATING CONDITIONS		
PARAMETER	RATING	UNITS
Ambient Operating Temperature Range	0 to +85	$^{\circ}\text{C}$
<b>1. <math>V_{DDQ}</math> Regulator</b>		
DDR-I Supply Voltage $V_{CC}$	[ $V_{DDQ} + 0.3$ ] to 3.6	V
Load Current	0 to 1500	mA
$C_{CC}$ , $C_{DDQ}$	10, 10	$\mu\text{F}$
<b>2. <math>V_{TT}</math> Regulator</b>		
DDR-I Supply Voltage $V_{DDQ}$	2.3 to 2.8	V
DDR-I Load Current	0 to $\pm 500$	mA
$C_{TT}$	47	$\mu\text{F}$
<b>3. <math>V_{CORE}</math> Regulator</b>		
Core Supply Voltage $V_{CC}$	[ $V_{DDQ}$ or $V_{CORE} + 0.3$ ] to 3.6	V
DDR-I Load Current	0 to 1500	mA
$C_{CORE}$	10	$\mu\text{F}$

**Specifications (cont'd)**

<b>ELECTRICAL OPERATING CHARACTERISTICS (SEE NOTE1)</b>						
<b>SYMBOL</b>	<b>PARAMETER</b>	<b>CONDITIONS</b>	<b>MIN</b>	<b>TYP</b>	<b>MAX</b>	<b>UNITS</b>
<b>General Parameters</b>						
T <sub>OVER</sub>	Shutdown Junction Temperature		-	150	-	°C
T <sub>HYST</sub>	Junction Temp Hysteresis	IC in shutdown	-	25	-	°C
I <sub>CCN</sub>	Normal Mode V <sub>CC</sub> Supply Current	$\overline{\text{EN\_DDR}} = \text{logic "0"};$ $\overline{\text{EN\_CORE}} = \text{logic "0"}$		400	800	μA
I <sub>CCQ</sub>	Shutdown Mode V <sub>CC</sub> Supply Current	$\overline{\text{EN\_DDR}} = \text{logic "1"};$ $\overline{\text{EN\_CORE}} = \text{logic "1"}$		2	10	μA
I <sub>SENSE IN</sub>	SENSE_CORE Input Current	V <sub>SENSE_CORE</sub> =0.6V		0.1	1.0	μA
V <sub>IH</sub>	$\overline{\text{EN\_DDR}}$ , $\overline{\text{EN\_CORE}}$ Input High Threshold	V <sub>CORE</sub> =3.3V	2.0			V
V <sub>IL</sub>	$\overline{\text{EN\_DDR}}$ , $\overline{\text{EN\_CORE}}$ Input Low Threshold	V <sub>CORE</sub> =3.3V			0.4	V
UVLO	Under Voltage Lock-Out	I <sub>DDQ</sub> = 10mA			1.8	V
t <sub>RISE</sub>	V <sub>DDQ</sub> , V <sub>CORE</sub> Rise Time	V <sub>CC</sub> = 3.3V, C <sub>LOAD</sub> = 10μF		0.5		ms
<b>V<sub>DDQ</sub> Regulator Parameters</b>						
V <sub>CC MIN</sub>	Input Voltage	V <sub>DDQ</sub> = 2.5V, I <sub>DDQ</sub> = 1.5A, Note 2	2.80			V
V <sub>DDQ DEF</sub>	Default Output Voltage	I <sub>DDQ</sub> = 0.01A, 2.8V ≤ V <sub>CC</sub> ≤ 3.6V, Note 2	2.45	2.50	2.55	V
V <sub>DDQ LD</sub>	Load Regulation	T <sub>A</sub> = 25°C, V <sub>CC</sub> = 3.3V, 0.01A ≤ I <sub>DDQ</sub> ≤ 1.5A, Note 2	-	-	2.5	%
V <sub>DDQ LINE</sub>	Line Regulation	T <sub>A</sub> = 25°C, I <sub>DDQ</sub> = 0.01A, 2.8V ≤ V <sub>CC</sub> ≤ 3.6V, Note 2	-1.0	-	1.0	%
e <sub>N DDQ</sub>	Output Noise Voltage	BW = 10Hz - 100kHz, C <sub>DDQ</sub> = 10μF		49		μVrms
I <sub>DDQ LIM</sub>	Current Limit	Note 2	1.7	2.0		A
I <sub>DDQ SC</sub>	Short Circuit Current	V <sub>DDQ</sub> < 0.3V		0.5		A

**ELECTRICAL OPERATING CHARACTERISTICS (CONT'D)** (SEE NOTE1)

V <sub>TT</sub> Regulator Parameters						
V <sub>TT</sub>	Output Voltage Range	V <sub>DDQ</sub> = 2.5V, I <sub>TT</sub> = 0.01A, I <sub>DDQ</sub> = 0A	1.20	1.25	1.30	V
V <sub>TT REF</sub>	Output Voltage Range	V <sub>CC</sub> = 0V, V <sub>DDQ</sub> = 2.500V, I <sub>TT</sub> = 0.01A	1.225	1.250	1.275	V
V <sub>TT LD</sub>	Load Regulation	T <sub>A</sub> = 25°C, V <sub>DDQ</sub> = 2.5V, 0.01A ≤ I <sub>TT</sub> ≤ ±0.5A	-1.0	-	1.0	%
e <sub>N TT</sub>	Output Noise Voltage	BW = 10Hz - 100kHz, C <sub>TT</sub> = 10μF		51		μVrms
I <sub>TT LIM</sub>	Current Limit		0.6	0.8		A
I <sub>TT SC</sub>	Short Circuit Current	V <sub>TT</sub> < 0.7V		0.3		A
V <sub>CORE</sub> Regulator Parameters						
V <sub>CC MIN</sub>	Input Voltage	V <sub>CORE</sub> = 1.5V, I <sub>CORE</sub> = 1.5A, SENSE_CORE = 0V, Note 3	2.2			V
V <sub>CORE DEF</sub>	Default Output Voltage Range	V <sub>CC</sub> = 3.3V, I <sub>CORE</sub> = 0.01A, SENSE_CORE = 0V	1.45	1.50	1.55	V
V <sub>CORE ADJ</sub>	Adjustable Output Voltage Range	V <sub>CC</sub> = 3.3V, SENSE_CORE from resistors R3 & R4, Note 4	1.2		1.8	V
V <sub>CORE LD</sub>	Load Regulation	T <sub>A</sub> = 25°C, V <sub>CC</sub> = 3.3V, 0.01A ≤ I <sub>CORE</sub> ≤ ±1.5	-	-	2.5	%
V <sub>CORE LINE</sub>	Line Regulation	T <sub>A</sub> = 25°C, 2.8V ≤ V <sub>CC</sub> ≤ 3.6V, I <sub>CORE</sub> = 0.01A	-1.0	-	1.0	%
e <sub>N CORE</sub>	Output Noise Voltage	BW = 10Hz - 100kHz, C <sub>CORE</sub> = 47μF		59		μVrms
I <sub>CORE LIM</sub>	Current Limit		1.7	2.0		A
I <sub>CORE SC</sub>	Short Circuit Current	V <sub>CORE</sub> < 0.3V		0.5		A

Note 1: All parameters specified at T<sub>A</sub> = 0°C to +85°C unless otherwise noted.

Note 2: Note that the I<sub>DDQ</sub> current specified is the load current output from the V<sub>DDQ</sub> pin. V<sub>DDQ</sub> also supplies current internally to the V<sub>TT</sub> regulator when it is sourcing current. The maximum source current can be up to 0.5A. The maximum total current from the V<sub>DDQ</sub> regulator is the external V<sub>DDQ</sub> current I<sub>DDQ</sub> added to the maximum V<sub>TT</sub> sourcing current I<sub>TT</sub>. All load currents are specified as such, but the V<sub>DDQ</sub> current limit is specified at a current just above the total maximum current.

Note 3: V<sub>CORE</sub> regulator only. Refer to V<sub>DDQ</sub> regulator parameters for V<sub>DDQ</sub> regulator.

Note 4:  $V_{CORE} = 1.15V \times (1 + \frac{R3}{R4})$

VCC(1)	EN_DDR	V <sub>DDQ</sub> OUT	V <sub>TT</sub> OUT
2.8V to 3.6V	Low	V <sub>DDQ</sub>	V <sub>DDQ</sub> / 2
X	High	0V	0V

**Table 1: Truth Table for CM3132**

## Performance Information

### Power Supply Ripple Rejection

$C_{CC} = 10\mu\text{F}$ ,  $V_{CC} = 3.3\text{V}$ ,  $I_{LOAD} = 50\text{mA}$ , PSRR measured with 50mV pk-pk sin wave on  $V_{CC}$ .

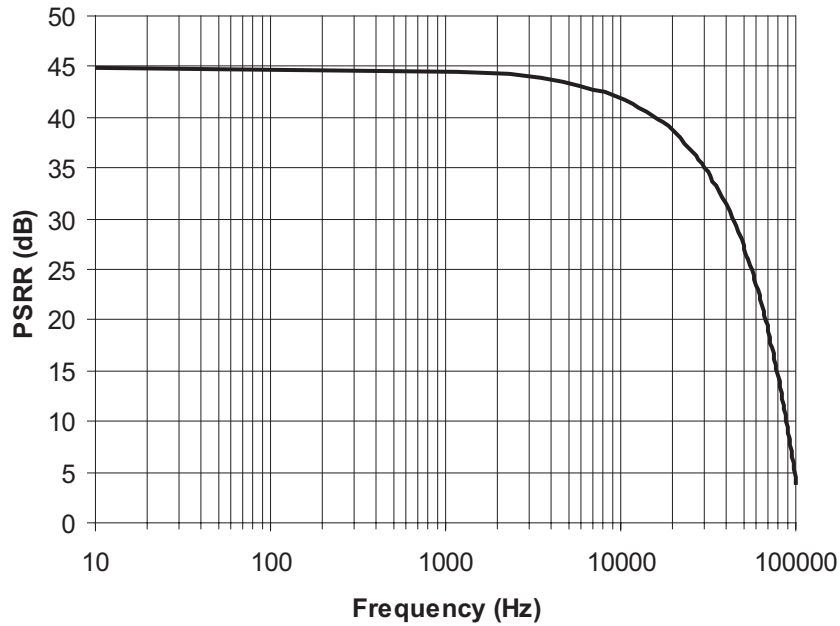


Figure 1.  $V_{CORE}$  PSRR ( $V_{CORE} = 1.5\text{V}$ )

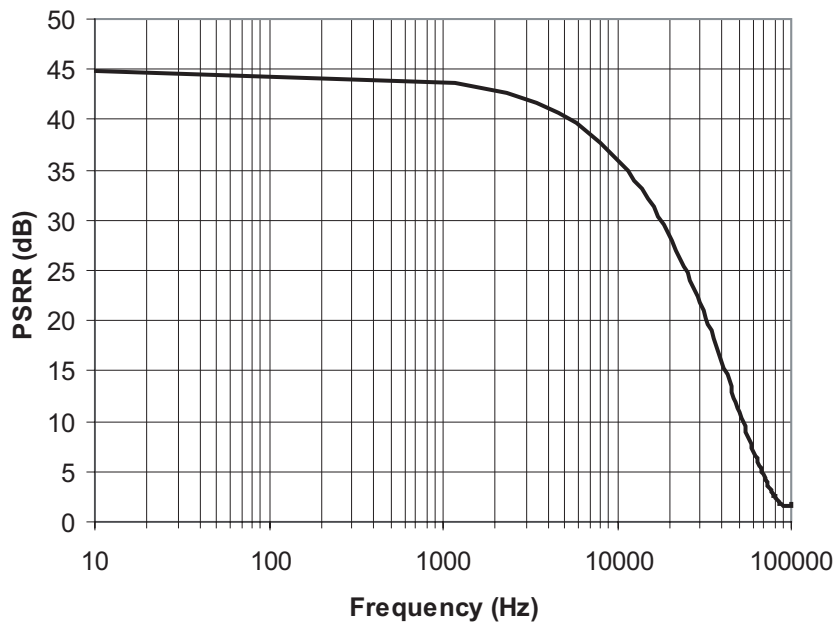
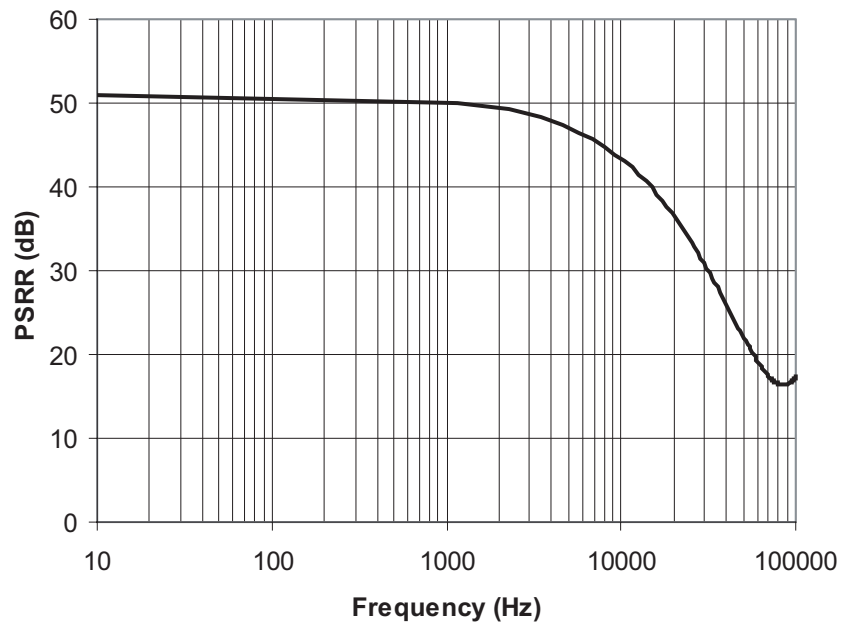


Figure 2.  $V_{DDQ}$  PSRR ( $V_{DDQ} = 2.5\text{V}$ )



**Figure 3.  $V_{TT}$  PSRR ( $V_{TT} = 1.25V$ )**

**Performance Information (cont'd)**

**Typical Thermal Characteristics**

The overall junction to ambient thermal resistance ( $\theta_{JA}$ ) for device power dissipation ( $P_D$ ) consists primarily of two paths in series. The first path is the junction to the case ( $\theta_{JC}$ ) which is defined by the package style, and the second path is case to ambient ( $\theta_{CA}$ ) thermal resistance which is dependent on board layout. The final operating junction temperature for any set of conditions can be estimated by the following thermal equation:

$$T_{JUNC} = T_{AMB} + P_D (\theta_{JC}) + P_D (\theta_{CA})$$

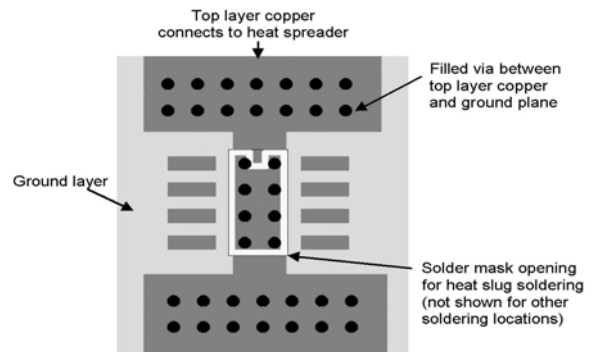
$$= T_{AMB} + P_D (\theta_{JA})$$

When a CM3132-02SB (PSOP-8) is mounted on a double-sided printed circuit board with two square inches of copper allocated for "heat spreading," the resulting  $\theta_{JA}$  is 40°C/W. Based on the over temperature limit of 150° C with an ambient of 70°C, the available power of this package will be:

$$P_D = \frac{150^\circ C - 70^\circ C}{40^\circ C/W} = 2W$$

**PCB Layout Considerations**

The CM3132-02SB/SH has a heat spreader attached to the bottom of the PSOP-8 package in order for heat to be transferred more easily from the package to the PCB. The heat spreader is a copper pad of dimensions just smaller than the package itself. By positioning the matching pad on the PCB top layer to connect to the spreader during manufacturing, the heat will be transferred between the two pads. The drawing below shows the recommended PCB layout. Note that there are six vias on either side to allow the heat to dissipate into the ground and power planes on the inner layers of the PCB. Vias can be placed underneath the chip, but this can cause blockage of the solder. The ground and power planes should be at least 2 sq in. of copper by the vias. It also helps dissipation if the chip is positioned away from the edge of the PCB, and not near other heat-dissipating devices. A good thermal link from the PCB pad to the rest of the PCB will assure the best heat transfer from the CM3132 package to ambient,  $\theta_{JA}$ , of around 40°C/W.



**Figure 4. Recommended Heat Sink PCB Layout**



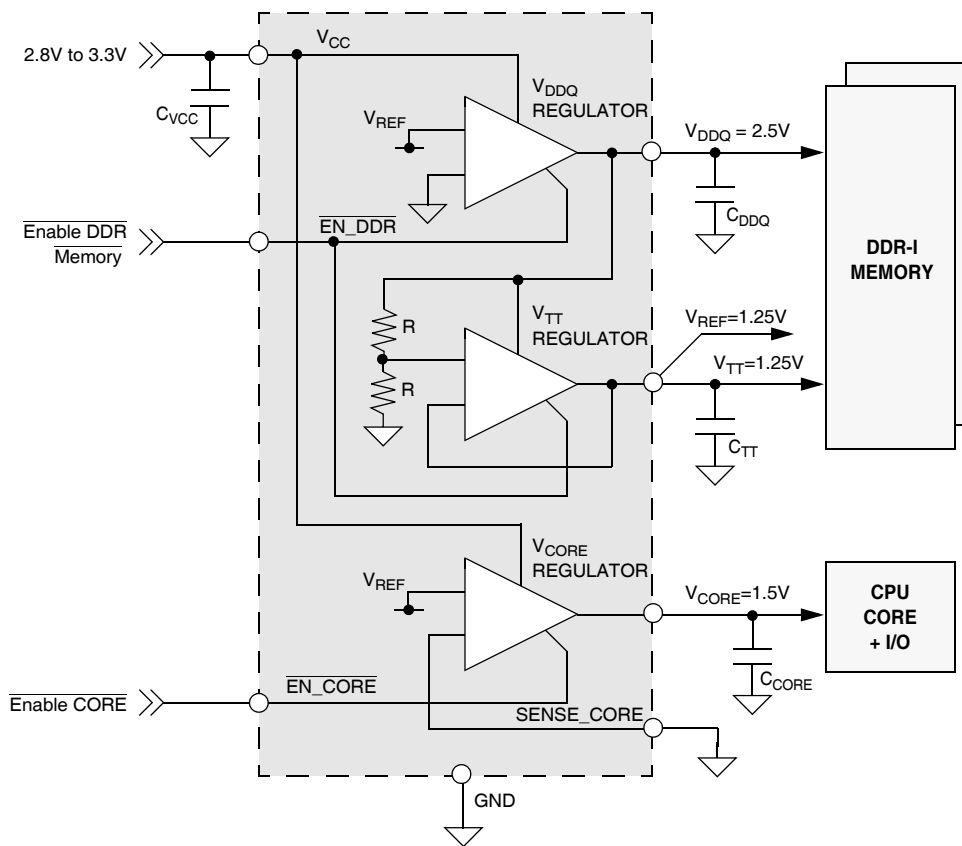
## Application Information

### Other Applications

The CM3132 can be used without any external resistors if a core voltage of 1.5V is required, the SENSE\_CORE pin is connected to GND.

In applications where a reference voltage ( $V_{REF}$ ) is required, the  $V_{TT}$  pin can be used. The  $V_{TT}$  output pin has an error relative to  $V_{DDQ}/2$  of up to  $\pm 25mV$ , which is well within most DDR system specs of  $\pm 50mV$ . This

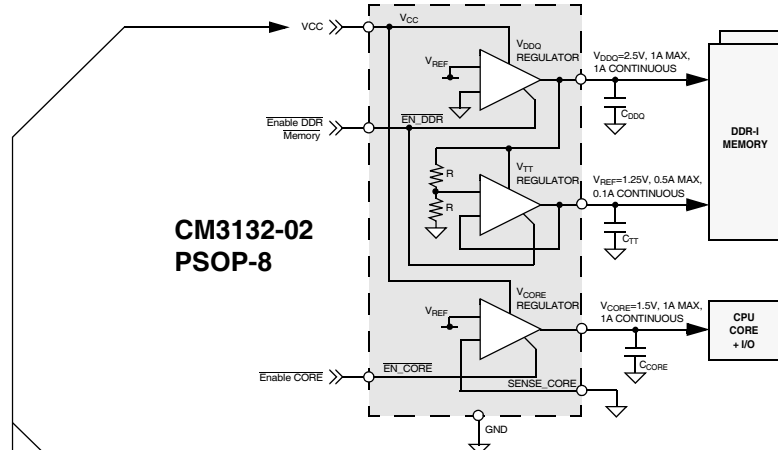
is because the  $V_{TT}$  output internally tracks the  $V_{DDQ}$  output very closely due to the matched on-chip resistors  $R$  that tap down from the  $V_{DDQ}$  rail, and the low offset voltage of the  $V_{TT}$  regulator. It is recommended that the  $V_{REF}$  trace be connected directly to the  $V_{TT}$  pin, as shown in Figure 5, to eliminate noise and ripple on the  $V_{TT}$  trace caused by current switching.



**Figure 5. Minimal cost solution for CM3132 supplying DDR memory and core CPU.**

**Application Information (cont'd)**

**1 PSOP-8 IC drives 1-DIMM single channel DDR-I and CPU Core VCORE rail**



With 3.3V<sub>CC</sub> @ 1A (V<sub>DDQ</sub>), 0.1A (V<sub>TT</sub>), 1A (V<sub>CORE</sub>),  
 $P_D = (3.3-2.5) * 1.05 + (2.5-1.25) * 0.1 + (3.3-1.5) * 1 = 0.84 + 0.125 + 1.8 = 2.765W$

With 3.0V<sub>CC</sub> @ 1A (V<sub>DDQ</sub>), 0.1A (V<sub>TT</sub>), 1A (V<sub>CORE</sub>),  
 $P_D = (3.0-2.5) * 1.05 + (2.5-1.25) * 0.1 + (3.0-1.5) * 1 = 0.525 + 0.125 + 1.5 = 2.15W$

With 2.8V<sub>CC</sub> @ 1A (V<sub>DDQ</sub>), 0.1A (V<sub>TT</sub>), 1A (V<sub>CORE</sub>),  
 $P_D = (2.8-2.5) * 1.05 + (2.5-1.25) * 0.1 + (2.8-1.5) * 1 = 0.315 + 0.125 + 1.3 = 1.74W$

**Figure 6. Power Dissipation Calculations**

$T_{JUNC} = T_{AMB} + P_D * (\theta_{JA})$

$P_D = (T_{AMB} - T_{JUNC}) / (\theta_{JA})$

$P_D = (V_{CC}-2.5)*I_{DDQ} + (2.5-1.25)*0.1 + (V_{CC}-V_{CORE})*I_{CORE}$

$P_D - (V_{CC}-2.5)*I_{DDQ} - 0.125 = (V_{CC}-V_{CORE})*I_{CORE}$

$I_{CORE} = [P_D - (V_{CC}-2.5)*I_{DDQ} - 0.125] / (V_{CC}-V_{CORE})$

$\theta_{JA} = 40\text{ }^\circ\text{C/W}$	Derating (degC/W)	40	40	40	40	40	40	40	40	40	
	Ambient (degC)	85	85	85	60	60	60	40	40	40	
	Max Power (W)	1.6	1.6	1.6	2.3	2.3	2.3	2.8	2.8	2.8	
	Vcc (V)	3.3	3.0	2.8	3.3	3.0	2.8	3.3	3.0	2.8	
	Min Vcore (V)	1.5	1.5	1.5	1.5	1.4	1.0	1.5	1.2	1.1	
	Max Iddq (A)	1.0	0.8	0.5	1.0	1.0	1.0	1.0	1.0	1.0	
	Max Icore (A)	0.4	0.7	1.0	0.7	1.0	1.0	1.0	1.0	1.4	
	Derating (degC/W)	60	60	60	60	60	60	60	60	60	
	Ambient (degC)	85	85	85	60	60	60	40	40	40	
$\theta_{JA} = 60\text{ }^\circ\text{C/W}$	Max Power (W)	1.1	1.1	1.1	1.5	1.5	1.5	1.8	1.8	1.8	
	Vcc (V)	3.3	3.0	2.8	3.3	3.0	2.8	3.3	3.0	2.8	
	Min Vcore (V)	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.4	
	Max Iddq (A)	0.3	0.5	0.6	1.0	0.7	0.5	0.5	0.7	1.0	
	Max Icore (A)	0.4	0.5	0.6	0.3	0.7	0.9	0.7	1.0	1.0	
	Derating (degC/W)	80	80	80	80	80	80	80	80	80	
	Ambient (degC)	85	85	85	60	60	60	40	40	40	
	$\theta_{JA} = 80\text{ }^\circ\text{C/W}$	Max Power (W)	0.8	0.8	0.8	1.1	1.1	1.1	1.4	1.4	1.4
		Vcc (V)	3.3	3.0	2.8	3.3	3.0	2.8	3.3	3.0	2.8
Min Vcore (V)		1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	
Max Iddq (A)		0.3	0.3	0.3	0.5	0.5	0.5	0.5	0.7	0.5	
Max Icore (A)		0.2	0.4	0.5	0.3	0.5	0.7	0.5	0.6	0.8	

**Figure 7. Power Derating Table**

## Mechanical Details

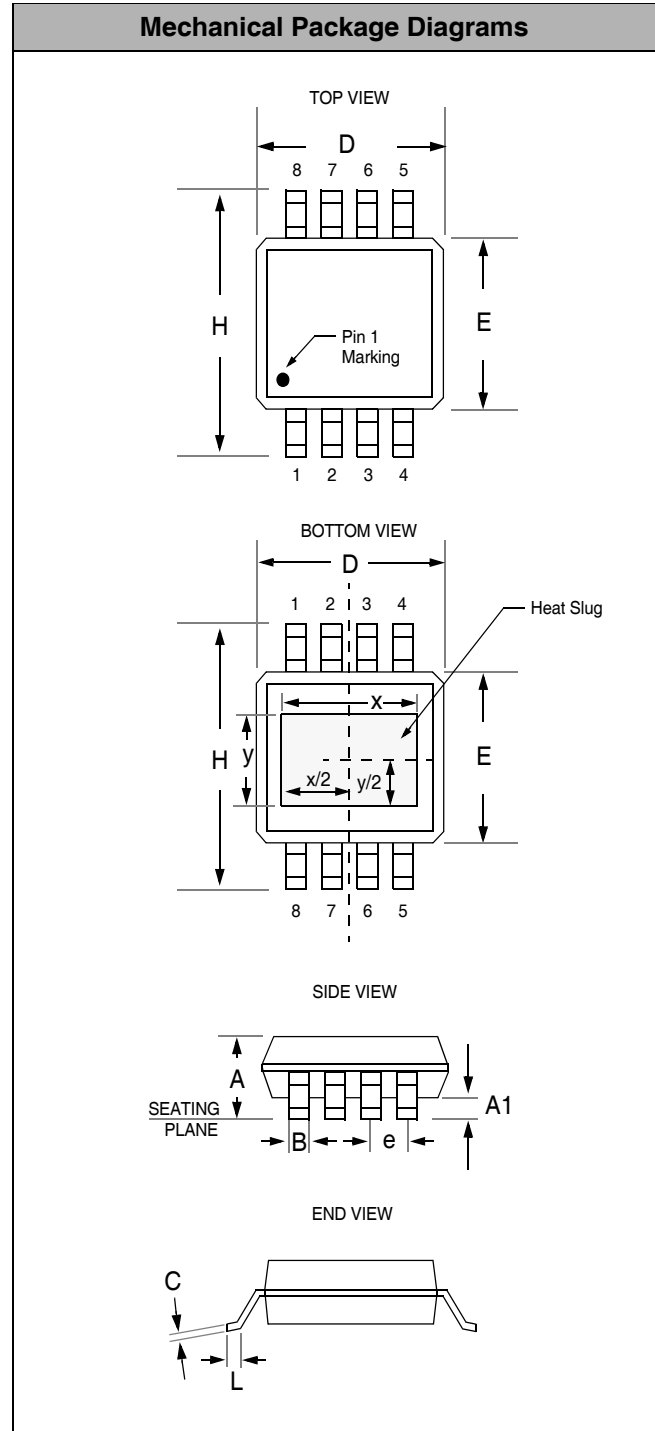
### PSOP-8 Mechanical Specifications

Dimensions for CM3132 devices packaged in an 8-lead PSOP package with a heatspreader are shown below.

PACKAGE DIMENSIONS				
Package	PSOP-8			
Leads	8			
Dimensions	Millimeters		Inches	
	Min	Max	Min	Max
A	1.30	1.62	0.051	0.064
A <sub>1</sub>	0.03	0.10	0.001	0.004
B	0.33	0.51	0.013	0.020
C	0.18	0.25	0.007	0.010
D	4.83	5.00	0.190	0.197
E	3.81	3.99	0.150	0.157
e	1.02	1.52	0.040	0.060
H	5.79	6.20	0.228	0.244
L	0.41	1.27	0.016	0.050
x**	3.30	3.81	0.130	0.150
y**	2.29	2.79	0.090	0.110
# per tube	100 pieces*			
# per tape and reel	2500 pieces			
Controlling dimension: inches				

\* This is an approximate number which may vary.

\*\* Centered on package centerline.



**Package Dimensions for PSOP-8**