CMPWR101

250 mA SmartOR™ Regulator with V_{AUX} Switch

Product Description

The ON Semiconductor's SmartOR™ CMPWR101 is a low dropout regulator that delivers up to 250 mA of load current at a fixed 3.3 V output. An internal threshold level (typically 4.1 V) is used to prevent the regulator from being operated below dropout voltage. The device continuously monitors the input supply and will automatically disable the regulator when V_{CC} falls below the threshold level. When the regulator is disabled, a low impedance, fully integrated switch is enabled which allows the output to be directly powered from an auxiliary 3.3 V supply.

When V_{CC} is restored to a level above the select threshold, the low impedance switch is disabled and the regulator is once again enabled.

All the necessary control circuitry needed to provide a smooth and automatic transition between the supplies has been incorporated. This allows V_{CC} to be dynamically switched without loss of output voltage.

An output logic signal, DRIVE, is active LOW whenever the internal regulator is disabled.

The CMPWR101 is housed in a 8−pin SOIC package and is available with RoHS compliant lead−free finishing.

Features

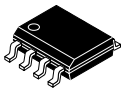
- Automatic Detection of V_{CC} Input Supply
- Glitch−Free Output During Supply Transitions
- Built−In Hysteresis During Supply Selection
- 250 mA Output Maximum Load Current
- Fully Integrated V_{AUX} Switch
- Overload Current Protection
- Short Circuit Current Protection
- Operates from Either V_{CC} or V_{AUX}
- 8−Pin SOIC Package
- These Devices are Pb−Free and are RoHS Compliant

Applications

- PCI Adapter Cards
- Network Interface Cards (NICs)
- Dual Power Systems
- Systems with Standby Capabilities

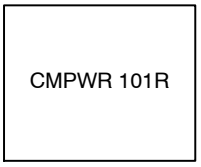
ON Semiconductor®

http://onsemi.com



SIOC 8
R SUFFIX
CASE 751BD

MARKING DIAGRAM



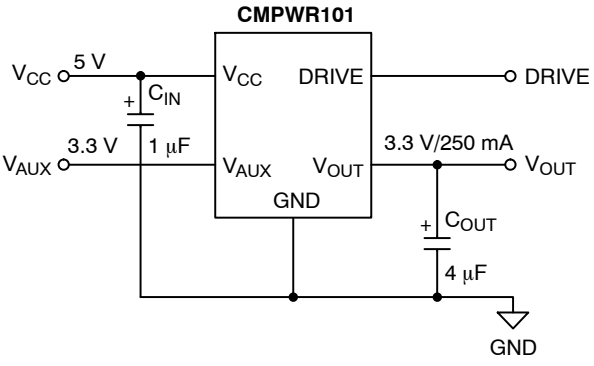
CMPWR 101R = CMPWR101R

ORDERING INFORMATION

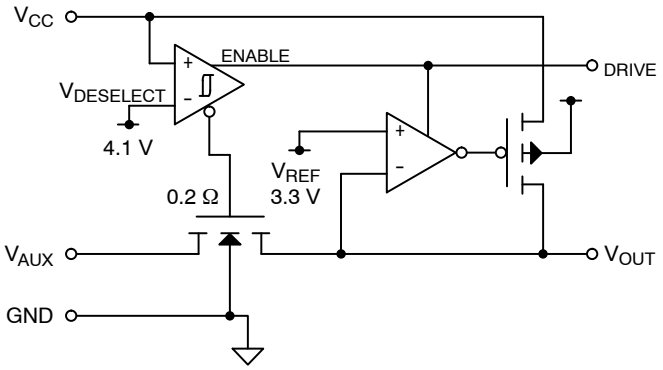
Device	Package	Shipping†
CMPWR101R	SOIC (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

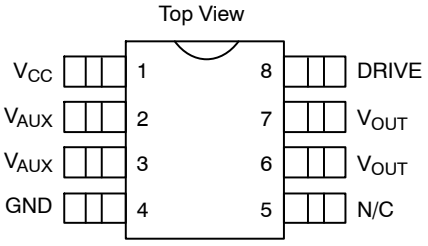
TYPICAL APPLICATION CIRCUIT



SIMPLIFIED ELECTRICAL SCHEMATIC



PACKAGE / PINOUT DIAGRAM



8−Pin SOIC

Table 1. PIN DESCRIPTIONS

Pin(s)	Name	Description
1	V_{CC}	V_{CC} is the power source for the internal regulator and is monitored continuously by an internal controller circuit. Whenever V_{CC} exceeds V_{CCSEL} (4.25 V typically), the internal regulator will be enabled and deliver a fixed 3.3 V at V_{OUT}. When V_{CC} falls below V_{CCDES} (4.10 V typically), the regulator will be disabled. Internal loading on this pin is typically 0.6 mA when the regulator is enabled, which reduces to 0.1 mA whenever the regulator is disabled. If V_{CC} falls below the voltage on the V_{AUX} pin, the V_{CC} loading will further reduce to only a few microamperes. During a V_{CC} power−up or power−down sequence, there will be an effective step increase in V_{CC} line current when the regulator is enabled/disabled. This line current transient will cause a voltage disturbance at the V_{CC} pin. The magnitude of the disturbance will be directly proportional to the effective power supply source impedance being delivered to the V_{CC} input. A built−in hysteresis voltage of 150 mV has been incorporated to minimize any chatter during supply changeover. It is recommended that the power supply connected to the V_{CC} input should have a source resistance of less than 0.25 Ω to minimize the event of chatter during the enabling/disabling of the regulator. If the V_{CC} pin is within a few inches of the main input filter, a capacitor may not be necessary. Otherwise an input filter capacitor in the range of 1 μF to 10 μF will help to lower the effective source impedance.
2−3	V_{AUX}	V_{AUX} is the auxiliary power source. When selected, ($V_{CC} < V_{CCDES}$), the auxiliary supply is directly connected to V_{OUT}, via the low impedance (0.3 Ω typically) fully integrated switch. The internal loading on this pin is typically less than 10 μA and will increase to 100 μA if V_{CC} falls below the voltage on V_{AUX}. When V_{AUX} = 0 V, the V_{CCDES} voltage is inhibited which prevents the regulator from being disabled.
4	GND	GND is the negative reference for all voltages. The current that flows in the ground connection is very low (typically 0.6 mA) and has minimal variation over all load conditions.
5	NC	NC is an unconnected pin which is electrically isolated from the internal circuitry.
6−7	V_{OUT}	V_{OUT} is the regulator output voltage connection used to power the load. An output capacitor of 4.7 μF is used to provide the necessary phase compensation, thereby preventing oscillation. The capacitor also helps to minimize the peak output disturbance during power supply changeover.
8	DRIVE	DRIVE is a CMOS output logic signal (Active Low) referenced to the V_{CC} supply. This output is taken low whenever the internal regulator is not enabled. This output is intended only as a control signal for external circuitry.

SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
ESD Protection (HBM)	±2000	V
Pin Input Voltages V_{CC} V_{AUX} DRIVE	 [GND − 0.5] to +6.0 [GND − 0.5] to +4.0 [GND − 0.5] to [V_{CC} + 0.5]	V
Storage Temperature Range	−40 to +150	°C
Operating Temperature Range Ambient Junction	 0 to +70 0 to +125	°C
Power Dissipation (Note 1)	0.5	W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The power rating is based on a printed circuit board heat spreading capability equivalent to 2 square inches of copper connected to the GND pins. Typical multi−layer boards using power plane construction will provide this heat spreading ability without the need for additional dedicated copper area. (Please consult with factory for thermal evaluation assistance).

Table 3. STANDARD OPERATING CONDITIONS

Parameter	Rating	Units
V_{CC}	5.0 ±0.5	V
V_{AUX}	3.3 ±0.3	V
Ambient Operating Temperature Range	0 to +70	°C
Load Current	0 to 250	mA
C_{EXT}	4.7 ±20%	μF

Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OUT}	Regulator Output Voltage	0 mA < I_{LOAD} < 250 mA	3.135	3.300	3.465	V
I_{LIM}	Regulator Current Limit		275			mA
V_{CCSEL}	V_{CC} Select Voltage	Regulator Enabled		4.30	4.45	V
V_{CCDES}	V_{CC} Deselect Voltage	Regulator Disabled	3.90	4.10		V
V_{CCHYST}	Hysteresis Voltage	(Note 3)		0.20		V
$V_{R\ LOAD}$	Load Regulation	V_{CC} = 5 V, 5 mA < I_{LOAD} < 250 mA		20		mV
$V_{R\ LINE}$	Line Regulation	I_{LOAD} = 5 mA; 4.5 V < V_{CC} < to 5.5 V		2		mV
R_{SW}	V_{AUX} Switch Resistance	V_{CCDES} > V_{CC}, V_{AUX} = 3.3 V		0.25	0.40	Ω
I_{RCC} I_{RAUX}	V_{CC} Reverse Leakage V_{AUX} Reverse Leakage	V_{AUX} = 3.3 V, V_{CC} = 0 V V_{AUX} = 0 V, V_{CC} = 5 V		2 2	50 50	μA
I_{GND}	Ground Current	V_{CC} < V_{CCDES}, I_{LOAD} = 0 mA V_{CC} > V_{CCSEL}, I_{LOAD} = 0 mA V_{CC} > V_{CCSEL}, I_{LOAD} = 250 mA		0.20 0.60 0.70	0.40 1.00 1.20	mA
I_{AUX}	V_{AUX} Supply Current	V_{AUX} > V_{CC} V_{CC} > V_{AUX}		0.20 0.02	0.40 0.10	mA
R_{OH}	DRIVE Pull−up Resistance	R_{PULLUP} to V_{CC}, V_{CC} > V_{CCSEL}		4.0	8.0	kΩ
R_{OL}	DRIVE Pull−down Resistance	$R_{PULLDOWN}$ to GND, V_{CCDES} > V_{CC}		0.1	0.4	kΩ

2. Operating Characteristics are over Standard Operating Conditions unless otherwise specified.
3. The hysteresis defines the maximum level of acceptable disturbance on V_{CC} during switching. It is recommended that the V_{CC} source impedance be kept below 0.25 Ω to ensure the switching disturbance remains below the hysteresis during select/deselect transitions. An input capacitor may be required to help minimize the switching transient.

PERFORMANCE INFORMATION

CMPWR101 Typical DC Characteristics (nominal conditions unless specified otherwise)

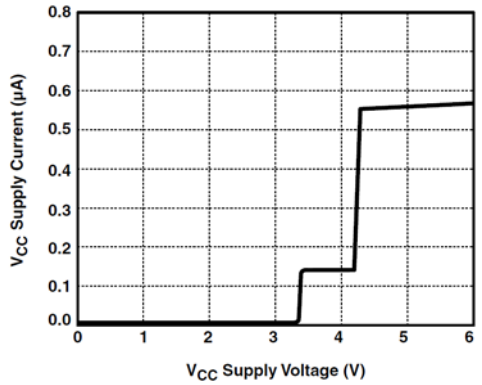


Figure 1. Supply Current vs. Voltage (V_{AUX} = 3.3 V)

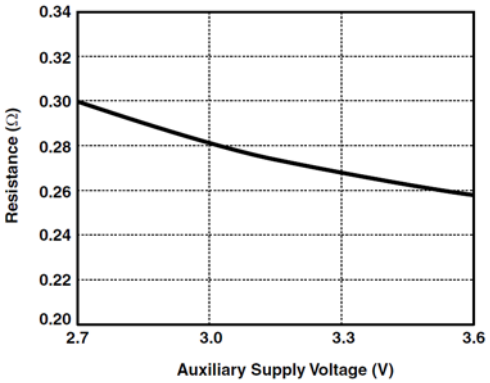


Figure 2. Switch Resistance vs. Supply Voltage

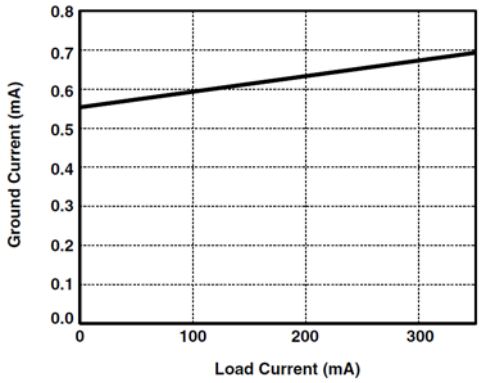


Figure 3. Ground Current vs. Output Load

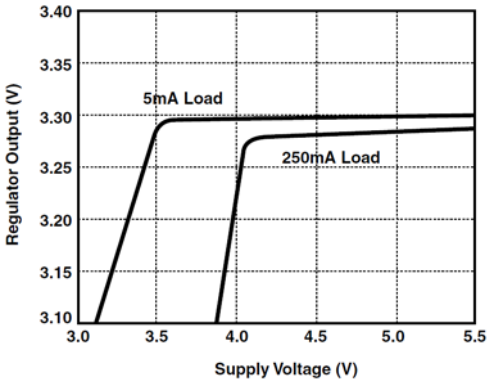


Figure 4. Line Regulation (1% and 100& Rated Load)

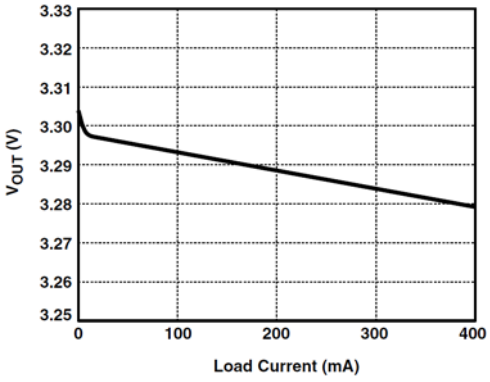


Figure 5. Load Regulation

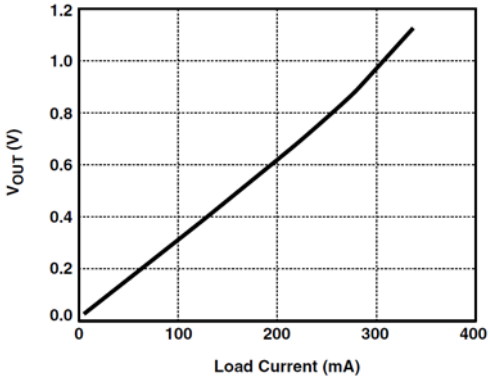


Figure 6. Dropout Voltage with Load Current

PERFORMANCE INFORMATION (Cont'd)

CMPWR101 Transient Characteristics (nominal conditions unless specified otherwise)
(V_{CC} source resistance set to 0.2 Ω)

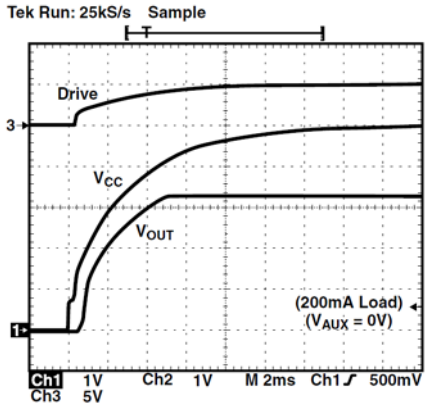


Figure 7. V_{CC} Cold Start Power Up (V_{AUX} = 0 V)

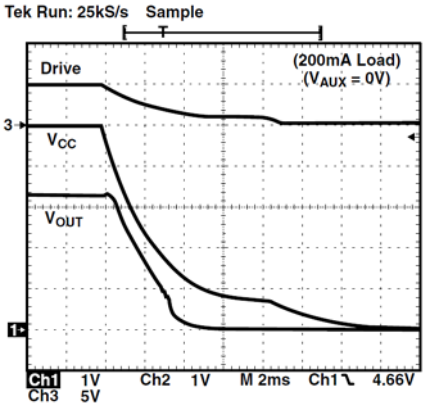


Figure 8. V_{CC} Complete Power Down (V_{AUX} = 0 V)

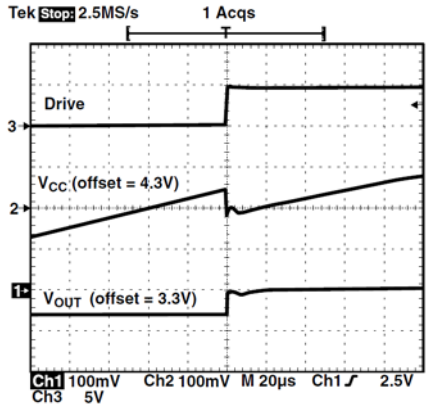


Figure 9. V_{CC} Power Up (V_{AUX} = 3.3 V)

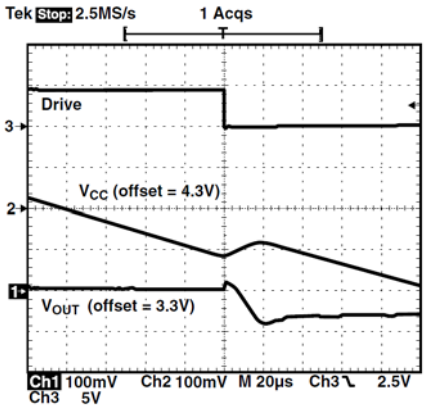


Figure 10. V_{CC} Power Down (V_{AUX} = 3.3 V)

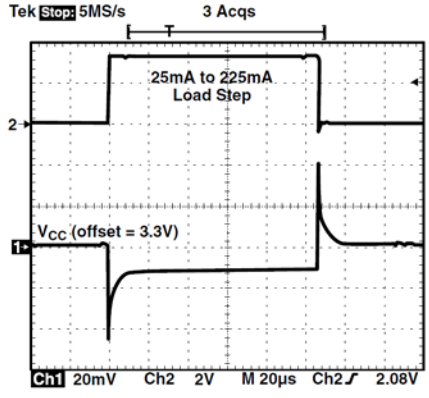


Figure 11. Load Transient (10% to 90%) Step Response

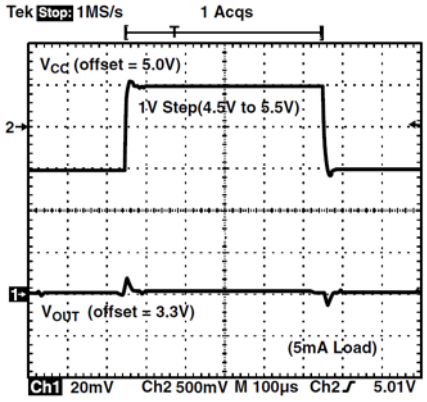


Figure 12. Line Transient (1 V_{PP}) Step Response

PERFORMANCE INFORMATION (Cont'd)

CMPWR101 Typical Thermal Characteristics

The overall junction to ambient thermal resistance (θ_{JA}) for device power dissipation (P_D) consists primarily of two paths in series. The first path is the junction to the case (θ_{JC}) which is defined by the package style, and the second path is case to ambient (θ_{CA}) thermal resistance which is dependent on board layout. The final operating junction temperature for any set of conditions can be estimated by the following thermal equation:

$$T_{JUNC} = T_{AMB} + P_D(\theta_{JC}) + P_D(\theta_{CA})$$
$$= T_{AMB} + P_D(\theta_{JA})$$

The CMPWR101 uses a standard SOIC package. When this package is mounted on a double−sided printed circuit board with two square inches of copper allocated for "heat spreading", the resulting θJA is 85°C/W.

Based on a maximum power dissipation of 0.43 W (1.7 V x 250 mA) with an ambient of 70°C, the resulting junction temperature will be:

$$T_{JUNC} = T_{AMB} + P_D(\theta_{JA})$$
$$= 70°C + 0.4\,W\,(80°C/D)$$
$$= 70°C + 37°C = 103°C$$

Thermal characteristics were measured using a double−sided board with two square inches of copper area connected to the GND pin for "heat spreading".

Measurements showing performance up to junction temperature of 125°C were performed under light load conditions (5 mA). This allows the ambient temperature to be representative of the internal junction temperature.

NOTE: Note: The use of multi−layer board construction with separate ground and power planes will further enhance the overall thermal performance. In the event of no copper area being dedicated for heat spreading, a multi−layer board construction, using only the minimum size pad layout, will provide the CMPWR101 with an overall θ_{JA} of 100°C/W which allows up to 500 mW to be safely dissipated.

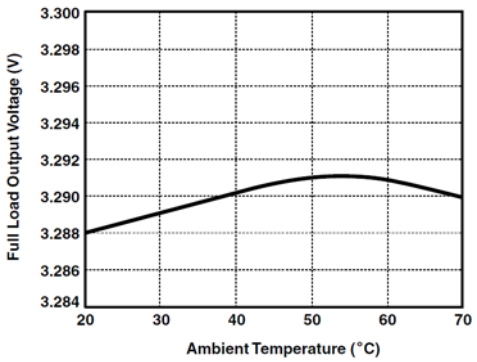


Figure 13. Regulator V_{OUT} vs. T_{AMB} (250 mA Load)

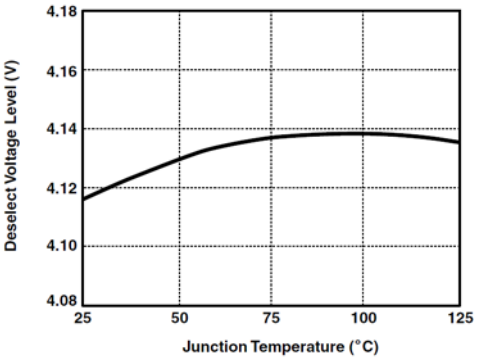


Figure 14. Deselect Threshold vs. T_{JUNCT}

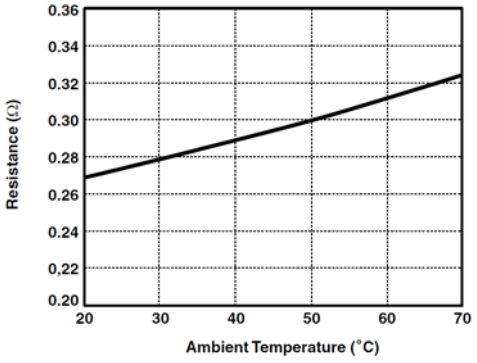
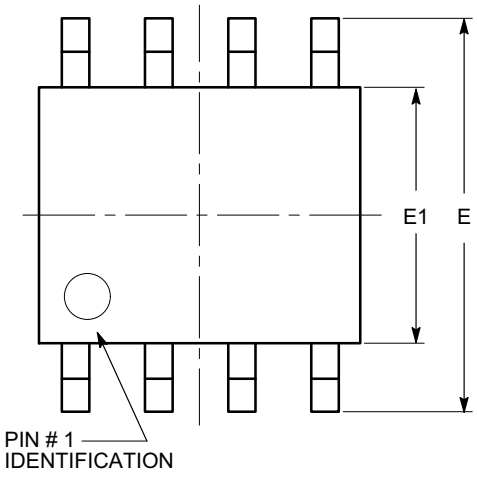


Figure 15. Switch Resistance vs. Ambient Temperature

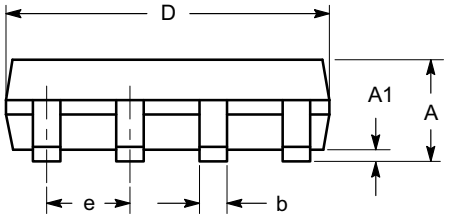
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD−01
ISSUE O

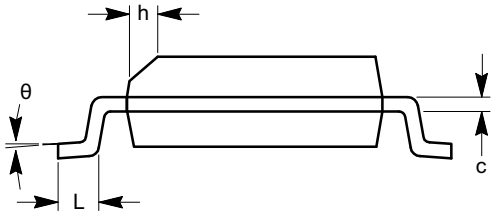


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0°		8°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

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CMPWR101/D