Ultra Low Power Microprocessor Reset IC

CN803/809/CN810

General Description

The CN803/809/810 series are micro- processor (µP) supervisory circuits used to monitor the power supplies in µP and digital systems. They provide excellent circuit reliability and low cost by eliminating external components.

These circuits perform a single function: they assert a reset signal whenever the V_{CC} supply voltage declines below a preset threshold, keeping it asserted for at least 140ms after V_{CC} has risen above the reset threshold.

The CN809/810 have CMOS outputs, the CN803 has open drain output. The CN803/809 have an active-low $\overline{RESET}$ output, while the CN810 has an active-high RESET output. The reset comparator is designed to ignore fast transients on V_{CC}, and the outputs are guaranteed to be in the correct logic state for V_{CC} down to 1.15V over the temperature range.

The device is available in 3 pin SOT23 package.

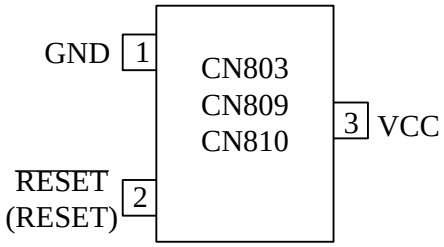
Applications

- Computers
- Portable/Battery-Powered Equipment
- Intelligent Instruments
- Controllers

Features

- Precise Reset Threshold: ±2.5%
- CMOS Output(CN809/810) and Open Drain Output(CN803)
- 140ms min Reset Pulse Width
- 3.2µA Supply Current @V_{CC}=3V
- Guaranteed Reset Valid to V_{CC} = +1.15V
- Power Supply Transient Immunity
- Operating Temperature Range
  -40°C to +85°C
- Available in SOT23-3

Pin Assignment



SOT23-3

( ) is for CN810 only

Device Function Reference Table:

Part No.	Reset threshold	Reset active Low or High	Output Type	Marking
CN809L	4.63V	Low	CMOS	AAAA
CN810L	4.63V	High	CMOS	AGAA
CN809M	4.38V	Low	CMOS	ABAA
CN810M	4.38V	High	CMOS	AHAA
CN809J	4.00V	Low	CMOS	CWAA
CN809T	3.08V	Low	CMOS	ACAA
CN803S	2.93V	Low	Open Drain	ABC
CN809S	2.93V	Low	CMOS	ADAA
CN810S	2.93V	High	CMOS	AKAA
CN803R	2.63V	Low	Open Drain	ABD
CN809R	2.63V	Low	CMOS	AFAA

Block Diagram

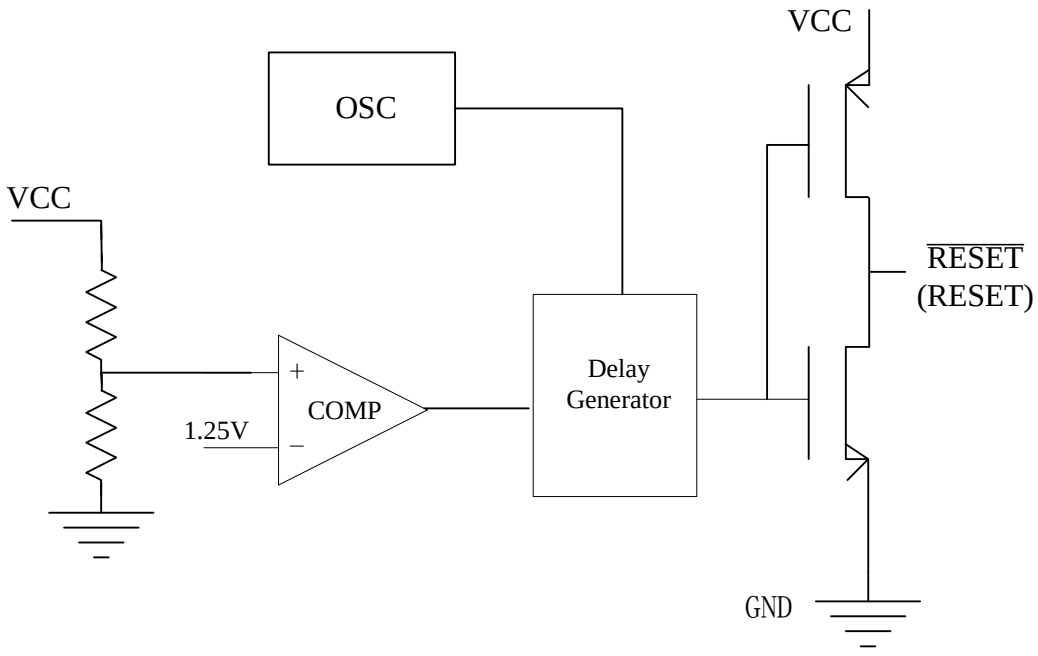


Fig.1 Block Diagram For CMOS Output

Pin Description

Pin No.	Symbol	Description
1	GND	**Ground terminal**
2	$\overline{RESET}$ (CN809)	**CMOS Output**. This output remains low if V_{CC} drops below V_{RES}, and for at least 140ms after V_{CC} rises above $V_{RES} + V_{HYST}$.
	RESET (CN810)	**CMOS Output**. This output remains high if V_{CC} drops below V_{RES}, and for at least 140ms after V_{CC} rises above $V_{RES} + V_{HYST.}$
	$\overline{RESET}$ (CN803)	**Open Drain Output**. This output remains low if V_{CC} drops below V_{RES}, and for at least 140ms after V_{CC} rises above $V_{RES} + V_{HYST}$.
3	V_{CC}	**Analog Input**. This pin is both the power supply to internal circuit and the voltage to be monitored.

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (With respect to GND)

V_{CC}.....-0.3V to +6.0V

$\overline{RESET}$, RESET …...-0.3V to +6.0V

Input/Output Current

V_{CC} 20mA

$\overline{RESET}$, RESET ..…….....20mA

Thermal Resistance……..300°C/W

Operating Temperature…...……...-40 to +85°C

Storage Temperature.....…….....-65 to +150°C

Maximum Junction Temperature... +150°C

Lead Temperature (soldering, 10s) .....+300°C

ESD Rating(HBM)…….…….……4KV

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics (V_{CC}=3V, T_A= －40℃ to 85℃, Typical values are at T_A=25℃, unless otherwise noted.)

Parameters	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum input voltage	V_{CCMAX}		5.5			V
Minimum input voltage	V_{CCMIN}				1.15	V
Supply current	I_{VCC}	V_{CC}=2.0V		2.8	5.5	uA
		V_{CC}=3.0V		3.2	6	
		V_{CC}=5.0V		4.0	7.5	
Reset Threshold	V_{RES}	CN8__L	4.51	4.63	4.75	V
		CN8__M	4.25	4.38	4.5	
		CN8__J	3.89	4.00	4.11	
		CN8__T	3.0	3.08	3.15	
		CN8__S	2.86	2.93	3.0	
		CN8__R	2.56	2.63	2.7	
		CN8__Z	2.26	2.32	2.38	
Reset Threshold hysteresis	V_{HYST}			0.013V_{RES}		V
V_{CC} to $\overline{RESET}$ Delay(CN803/809)		V_{CC} transitions from V_{RES}+0.1V to V_{RES}－0.1V		20		us
V_{CC} to RESET Delay(CN810)		V_{CC} transitions from V_{RES}+0.1V to V_{RES}－0.1V		20		us
$\overline{RESET}$ Output Voltage Low (CN803/809)	V_{OL}	V_{RES}>V_{CC}=2V,I_{SINK}=1.5mA			0.3	V
		V_{RES}>V_{CC}=3V,I_{SINK}=3.2mA			0.3	
		V_{RES}>V_{CC}=4V,I_{SINK}=5mA			0.3	
$\overline{RESET}$ Output Voltage High (CN809)	V_{OH}	V_{RES}<V_{CC}=3V,I_{SRC}=1.2mA	V_{CC}-0.4			V
		V_{RES}<V_{CC}=4V,I_{SRC}=2mA	V_{CC}-0.4			
		V_{RES}<V_{CC}=5V,I_{SRC}=2.5mA	V_{CC}-0.4			
RESET Output Voltage Low (CN810)	V_{OL}	V_{RES}<V_{CC}=3V,I_{SINK}=3.2mA			0.3	V
		V_{RES}<V_{CC}=4V,I_{SINK}=5mA			0.3	
		V_{RES}<V_{CC}=5V,I_{SINK}=6mA			0.3	
RESET Output Voltage High (CN810)	V_{OH}	V_{RES}>V_{CC}=2V,I_{SRC}=600uA	V_{CC}-0.4			V
		V_{RES}>V_{CC}=3V, I_{SRC}=1.2mA	V_{CC}-0.4			
		V_{RES}>V_{CC}=4V, I_{SRC}=2mA	V_{CC}-0.4			
Reset Pulse Width	T_{RES}		140	240	400	ms

Note : Parts are 100% production tested at 25°C. Specifications over full temperature range are guaranteed by design

Detailed Description

A microprocessor's (µP's) reset input starts the µP in a known state. The CN803/809/810 series assert reset to prevent code-execution errors during power-up, power-down, or brownout conditions. The device consists of a comparator, a low current high precision voltage reference, voltage divider, output delay circuit and output driver. They assert a reset signal whenever the V_{CC} supply voltage declines below a preset threshold, keeping it asserted for at least 140ms after V_{CC} has risen above the reset threshold.
The CN809/810 have a CMOS output stage, the CN803 has an open drain output stage. The CN803/809 have an active-low $\overline{RESET}$ output, while the CN810 has an active-high RESET output. The reset comparator is designed to ignore fast transients on V_{CC}, and the outputs are guaranteed to be in the correct logic state for V_{CC} down to 1.15V over the temperature range.
The operation of the device can be best understood by referring to figure 3.

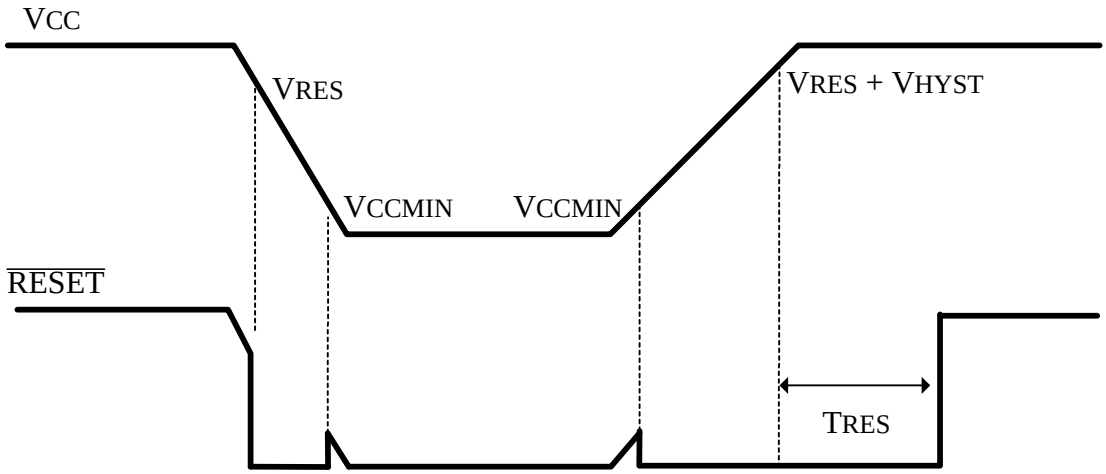


Fig.2 Timing waveform

Applications Information

Negative-Going V_{CC} Transients

In addition to issuing a reset to the µP during power-up, power-down, and brownout conditions, the CN803/809/810 series are relatively immune to short-duration negative-going V_{CC} transients (glitches). As the magnitude of the transient increases (goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 100mV below the reset threshold and lasts 10µs or less will not cause a reset pulse. A 0.1µF bypass capacitor mounted as close as possible to the V_{CC} pin provides additional transient immunity.

Ensuring a Valid Reset Output Down to V_{CC} = 0

When V_{CC} falls below 1.15V, the CN809 $\overline{RESET}$ output no longer sinks current—it becomes an open circuit. Therefore, high-impedance CMOS logic inputs connected to $\overline{RESET}$ can drift to undetermined voltages. This presents no problem in most applications, since most µP and other circuitry is inoperative with V_{CC} below 1.15V. However, in applications where $\overline{RESET}$ must be valid down to 0V, a pull-down resistor is needed from $\overline{RESET}$ pin to GND as shown in Figure 4, then $\overline{RESET}$ output will be held at low state. The resistor's value is not critical, it should be about 100KΩ, large enough not to load $\overline{RESET}$,

small enough to pull $\overline{RESET}$ to ground.

A 100KΩ pull-up resistor to V_{CC} is also recommended for the CN810 if active high RESET is required to remain valid for V_{CC} < 1.15V.

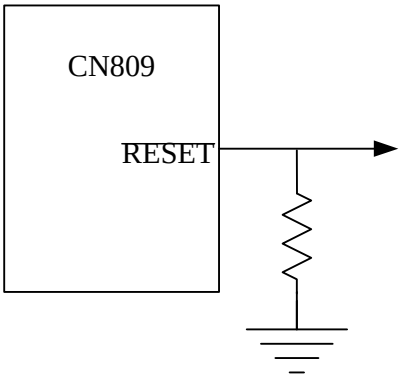
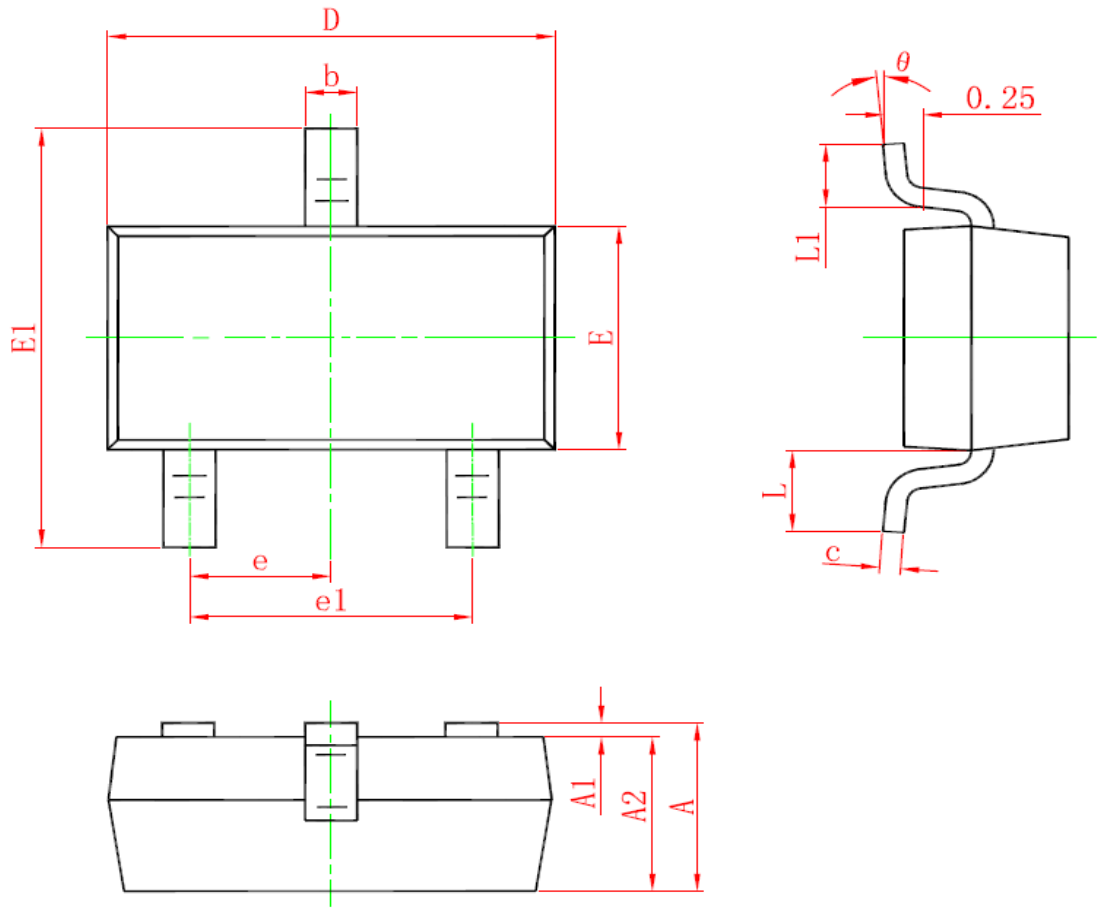


Fig.3 RESET Valid to Ground Circuit

Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP.		0.037 TYP.	
e1	1.800	2.000	0.071	0.079
L	0.550 REF.		0.022 REF.	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°