# PROCESS CP207

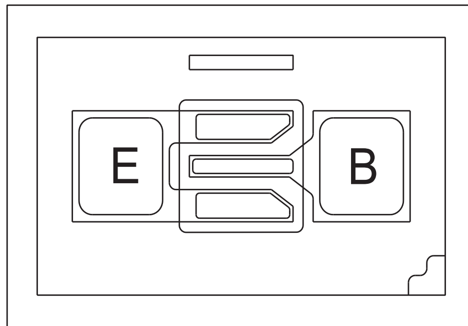
## Small Signal Transistor

### NPN - Saturated Switch Transistor Chip

**PROCESS DETAILS**

| Process | EPITAXIAL PLANAR |
|---|---|
| Die Size | 9.0 x 14 MILS |
| Die Thickness | 8.0 MILS |
| Base Bonding Pad Area | 2.7 x 2.7 MILS |
| Emitter Bonding Pad Area | 2.7 x 2.7 MILS |
| Top Side Metalization | Al - 13,000Å |
| Back Side Metalization | Au - 6,000Å |

**GEOMETRY**




BACKSIDE COLLECTOR

R1

**GROSS DIE PER 4 INCH WAFER**

93,430

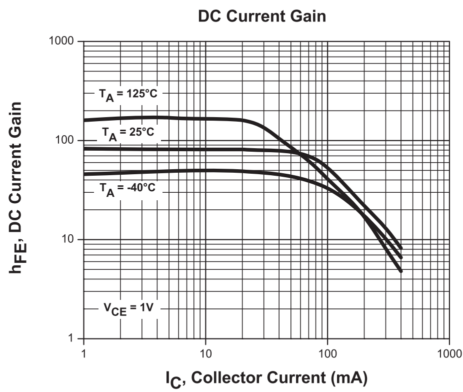
**PRINCIPAL DEVICE TYPES**

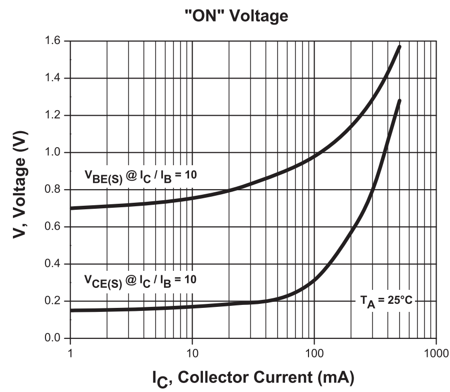
2N2369A
CMPT2369

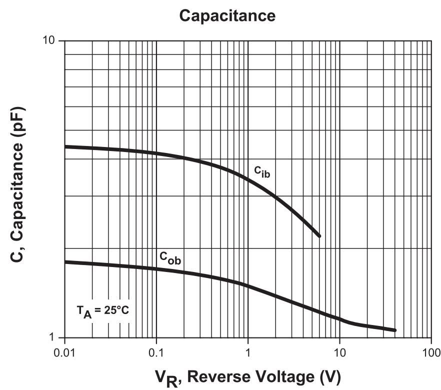
R4 (22-March 2010)

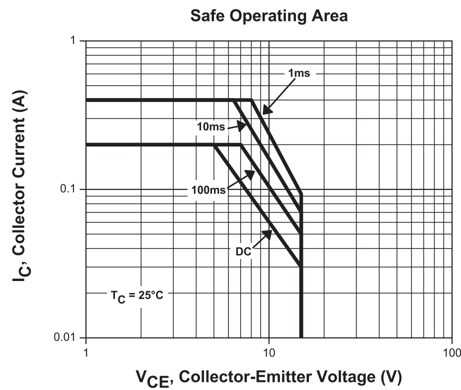
# PROCESS CP207

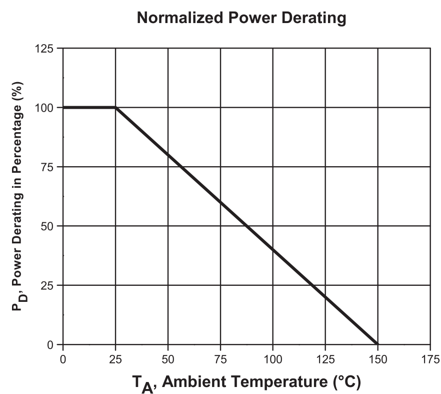
## Typical Electrical Characteristics

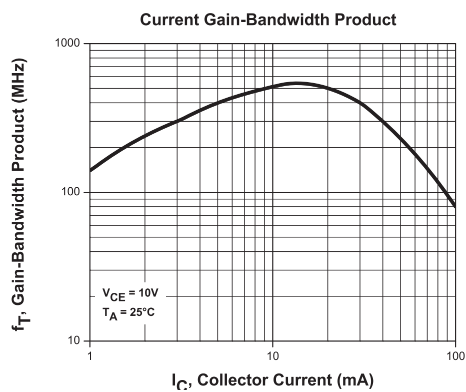



R4 (22-March 2010)